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Colin Hinson
In the village of Blunham, Bedfordshire.

SECTION I

GENERAL DESCRIPTION

1-1 SCOPE OF MANUAL.

This manual describes theory of operation and preventive and corrective maintenance procedures for the Texas Instruments Silent 700* Model 742 Programmable Data Terminal (PDT) manufactured by the Digital Systems Division of Texas Instruments Incorporated. Information presented herein is intended to aid maintaining and servicing the Model 742 PDT. This manual is a supplement to the basic ASR/KSR Maintnenace Manual. Additional information concerning the terminal is contained in the Silent 700 ASR/KSR Electronic Data Terminals Models 732/733 ASR/KSR Maintenance Manual (TI Manual No. 960129-9701).

The maintenance information in this manual is intended to help service personnel solve minor maintenance problems in the field and assist analysis of major troubles at regional TI service centers. A general description of the Model 742 is included in this manual, along with necessary interfacing information. A general theory of operation for PC cards and subsystems unique to the Model 742 and a troubleshooting guide are also included herein. Parts lists and related mechanical and electrical drawings of unique Model 742 devices are included in the appendixes to this publication.

1-2 EQUIPMENT DESCRIPTION.

The Model 742 is an automatic send/receive, programmable data terminal utilizing the USASCII code and character set. The Model 742 Programmable Data Terminal is capable of loading a format program from cassette into RAM memory and executing the program to control keyboard data entry in the local operational mode (off-line).

The Model 742 is also capable of transmitting, receiving, playing back from tape, and recording on tape the ASCII code and character set at switch-selectable speeds of 10, 15, 30, or 120 characters per second (CPS) via a standard EIA line interface. Functions such as tape edit or high speed tape duplication are also possible in the off-line (local) mode.

The following options are available for the Model 742:

- Answer-back memory
- Multidrop communications
- 1200-baud internal modem
- Reverse channel control.

1-3 OPTIONAL EQUIPMENT.

1-3.1 ANSWER-BACK MEMORY. The Answer-Back Memory option provides up to 21 programmable, nonvolatile characters. The Answer-Back Memory is normally programmed into the Processor PC card control PROM at the factory, according to the customer-specified pattern.

1-3.2 MULTIDROP COMMUNICATIONS. Equipped with this option the Model 742 responds to polling from a computer. Each terminal has a switch-selectable station identification character to distinguish it from other terminals on the same communication line. This permits the computer to select a particular terminal or terminals for communications on a multidrop line.

1-3.3 1200-BAUD MODEM. The 1200-Baud Modem option line interface replaces the standard EIA interface. The 1200-Baud Modem conforms to the Bell type CBS Data Access Arrangement (DAA). The 1200-Baud Modem operates asynchronously up to a maximum speed of 1200 baud in half-duplex over a two-wire voice-grade line. Signaling is accomplished by frequency shift keying (FSK).

1-3.4 REVERSE CHANNEL. This option is designed to provide circuit assurance. A 387-Hz reverse channel signal is generated by the receiving station to indicate to the transmitting station that the receiving station is in a receiving mode.

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TABLE 2-4.1. EIA WITH AUTO ANSWER INTERFACE CABLE PIN FUNCTIONS
(CABLE 969626-0001)

Connector Pin Numbers		Pin Function[1]
PDT Terminal	Data Set	
6	20	Data Terminal Ready
7	7	Signal Ground
8	5	Clear to Send[2]
9	6	Data Set Ready[3]
10	3	Received Data
A	1	Protective Ground
F	4	Request to Send
H	2	Transmitted Data
K	8	Data Carrier Detect[4]
J	22	Ring Indicator
5	11	Reverse Channel Transmit Data
4	12	Reverse Channel Receive Data

NOTES:
[1] All are used only with external modem.
[2] Held to an ON condition by data set during transmission; required by terminal for transmission.
[3] Held to an ON condition when data set is operative; required for terminal operation.
[4] Held to an ON condition by modem when carrier is received; required by terminal for data reception.

TABLE 2-4.2. INTERNAL 1200 BAUD MODEM PIN FUNCTIONS
(CABLE 973260-0001)

PDT Terminal	Cable Lead Colors	DAA Terminal Marking	Signal Name
7	Black	SG	Signal Ground
B	Brown	DA	Data Access
D	Red	OH	Off Hook
E	Orange	DT	Data Tip
3	Yellow	DR	Data Ring
J	Green	RI	Ring Indicator
2	Blue	SH	Switch Hook
1	White	CCT	Coupler Cut Through

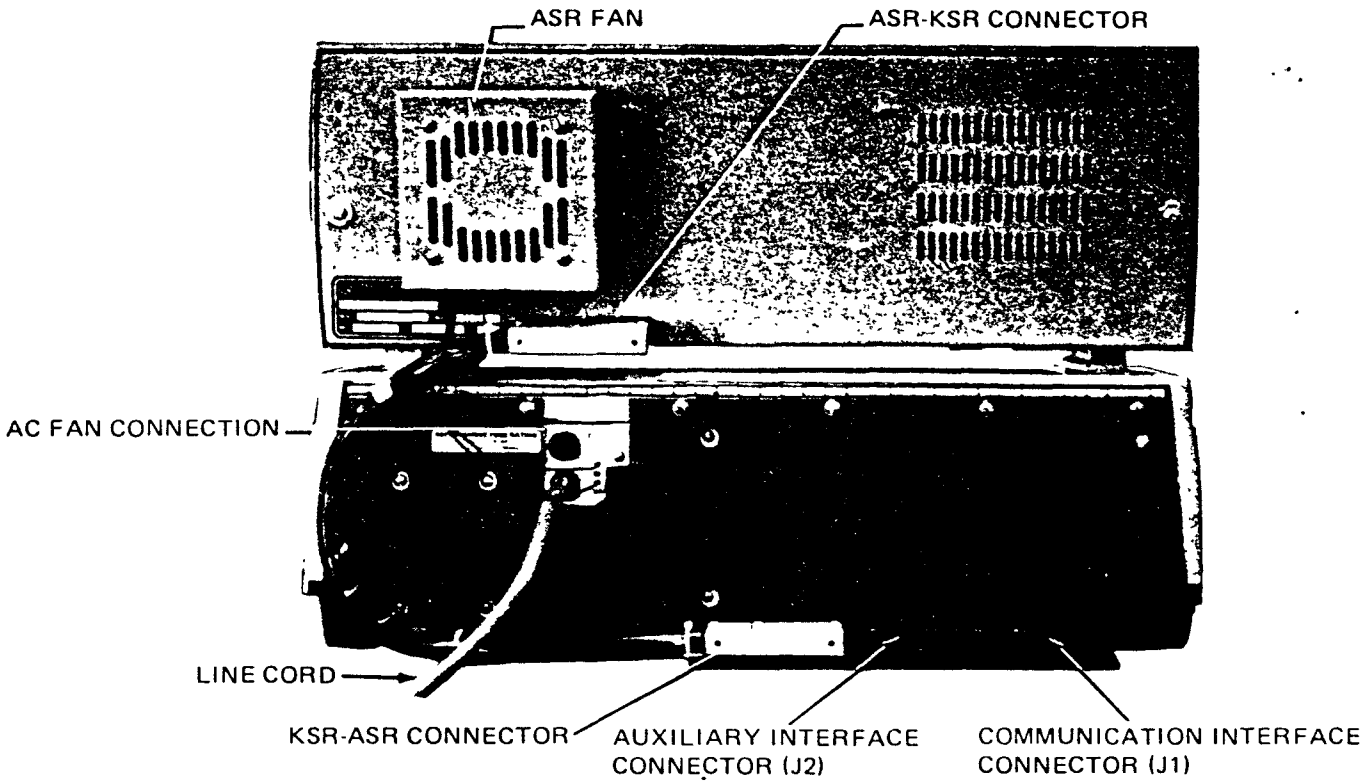

FIGURE 2-4.1 MODEL 742 REAR VIEW, SHOWING CONNECTORS

The auxiliary interface connector (pin assignments are shown in Table 2-4.3) provides several EIA-level signals.

TABLE 2-4.3.
AUXILIARY CABLE PIN FUNCTIONS

PDT Terminal	AUX P13	Signal Name
11	3	EIA Data Out
12	12	EIA Control In
13	11	EIA Control Out
1	7	EIA Signal Ground
	4	EIA Request to Send[1]
	5	EIA Clear to Send[1]
	6	EIA Data Set Ready[2]
	8	EIA Data Carrier Detect[2]
	20	EIA Data Terminal Ready[2]

NOTES:
[1] Pins 4 and 5 are jumpered together.
[2] Pins 6, 8, and 20 are jumpered together.

2-5 PAPER LOADING.

CAUTION

The printer should never be operated without paper on the platen (drive roller); damage to both platen and printhead could result.

The data terminal must be loaded with paper before applying power. Load the paper as follows:

a. Raise the terminal cover and lift the window/pinch roller (see Figure 2-5.1).

b. Place a fresh roll of Texas Instruments Silent 700 printing paper (TI Part No. 213714) on the supply hubs, ascertaining that the roll can rotate freely.

c. Thread paper between the paper chute and the drive roller as shown in Figure 2-5.1. Be sure paper is centered in the paper chute.

d. Lower the window.

e. Set the POWER switch ON and depress the PAPER ADV key. Make sure paper is feeding smooth and straight.

f. Close the data terminal cover, ascertaining that paper is fed through the slot in the cover.

2-6 STRAPPABLE OPTIONS, END-OF-LINE ALARM.

The end-of-line alarm can be prevented from sounding automatically by removing R20 (10 ohms) by hand from connectors J1 and J2 on the Printer Control PC card (red tabbed card in slot A2 of the KSR card rack). If this feature is wanted, hand insert the 10-ohm resistor (R20) between J1 and J2 on the Printer Control card. Removal of R20 will not inhibit the alarm from sounding upon receipt of the ASCII BEL character.

2-7 OPTIONS.

2-7.1 ANSWER-BACK MEMORY. To gain this option, the PROM located at U37 of the Processor PC card (slot A-6, lower unit) must be replaced by a PROM configured at the factory to provide Answer-Back Memory.

2-7.2 MULTIDROP COMMUNICATION. To gain this option, the PROM located at U37 of the Processor PC card (slot A-6, lower unit) must be replaced by a PROM configured at the factory to provide multidrop communication.

2-7.3 1200-BAUD INTERNAL MODEM. To gain this option, a PC card (TI Part No. 959348-001) is inserted in lower unit PC card slot A-8. Installation requires removal of the Expansion and Processor PC cards to enable the Modem PC card to slip safely past the status display panel cable (see Section V). In addition, the modem cable (TI Part No. 973260-0001) must be installed as described in Section 2-4. An optional PROM configured to provide Auto-Answer also must be installed (see the 1200-Baud Modem Installation Instructions, TI Publication No. 973296-9701).

2-7.4 REVERSE CHANNEL. To gain this option, the PROM located at U37 of the Processor PC card must be replaced by a PROM configured at the factory to provide reverse channel operation. This option cannot be used with the 1200-Baud Modem option described in Section 2-7.3.

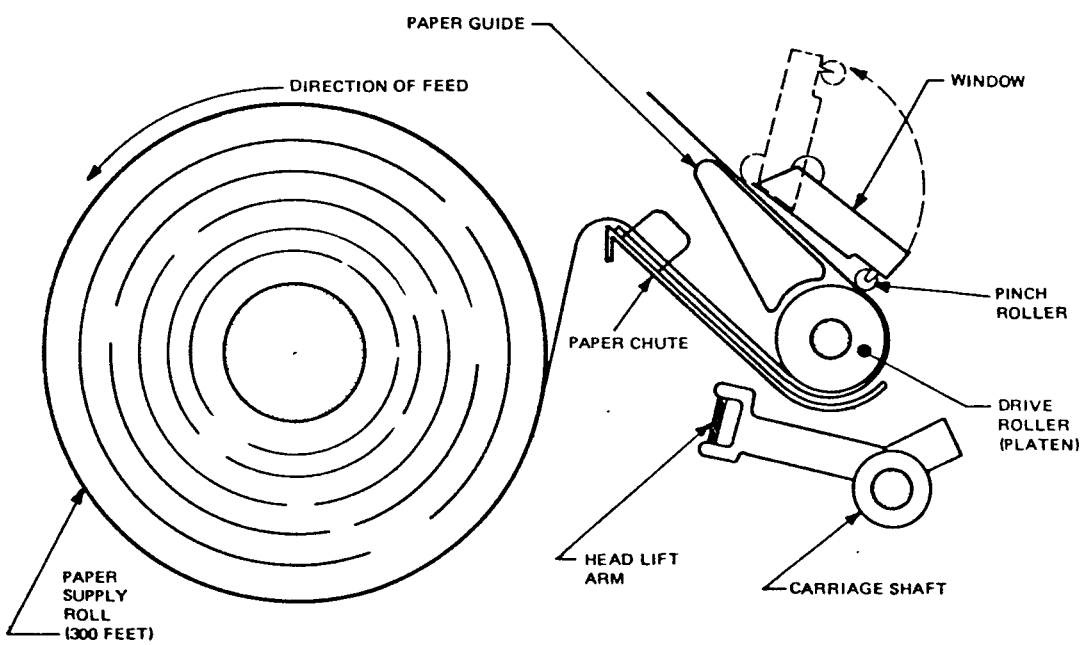

FIGURE 2-5.1. PAPER LOADING

SECTION III

THEORY OF OPERATION

3-1 FUNCTIONAL DESCRIPTION.

The Texas Instruments Silent 700* Model 742 Programmable Data Terminal is structured similar to a small computer system as diagrammed in Figure 3-1.1. The functional characteristics of the Model 742 are determined by a control program contained in read-only-memory and the input/output devices shown in the block diagram. Nine basic functions are performed within each Model 742 PDT:

- Control program (Paragraph 3-3)
- Power supply (Paragraph 3-4)
- Printer (Paragraph 3-5)
- Keyboard and interface (Paragraph 3-6)
- Line interface (Paragraphs 3-7, 3-12)
- Terminal control (Paragraph 3-8)
- Dual cassette subsystem (Paragraph 3-9)
- Processor (Paragraphs 3-10 and 3-11)
- Terminal status display (Paragraph 3-13)

Frequent references are made in this section to Texas Instruments assembly and electrical drawings contained in the appendixes to this manual.

As in any computer system, the functional operation of the Model 742 may not be completely understandable after studying the hardware functions and the control program. The purpose of this section is to explain the combined functional characteristics of the firmware (ROM control programs and hardware).

The Model 742 is a standard TI Model 733 ASR Data Terminal with a special keyboard, a microprocessor controller, a special terminal control PC card, special controls and indicators, and an optional 1200-baud modem all contained in a single package. The keyboard features a numeric cluster and function keys to facilitate rapid, formatted data entry and editing. The microprocessor provides the basic format and keyboard input storage, control of terminal functions, error checking on keyboard input, control of operating modes, and control of communications with a central computer. As shown in Figure 3-1.1, the processor provides control for all terminal functions. All input devices (playback, keyboard, and communications line receiver) send characters to the processor. The processor may store the characters, output them, or decode them and perform some control operation. Characters output by the processor may be sent to any or all of the output devices (recorder, printer, and communications line transmitter).

The Model 742 Data Terminal may be used to prepare or collect data under control of the local processor program at the same time the communication line program is controlling communication with the central computer. The keyboard, printer, playback, and record functions may each be placed under the control of local or line programs (or off) by means of four 3-position switches on the ASR module (upper unit) display panel. The line program and the communication line transmitter and receiver are enabled by setting the terminal ON-LINE switch to ON-LINE. All line and local control programs are in read-only-memory (ROM); therefore, all basic terminal functions are operable when power is first applied.

The programmability of the terminal is limited to local operation and is oriented toward formatting and error checking of input data. The operator must select the I/O devices (keyboard, printer, playback, and record) which are to be controlled by the local processor program by setting the appropriate switches to the local positions. The selected devices may be used to generate, edit, duplicate, or list cassette tapes, either manually or under control of a stored format program.

The line program controls all communication with the central computer. It monitors and controls the EIA lines to the data access arrangement (DAA) on the telephone line or an external modem and automatically establishes or terminates the connection with the computer. It controls the communication line transmitter and receiver and any of the I/O devices the operator selects for line operation. The central computer may remotely control the line I/O devices through special control characters which the line program recognizes. Data may be transmitted and received in

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blocked form with character parity and block LRC checking to ensure error-free communication.

3-1.1 LOCAL OPERATION. Local operation of the Model 742 may be understood by studying the local controller program state diagram, Figure 3-1.2. When power is first applied, the program enters local state 1 (LOC1) which is called the NORMAL mode. In NORMAL mode, tapes may be generated, listed, and duplicated.

The local controller program may enter four additional modes:

- Search
- Load format program
- Execute format program
- Load and execute octal programs.

These modes are entered by pressing the ESC key on the keyboard, followed by pressing the appropriate character. In the search mode a search ID up to 16 characters long may be entered (LOC3), and the playback cassette will be searched (LOC4) for this character sequence. The format loader (LOC5) loads a format program from the playback cassette into random access memory (RAM). In the EXECUTE mode, format programs contained in RAM are interpreted (LOC6) and local operation of the Model 742 is under control of this user-generated program. A detailed explanation of the format language is contained in the Model 742 Programmer's Reference Manual (TI Manual No. 974011-9701). The octal program loader is used to load machine language programs from the playback cassette into the RAM. Control of all Model 742 functions is turned over to this program when loading is complete. This mode of operation is used primarily to help test and debug the Model 742.

The following local indicators are located on the status display panel:

ERROR – a steady light indicates an input error; it is cancelled by pressing the RUB OUT, HOME, or BREAK key

BUSY – a steady light indicates the terminal is busy; the operator must wait for the light to extinguish before continuing to enter data

NORMAL MODE – a steady light indicates the terminal is in the normal mode

EXECUTE MODE – a steady light indicates the terminal is in the execute mode.

3-1.2 LINE OPERATION. The line controller program is disabled when the terminal ON-LINE switch is in the OFF position. Set to the ON-LINE position, the line controller performs the functions of line discipline, remote device control, data communication, answer-back memory, and line protocol.

3-1.2.1 Line Controls. The Model 742 is equipped with six switches in addition to the terminal ON-LINE switch to control line operation.

RDC ON/OFF switch – located on the Processor PC card, accessible through the top of the PC card rack cover; set to the ON position to enable the remote device control function

LINE PROTOCOL select switch – a three-position switch located on the Expansion PC card, accessible through the top of the PC card rack cover. Set to the left position the line protocol is blocked; set to the right position the line protocol is TTY-compatible (not blocked). in both the left and right position the line discipline function is enabled. Set to the center position the line discipline function is bypassed, and the terminal is enabled to transmit and receive in the nonblocked mode.

HI-SPEED switch – located on the POWER switch panel; in the HI position the terminal transmits and receives at 1200 baud. In the LO position the terminal transmits at 110, 150, or 300 baud, depending on the setting of the PC card rack SPEED switch. This switch also affects the auto answer function and modem turnaround operation.

SPEED switch – a three-position switch, located on the Transmit/Receive PC card, accessible through the top of the PC card rack cover. The switch is functional only when the HI-SPEED switch is set to LO. The left, center, and right positions correspond to terminal transmit and receive speeds of 110, 150, and 300 baud, respectively.

PARITY switch – a three-position switch located on the Transmit/Receive PC card, accessible through the top of the PC card rack cover. The left, center, and right positions of this switch result in transmitted character

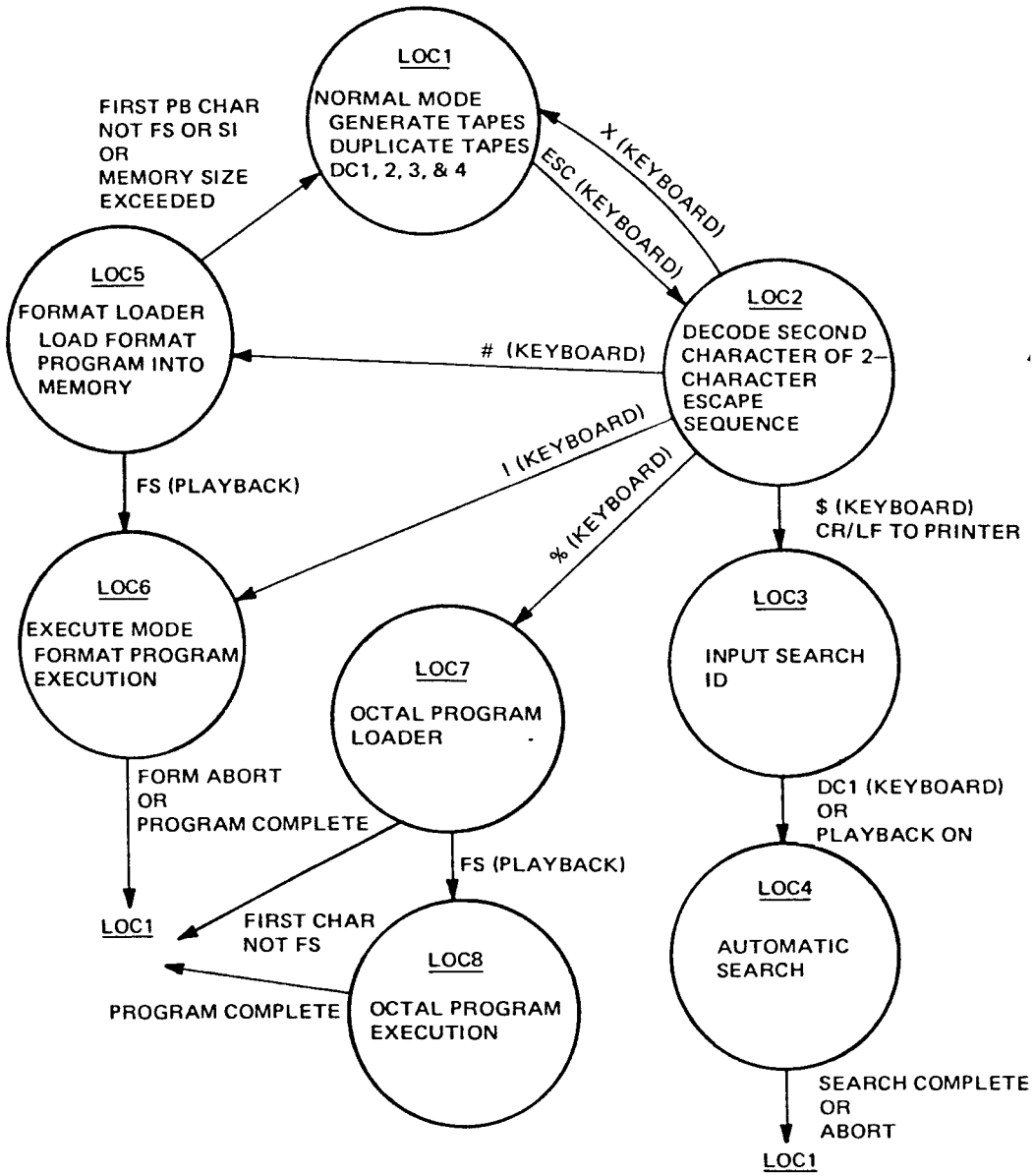


FIGURE 3-1.2. LOCAL CONTROLLER STATE DIAGRAM

parity of odd, mark, and even, respectively. This switch must be set to EVEN for correct block communication.

FULL/HALF DUPLEX switch – located on the Transmit/Receive PC card, accessible through the top of the PC card rack cover. Set to the HALF duplex (left) position, data transmitted in the nonblocked mode may also be printed and recorded (if these devices are on). Set to the FULL duplex (right) position, data which is transmitted in the nonblocked mode is not printed or recorded. This switch must be set to the FULL duplex position for blocked communication. The terminal always communicates in a half duplex mode regardless of the position of this switch, since this is fixed by the communication controller program.

3-1.2.2 Line Indicators. The following indicators are located on the terminal status display panel.

RING INDICATOR – a flashing light indicates the terminal is being called

TERMINAL READY – a steady light indicates the terminal is ready to answer a call (i.e., the terminal ON-LINE switch is in the ON-LINE position).

TRANSMIT MODE – a steady light indicates the terminal is in the transmit mode; this indicator is off until a call is answered and when the terminal is in the receive mode.

RECEIVE MODE – a steady light indicates the terminal is in the receive mode; this indicator is off until a call is answered and when the terminal is in the transmit mode.

3-1.2.3 Line Discipline. The line discipline program establishes and terminates connection to the communication line. The line discipline selected may be either automatic answer for use in a dial network or polling for use in a multidrop environment. Selection is determined by setting the appropriate PROM bit in the control PROM on the Processor PC card. The line discipline program may be disabled by setting the LINE PROTOCOL switch to the center position.

A state flow diagram of the line discipline program is shown in Figure 3-1.3. The program is in state LIN0 whenever the terminal ON-LINE switch is in the OFF position, and no line communication can occur. When the terminal is switched ON-LINE, the program goes to LIN1 and checks the LINE PROTOCOL switch to determine if the line discipline should be disabled. If it is disabled, the program goes to LIN2 and the terminal is enabled to transmit and receive characters in the nonblocked mode. The program switches on the EIA data-terminal-ready (DTR) signal in this state to permit establishment of a connection. The program remains in LIN2 until the terminal ON-LINE switch is set to the OFF position.

If the line discipline program is not disabled, the PROM bit is tested to determine if auto-answer or polling is selected. The following sections describe these two line disciplines.

a. Automatic answer. With automatic answer line discipline the terminal may be interfaced through a Bell 202C modem, a Bell 103A modem, or a Bell Type-CBS Data Access Arrangement (DAA) or equivalents in conjunction with the optional internal 202C-compatible modem. The EIA control and status lines used by the auto answer function are accessed through a cable which plugs into the J1 connector at the rear of the terminal. When an internal modem is used, it performs part of the auto answer function and supplies the additional signals required by the DAA.

- Answering A Call. The auto answer program remains in state LIN1 with DTR switched off until the EIA data set ready (DSR) signal is switched off by the modem to ensure that a disconnect has been completed. When the modem switches off, the auto answer program goes to state LIN6 and switches on DTR. This enables the modem to answer a call when the EIA ring indicator (RI) signal is received. When the modem senses a RI signal with DTR switched on, it answers the call, transmits a 3 to 5 second answer tone, and then switches DSR on.

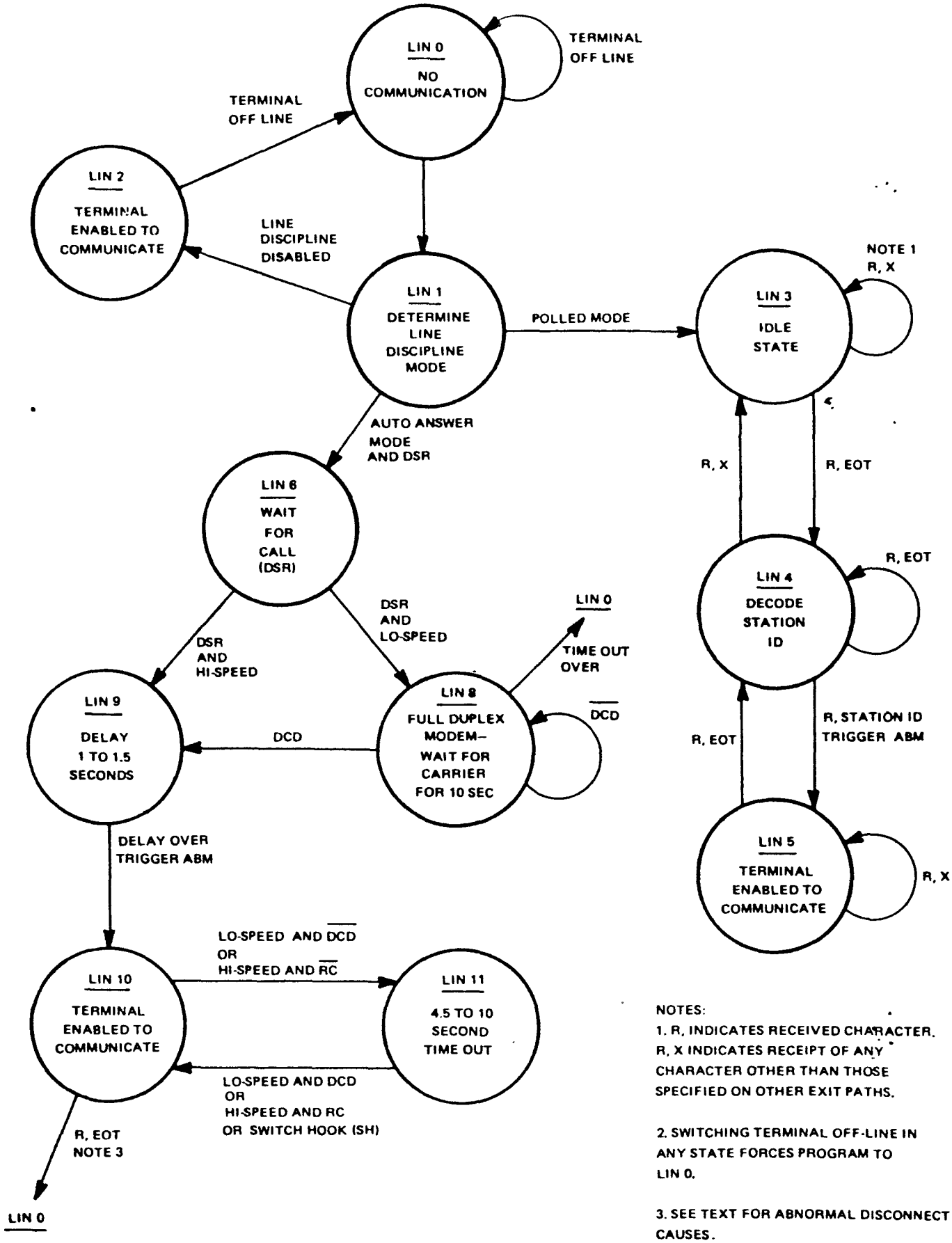


FIGURE 3-1.3. LINE DISCIPLINE STATE DIAGRAM

When the auto answer program senses DSR and the HI-SPEED switch is set to LO (indicating a type-103A full-duplex modem), it goes to state LIN8 and waits for the modem to switch on the EIA data carrier detect (DCD) signal. If the modem does not switch on DCD within 9 to 11 seconds, the auto answer program returns to state LIN0 and disconnects the call. When the modem switches DCD on, the auto answer program goes to state LIN9.

If the HI-SPEED switch is set to HI when DSR is switched on, the auto answer program goes to state LIN9. The program remains in LIN9 for 1.0 to 1.5 seconds to allow the communication line to settle. It then goes to state LIN10 and triggers the answer-back memory program if the appropriate control PROM bit is set to select this option.

Once the auto answer program is in state LIN10, the answering function is completed and the communications controller program is allowed to receive and transmit data. Then the function of the auto answer program is to decide when a call should be terminated.

- Terminating A Call. A call normally is terminated by the central computer sending an EOT character when the terminal is not waiting to receive the completion of a data block or the acknowledge to a transmitted data block (when line protocol is blocked). The auto answer program terminates a call by switching off DTR to the modem and returning to state LIN0.

  The auto answer program will terminate the call when any of the following abnormal conditions occur:

  (1) The modem switches off DSR.

  (2) No character is transmitted for a period of 40 to 45 seconds when the LINE PROTOCOL switch is set to the left (blocked) position and the EIA switch hook (SH) signal from the DAA is not on.

  (3) No character is received or transmitted for a period of 9 to 11 seconds when the LINE PROTOCOL switch is set to the right (nonblocked) position and the SH signal is not on.

  (4) The DCD signal is switched off by the modem for a period of 4.5 to 10 seconds when the HI-SPEED switch is set to LO (indicating 103A-type full-duplex modem).

  (5) The EIA reverse channel receive signal is switched off by the modem for a period of 4.5 to 10 seconds when the terminal is in the transmit mode, the HI-SPEED switch is set to HI, and the reverse channel option is selected by the appropriate control PROM bit.

  (6) The terminal ON-LINE switch is set to OFF.

b. Polling. With polling line discipline the terminal may be interfaced through a Bell 202D modem, a Bell 103F modem, or by direct connection to the optional internal 202C-compatible modem. (The cable used to interface the Bell 202D and 103F modems is the same as the Auto Answer cable for the Bell 202C and 103A modems.) If the control PROM bit is set to select the polling mode, the line discipline program goes from state LIN1 to LIN3 and switches on DTR to enable the modem. The terminal must be switched ON-LINE at all times when the terminal is required to respond to polling.

   In state LIN3 the polling program monitors all received characters but inhibits all other line programs from functioning so that no communication may occur. With the terminal in this state, other terminals connected to the

multidrop communications line may transmit and receive data without affecting the terminal. When an end of transmission (EOT) character is received, the polling program goes to state LIN4.

State LIN4 is used to decode the station ID character. Any number of additional EOT characters may be received and the polling program will remain in LIN4. If the first non-EOT character received is not the station ID character selected by the seven pencil switches on the Expansion PC card (see Figure 3-1.4), the polling program returns to state LIN3 to wait for the next polling sequence. If the character is the station ID character, the polling program goes to state LIN5 and triggers the answer-back memory program if such control PROM bit option is selected.

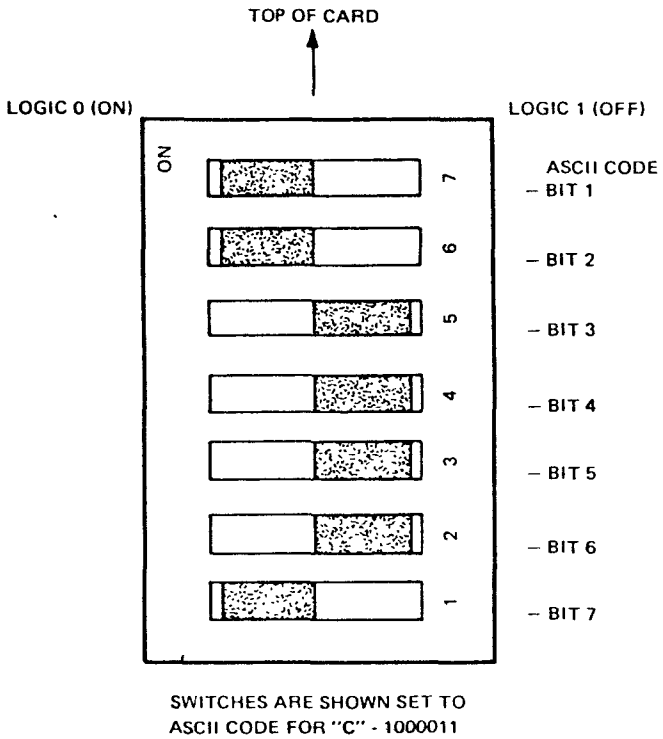


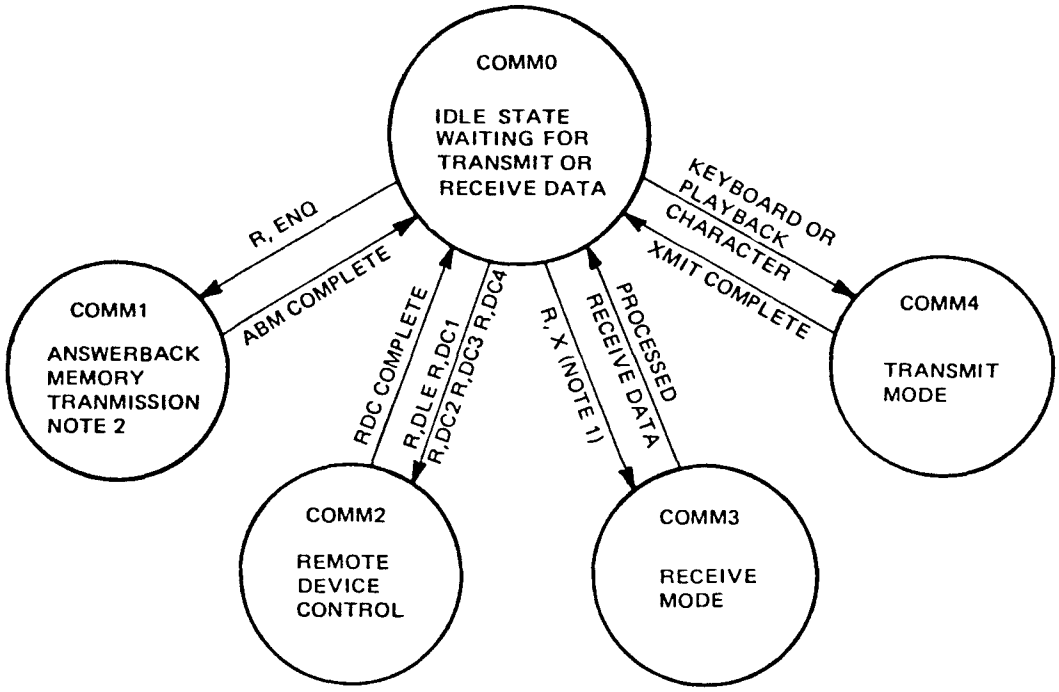
FIGURE 3-1.4. EXPANSION PC CARD PENCIL SWITCHES FOR SETTING STATION ID

In state LIN5 the terminal may transmit and receive data and may be controlled by remote device control (RDC) commands. The computer may request the status of the terminal by sending a DLE character followed by a < character. The terminal will enter the transmit mode and send an ASCII character in which each bit corresponds to a particular terminal status. This will be a single character if the LINE PROTOCOL switch is set to the nonblocked position but will be a transmission block (STX-status-ETB-LRC) if the switch is set for blocked communication. The computer can determine from this character whether or not the playback and/or record functions are on-line and ready.

The polling program remains in LIN5 until an EOT character is received while the terminal is not waiting to receive the completion of a data block or an acknowledge to a transmitted data block. The EOT character forces the polling program back to state LIN4 where it receives another polling sequence. The terminal may be polled any number of times in a sequence.

3-1.2.4 Communications Control. When a communications path has been established by the line discipline program, the communications control program is enabled, and data may be transferred to and from the computer. All communication is performed in half-duplex, as shown in the state diagram, Figure 3-1.5. In state COMM0 the terminal is idle and waiting for either a character received from the communication line or a character from the playback function or keyboard to force it into a new state.

a. Answer-Back Memory. The answer-back-memory (ABM) option may be selected by setting the appropriate control PROM bit. The ABM program transmits up to 21 user-specified ASCII characters to the communication line. The characters are programmed into the control PROM and are nonvolatile. The ABM characters are transmitted whenever the communication controller program is in state COMM0 and an ENQ character is received from the communications line. If the appropriate control PROM bit is set, the ABM characters are also



NOTES:

1. R,X INDICATES A RECEIVE CHARACTER OTHER THAN THOSE SPECIFIED ON OTHER EXIT PATHS.
2. THIS STATE MAY ALSO BE ENTERED WHEN A COMMUNICATION PATH IS FIRST ESTABLISHED.

FIGURE 3-1.5. COMMUNICATIONS CONTROLLER STATE DIAGRAM

transmitted when a communications path is first established. The characters may be printed and recorded if the FULL/HALF DUPLEX switch is set to the HALF DUPLEX position.

Remote Device Control. The remote device control (RDC) program allows the computer to control and manipulate the playback and record cassettes, switch the printer on and off, and request the status of the terminal. Four single character commands and thirteen double character commands are possible. The program normally decodes the characters, issues the indicated command within one character time, and then returns to state COMM0 ready to receive the next character. If the command initiates a long operation (such as load cassette 1) the RDC program does not wait for the operation to be completed.

If the commanded operation is a tape rewind and the specified cassette is on clear leader (EOT), all other terminal functions, including local, are locked out for 1.5 seconds to permit the tape to move past clear leader. This can be

avoided, except when necessary, by using the "request status" command to determine if the cassette is on clear leader. The parity of a remote control character must be even; if not, no function is performed.

- Single-Character Functions
  Playback On – DC1 (X–ON)
  Record On – DC2 (TAPE)
  Record Off – DC4 (TAPE)

- Two-Character Functions
  These functions are performed with the USASCII character DLE plus the following characters:

Rewind cassette 1	1
Rewind cassette 2	2
Load cassette 1	3
Load cassette 2	4
Cassette 1 in record mode	5
Cassette 2 in record mode	6
Block forward	7
Block reverse	8
Printer on	9
Printer off	0
Auto device control on	:
Auto device control off	;
Request status	<

  The printer is automatically disabled from printing the first character following the DLE character. If this character is not one of the above, the terminal will send an ENQ character.

- Status Character
  The status character is a USASCII character transmitted by the terminal when the *Request Status* code is received from the line. The specific status and bit location is as follows: Bit 1 (least significant bit) – indicates that the playback is ready when bit 1 is a logic ONE. If bit 1 is a logic zero, playback is not ready for one of the following reasons:

  - Cassette door open or cassette not in place
  - Cassette on clear leader
  - Playback not in LINE mode
  - Other operations being performed; i.e., rewind, and load.

  Bit 2 – indicates a playback error has been made if bit 2 is a logic ONE. A logic ZERO indicates a playback error has not been made.

NOTE
A playback error may be cleared using the remote control functions; playback on, block rev, or block forward.

Bit 3 – indicates cassette 1 is on the clear leader at either end of tape if bit 3 is a logic ONE. A logic ZERO indicates the cassette is not on clear leader.

Bit 4 – same as bit 3 except cassette 2 is affected.

Bit 5 – indicates that the record function is ready to be enabled with a record-on signal when bit 5 is a logic ONE. If bit 5 is a logic ZERO, record is not ready for one of the following reasons:

- Cassette door open or cassette not in place
- Cassette on clear leader
- Record not in LINE mode
- Other operation being performed; i.e., rewind and load
- Tape cassette write
- Tab removed.

Bit 6 – indicates that the printer is on-line when bit 6 is a logic ONE. If bit 6 is a logic ZERO, the printer is not in the LINE mode.

Bit 7 – always a logic ONE to force the status character out of the control character subset.

EXAMPLE: If cassette 1 is not on clear leader, cassette 2 is on clear leader, a playback error has not been made, the playback is ready, and printer is ready; then the status character would be:

b1 – 1
b2 – 0
b3 – 0
b4 – 1
b5 – 0
b6 – 1
b7 – 1 (strapped to logic ONE)

= USASCII character "i"

If the LINE PROTOCOL switch is set to the right or center position (nonblocked), the status character will be transmitted as a single character. If the LINE PROTOCOL switch is set to the left position (blocked), the status character will be transmitted as a communication block, i.e., the sequence: STX-status-ETB-LRC. This block requires an acknowledge the same as a normal data block.

c. Nonblocked communication. The terminal transmits and receives data in a Teletype (TTY) compatible, half-duplex mode when the LINE PROTOCOL switch is set to the right or center position.

- Receive Mode. Data received from the communication line is printed if the printer is ON-LINE and not disabled by the *Printer OFF* command, and recorded if the record cassette is on-line and switched on. RDC characters are detected and the appropriate function is performed. An ENQ character causes the ABM characters to be transmitted if the ABM option is installed. The EOT character causes termination of the communication line connection. The terminal is normally in the receive mode and enters the transmit mode through the modem-turnaround (MTA) program only when there is data to be transmitted.

- Transmit Mode – Keyboard Data. When a keyboard character is entered with the keyboard ON-LINE, the communication line is "turned around," and the character is transmitted. The communication line is then turned back around if another character is not ready, and the terminal goes back into the receive mode. This process is repeated for each character to be transmitted.

- Transmit Mode – Playback Data. When the playback cassette is switched on either manually or by the receipt of a DC1, the modem is turned around and the terminal enters the transmit mode. The playback characters are buffered in a 425-character section of processor memory in order to improve transmission efficiency. Once begun, transmission will continue until a DC3 character is played back, a playback error occurs, the cassette reaches clear leader, or the communications path is disconnected by the line discipline program. The terminal cannot receive a DC3 since it is in the transmit mode. A playback error causes transmission to stop, and the terminal goes back into the receive mode to await commands from the computer.

d. Modem-Turnaround. The modem-turnaround (MTA) function described below applies to both blocked and nonblocked communication. The sequence followed is shown in Figure 3-1.6.

- Receive-To-Transmit Mode. If the HI-SPEED switch is set to HI, indicating a 1200-baud half-duplex modem is being used, the program waits for the computer modem's carrier to be switched off before beginning the 10-millisecond delay. If the switch is set to LO, a 300-baud full-duplex modem is being used and the carrier remains on at all times. Once RTS is switched ON, a 202C-compatible modem will delay about 180 milliseconds before switching on EIA clear-to-send (CTS), while a 103A-type modem holds CTS on all the time so there is no delay.

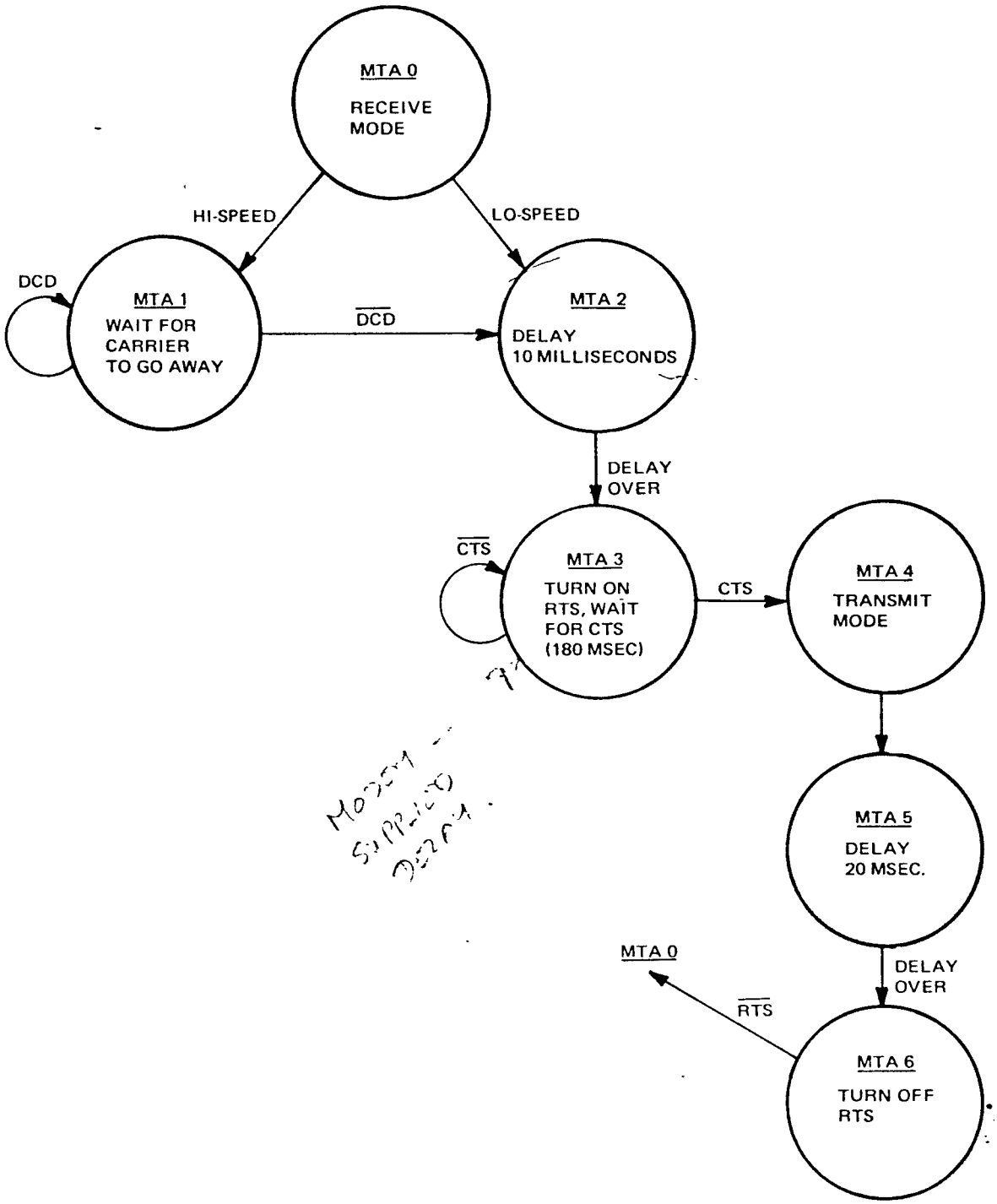


FIGURE 3-1.6. MODEM TURNAROUND (MTA) STATE DIAGRAM

- Transmit-To-Receive Mode. After the last character to be transmitted has been sent, the program delays 20 milliseconds to permit the character to clear the computer's modem. Then RTS is switched OFF, and the terminal goes back to the receive mode.

e. Blocked Communication. When the LINE PROTOCOL switch is set to the left position, the terminal transmits and receives data in block form. A data block comprises 425 or fewer characters preceded by an STX character and followed by an ETB (or ETX) character and a longitudinal redundancy check (LRC) character. The LRC character of each block and the parity bit of each character are checked for transmission errors, and blocks in which errors are detected are retransmitted.

The blocked communication controller performs the following functions:

- Groups the data from the keyboard or playback function into transmission blocks
- Inserts control characters related to each transmission block
- Retransmits blocks received at the calling station with an error
- Acknowledges blocks received with or without an error
- Interprets characters received as data to be recorded or printed or as acknowledge or remote control characters
- Transmits a CAN block when a playback error is made.

The following control characters are used to control the flow of data between the terminal and the central station.

ACK (Affirmative acknowledge) – acknowledges receipt of an error-free transmission block

NAK (Negative acknowledge) – acknowledges receipt of a transmission block with an error

STX (start of text) – indicates start of a transmission block

ETB (end of transmission block) Character – The ETB character indicates the end of a transmission block (not end of transmission or text) and that the next character is the LRC character. The ETB character is automatically inserted in a transmission block by the communication control after each 425 data characters received from the keyboard or playback function. An ETB received from the keyboard or from the playback function before the 425th character causes the characters received before the ETB to be transmitted as a short transmission block.

ETX (end of text) Character. The ETX character indicates the end of a transmission block (always less than 425 characters), the end of data (text) to be transmitted and that the next character is the LRC character. ETX is received from the keyboard (entered on the keyboard) or from the playback (previously recorded on tape) and not automatically inserted by the communication control. It indicates to the blocked communication controller that the characters received before the ETX are the last characters of the text and thus are to be transmitted as a block with the ETX character in lieu of the ETB character.

CAN (cancel) – indicates that a playback data error has occurred and that the computer should send commands to remove the error status.

ENQ (enquiry) – indicates that the transmitting station did not receive an ACK, NAK, or DC3 after transmitting a data block and that the receiving station should retransmit the ACK or NAK.

f. Error Checking. The following error checking and correction procedures are provided by the terminal.

- Parity checking. The parity sense of each character in a transmission block is checked when received, and an error flag is set if parity is not even. The parity sense of the acknowledge, STX, and remote control characters is also checked.

- LRC (longitudinal redundancy check) Character. The LRC character is an 8-bit character used to verify "error-free" reception of data at the terminal and the calling station. It is generated by taking a binary sum independently (without a carry) on each of the 7 individual information bits (b_1 to b_7) and the parity bit (b_8) in the characters of each transmission block. The summation begins with, but does not include, the STX character and ends with, and includes, the ETB or ETX character. Since the LRC character may be any character in the USASCII code, the terminal takes no action because of the LRC character except to acknowledge (ACK or NAK) proper or improper reception of the transmission block.

g. Acknowledgement Procedure.

(1) Received Data – After receipt of the LRC character in a transmission block, the terminal prepares itself to transmit the acknowledgement character. An ACK character is transmitted immediately if the parity check and the LRC check of the received data is valid and the data is to be recorded. If the data is to be recorded and the terminating character is an ETX, an ACK is transmitted after the ETX is recorded. If the printer is on-line, an ACK is transmitted after the last character is printed and/or recorded. After the ACK character is transmitted, the terminal switches to the receive mode to accept the next transmission block or remote control character.

If the parity check or LRC check is not valid, the terminal transmits a NAK character and switches back to the receive mode to receive the retransmission of the block. This process continues until the block is received correctly, or the calling station sends an EOT to terminate communications. If an ENQ character is received by the terminal before an STX character has started the next data block, the terminal enters the transmit mode and retransmits its response (ACK or NAK) to the last data block.

(2) Transmitted Data – After each block is transmitted, the terminal switches to the receive mode to await receipt of the acknowledge from the calling station. If the acknowledge character received is ACK, the terminal switches back to the transmit mode and begins transmission of the next block. If the block just transmitted is the last block to be transmitted (i.e., playback was automatically switched off by an ETX character), the terminal remains in the received mode after the ACK is received. If the acknowledge character received is NAK, the terminal switches back to the transmit mode and begins retransmission of the previous block. This process continues until the ACK character is received or a DC3 is received to switch off playback and force the terminal into the receive mode. The terminal then accepts control characters or an EOT to force an automatic disconnect.

If the first character received after transmitting a data block is not an ACK, NAK, or DC3, or if no character is received within 10 seconds, the terminal enters the transmit mode and transmits an ENQ character. It then returns to the receive mode and repeats the above procedure, awaiting an acknowledge from the calling station. Only one ENQ is sent if no response is received from the calling station. An automatic disconnect is performed if an ACK, NAK, or DC3 is still not received.

h. Procedure For Playback Errors. The terminal transmits a CAN (cancel) block when a playback error has been made while reading a tape to be transmitted to the communication line. The following procedure is followed.

When a playback error has been made, the communication control transmits all error-free characters (received from the playback for that transmission block) as a short block, with ETB as the terminating character. After positive acknowledgement is received from the calling station, the terminal transmits a CAN block (STX-CAN-ETB-LRC) and switches to the receive mode. The terminal then waits for an acknowledge and the appropriate control characters from the calling station (i.e., to reread, skip, or transmit the block with the error). If the terminal is commanded to reread the block and an error is again made, the terminal again transmits a CAN block.

i. Receive Mode. Receipt of an STX while the communications controller is in idle state (COMM0) forces the terminal into the receive block mode, as shown in the receive mode state diagram, Figure 3-1.7. The terminal remains in this mode until a data block terminated with an ETX and a valid LRC character is received, or until communication is terminated. While in this mode, the terminal will not recognize RDC characters nor transmit answer-back-memory upon receipt of an ENQ. A data block may contain any ASCII character other than an ETB or ETX, and no control function will be performed.

A typical receive data block causes the communications control program to complete the following state sequence:

RCV3-RCV4-RCV7-RCV9-RCV10-RCV11-RCV3.

If more than 425 characters are received before an ETB or ETX, the program waits in RCV5 until an ETB, ETX, or ENQ is received and responds with a NAK. If a valid data block is received when the PRINTER switch is not in the LINE position and an ETB terminates the block, an ACK will be transmitted immediately, and the block will be recorded while a new block is being received. Receiving an ETB or ETX while in RCV11 causes transmission of a NAK. Receiving an ENQ while in RCV11 causes the last ACK or NAK to be retransmitted. Manually switching on playback or pressing a keyboard key while the controller is in RCV11 will cause it to go into the transmit mode state XMT1.

j. Transmit Mode. If the processor receives a keyboard or playback character while the communications controller is in state COMM0 or RCV11, the program changes to state XMT1 where it checks the character and the line protocol switch to determine the type of transmission. With the switch set to blocked mode, any playback character or an STX from the keyboard will force the program into XMT3 after going through the modem turnaround (MTA) states and transmitting an STX character. This is shown in the transmit mode state diagram, Figure 3-1.8. Note that if the terminal is transmitting from the keyboard, an STX character must be entered at the beginning of each new block.

A normal 425-character block transmission causes the program to go through XMT3, XMT4, XMT5, and XMT6 as shown in Figure 3-1.8. Receipt of an ACK in XMT6 causes the program to retreat through state COMM0 and repeat the above sequence. If a NAK is received, the controller goes through states XMT8, XMT4, XMT5, and XMT6 to retransmit the data block.

If the keyboard or playback sends the processor an ETB or ETX, the character is transmitted and the controller skips state XMT4. Receipt of a NAK response to this short block causes XMT4 to be skipped in the retransmission.

(1) Keyboard Transmission. With the terminal idle in state COMM0, control characters (i.e., any character not in a

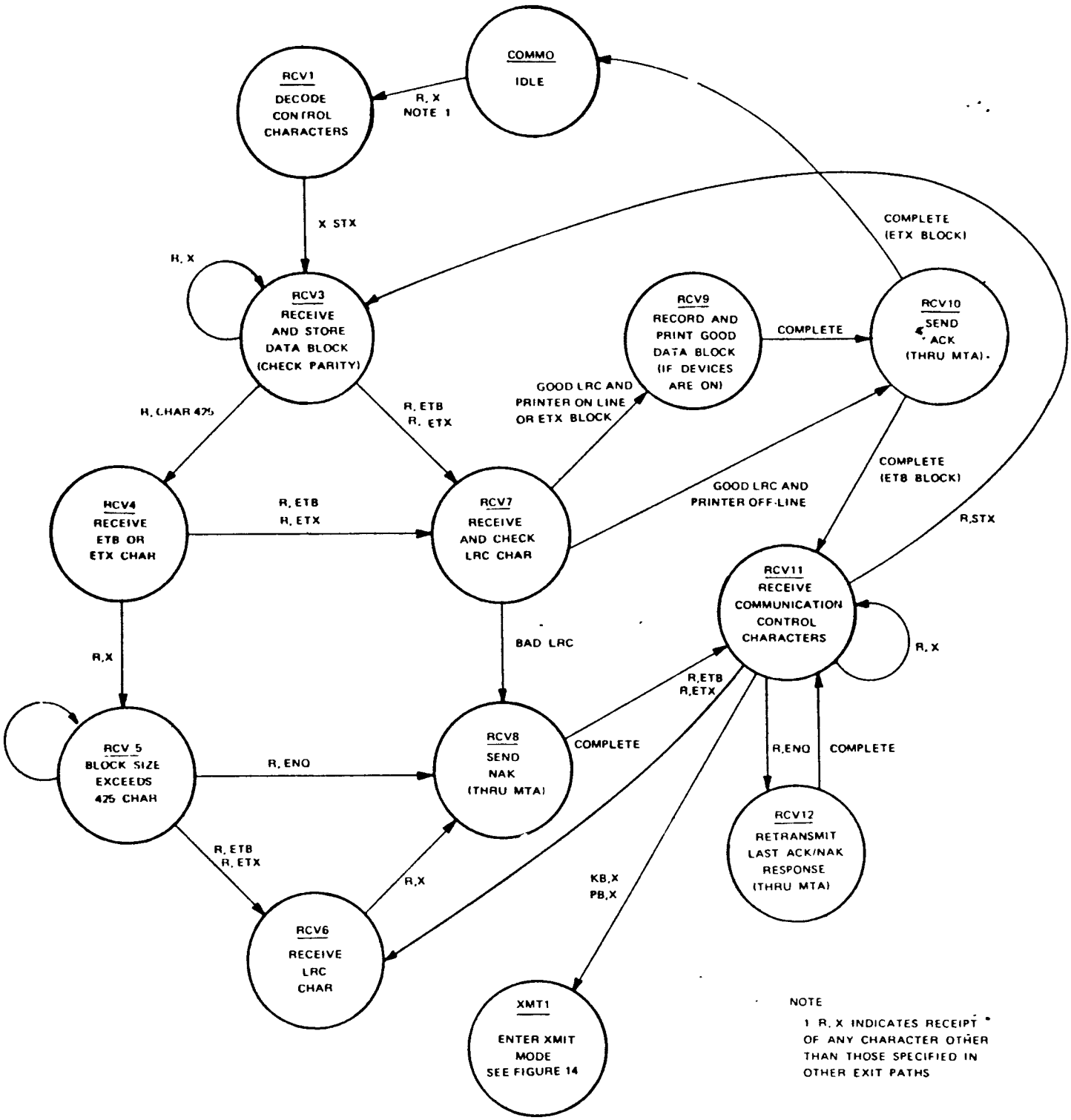


FIGURE 2-1.7. BLOCKED COMMUNICATIONS CONTROLLER RECEIVE-MODE STATE DIAGRAM

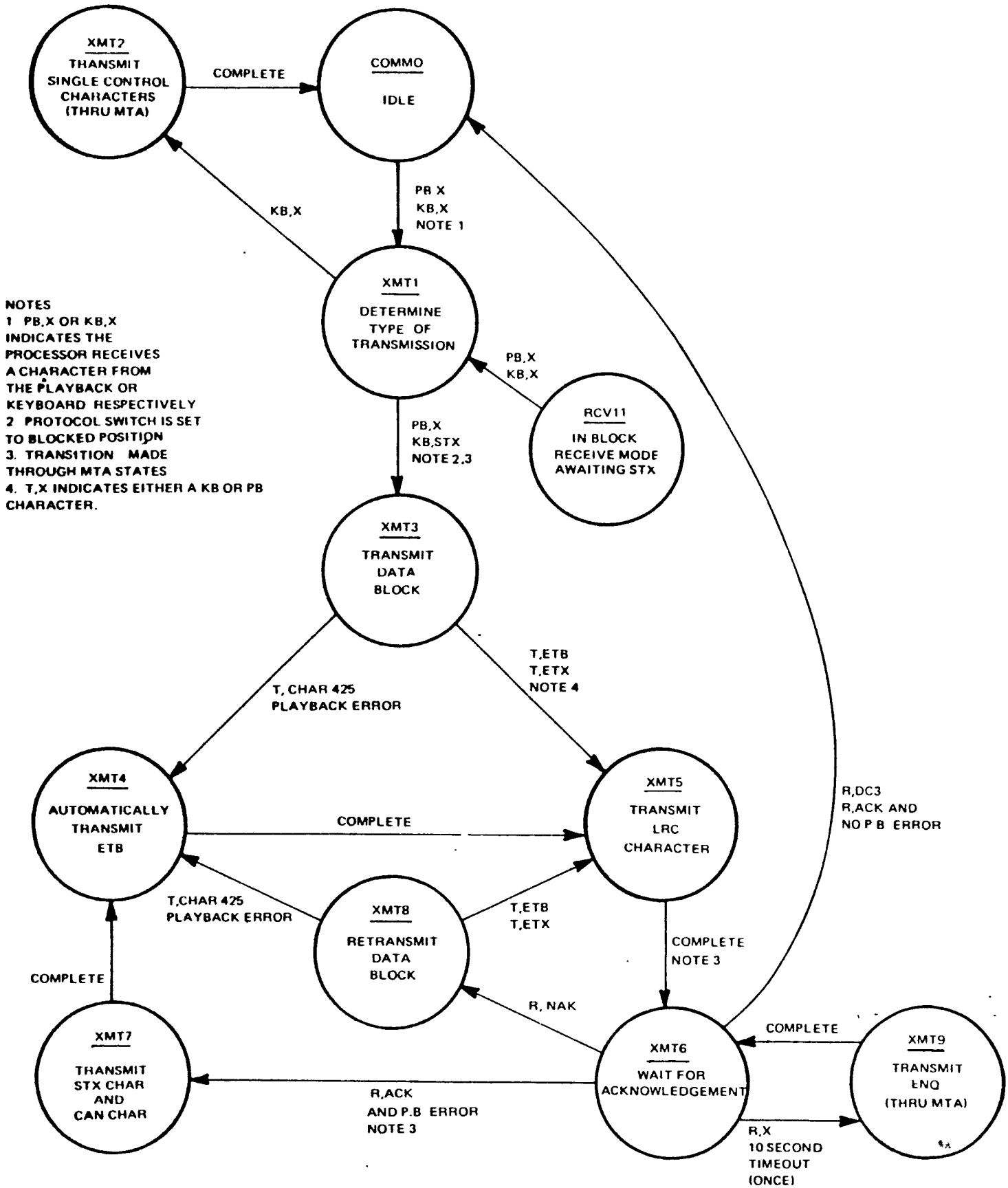


FIGURE 3-1.8. BLOCKED COMMUNICATIONS CONTROLLER TRANSMIT-MODE STATE DIAGRAM

data block) may be transmitted by pressing keyboard keys. These characters will not be printed. To enter the block transmit mode, an STX must be entered. The terminal enters the transmit mode immediately and sends the STX character. Each character entered from the keyboard after the STX is printed (unless the printer is switched off or remotely disabled) and transmitted. After typing the 425th data character the ETB and LRC characters are automatically transmitted and the acknowledgement procedure is followed. To begin the next block another STX must be entered. If less than 425 characters are to be sent, an ETB or ETX may be entered on the keyboard to terminate the block.

(2) Playback Transmission. Manually switching on playback or receiving a DC1 while in COMM0 causes the controller to transmit automatically an STX and enter the block transmission mode. The controller will continue to transmit data blocks from the playback tape until an ETX is played back (switches off playback) or a DC3 is received as the acknowledgement for a transmitted block (also switches off playback). Playing back an ETB causes a short block to be transmitted, but block transmission will continue since the playback is still on. Playing back a DC3 in this mode has no effect. Turning off playback manually in the middle of a transmission block causes the controller to enter the keyboard mode.

(3) Playback Errors. When a playback error occurs while transmitting a block, the controller automatically terminates the block with an ETB and LRC, and the normal acknowledgement procedure is followed. The next block sent, however, will consist only of STX-CAN-ETB-LRC. The cancel character is used to indicate to the computer that a playback error has occurred. The computer must send an acknowledgement, followed by remote device control characters, to force the terminal out of the error mode. If an attempt is to be made to reread the block, a block reverse command followed by a 1-second delay and a DC1 (playback on) command must be sent to the terminal. If the playback error occurs again, another CAN block will be sent. The block containing the error may be skipped and transmission continued with the next block by sending the terminal a block-forward command following the ACK. The invalid data in the block containing the error will be sent as the first part of a new transmission block if a playback-on command is sent to the terminal after the ACK.

3-2 HARDWARE SYSTEM ARCHITECTURE.

The Model 742 Programmable Data Terminal architecture is arranged around a single, serial data bus, a concept illustrated in Figure 3-2.1. The data bus is time-shared both by a line loop and a local loop within the terminal and by the devices within each loop through the processor. Which devices may use the serial data bus, and during what times, are decided by the terminal control function in conjunction with the processor. All data flows through the processor with two exceptions: (1) the status character from the tape cassette (upper unit) is received by the terminal control, and (2) the recorder print buffer function is not monitored by the processor.

The processor isolates the device sending the data from the device(s) receiving the data on both the line loop and the local loop. The processor separates the local loop and the line loop by the two input buffers (local buffer and line buffer). Terminal control generates two separate *enable-to-receive* signals (DATALOC and DATALINE), which enable the processor to determine the source of the data. Each data character placed on the data bus (with the two exceptions previously noted) is analyzed by the processor for appropriate action, depending on the firmware system in operation. Action by the processor includes:

(1) Certain communication disciplines

(2) Special operations (automatic search, remote device control, answer-back memory, etc.)

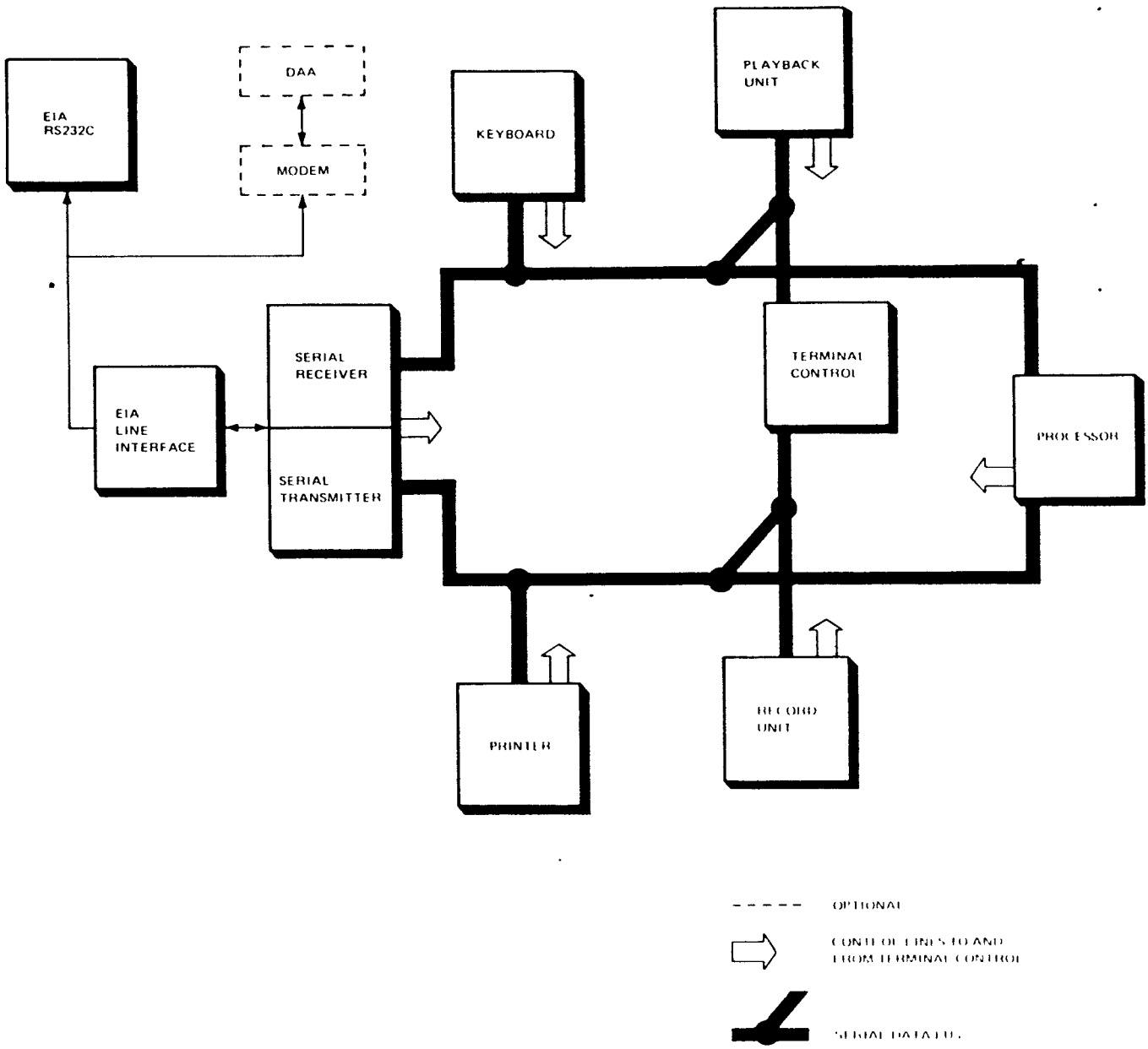


FIGURE 3-2.1. MODEL 742 PROGRAMMABLE DATA TERMINAL SYSTEM ARCHITECTURE

(3) Tape cassette control lines

(4) Remote-off control lines of the devices on both loops

(5) A control line to indicate on which loop the processor is operating.

The processor has one output buffer which is isolated from the input buffers and can output to either loop at different times. The operation of each loop is essentially simultaneous and independent because:

- the high rate at which data is transferred within the terminal on the data bus
- the separate local and line buffers on the processor card
- the comparatively slow rate at which devices (other than processor) on the data bus can react once they receive the data.

Since the terminal control can provide enables to the line and local loops and the processor can handle the data much faster than the loops require, both loops experience negligible delays.

better understanding of the terminal control and processor will yield easier comprehension of the system architecture. Figure 3-2.2 shows the timing for terminal control to accept requests from each transmitting device.

The terminal control and processor also monitor the status of each device on the data bus; i.e., whether the device is on-line, local, off, busy, etc. If more than one device has requested to transmit on the serial data bus, the terminal control must decide which device has the highest priority (see priority order in Figure 3-2.3), whether that device is on-line or local, and if the line loop or local loop is busy. For example, if the highest priority device requesting to transmit to the serial data bus is in local and the local loop is not busy, the terminal control will enable the transmitting device (i.e., keyboard) and the processor local buffer to the data bus and the data on it during an enable time frame. The local loop will then go busy for some time, and the terminal control may then act upon any request it may have from a line device (if the line loop is not busy).

Figure 3-2.4 shows a typical timing sequence when two devices simultaneously request the data bus. Figures 3-2.5 through 3-2.7 show some of the signals and data paths involved when the terminal control and processor interface with the various devices on the serial data bus.

3-3 FIRMWARE SYSTEM.

The firmware of the Model 742 is contained in 8192 words (8 bits per word) of read-only memory (ROM). This requires four ROM devices, each containing 2048 words. The lower 4k words (addresses 0 through 4095) are located on the processor PC card, and the upper 4k words are located on the Expansion PC card. A map of the firmware programs contained in the ROM is shown in Table 3-3.1.

The firmware programs utilize 2048 words of read/write memory RAM for pointers, flags, data storage, and format program storage. The lower 1k of RAM (addresses 10240 through 11264) is located on the Processor PC card, and the upper 1k is located on the Expansion PC card. A map of the various uses of the RAM is shown in Table 3-3.2.

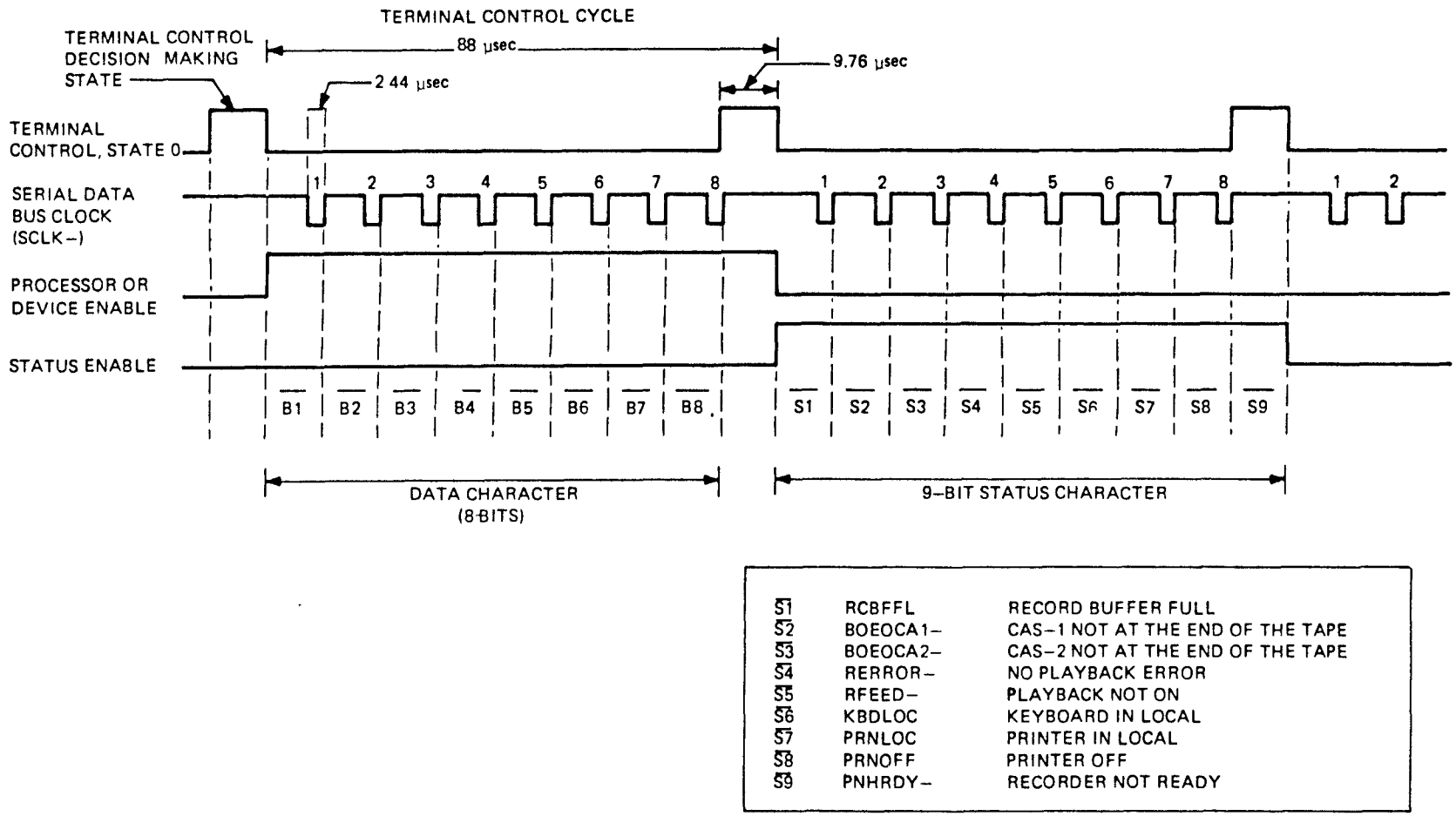
The firmware programs also utilize 32 words of programmable ROM for storage of customer-specified information. This includes flags which select various optional program functions, ASCII characters used to perform playback on/off and record on/off functions, and 21 characters of answer-back memory storage. This control PROM is located on the Processor PC card.

3-3.1 SUPERVISOR POINTERS. The Model 742 operating system consists of four state pointers and two jump pointers which control the system flow shown in Figure 3-3.1. The six supervisor pointers consist of:

(1) Local state pointer (LOCSP) – controls local program operation

(2) Line state pointer (LINSP) – controls line discipline and data transfer program operation

(3) Communication state pointer (COMSP) – controls data communication (reception and transmission) program operation



$\overline{S1}$	RCBFFL	RECORD BUFFER FULL
$\overline{S2}$	BOEOCA1–	CAS–1 NOT AT THE END OF THE TAPE
$\overline{S3}$	BOEOCA2–	CAS–2 NOT AT THE END OF THE TAPE
$\overline{S4}$	RERROR–	NO PLAYBACK ERROR
$\overline{S5}$	RFEED–	PLAYBACK NOT ON
$\overline{S6}$	KBDLOC	KEYBOARD IN LOCAL
$\overline{S7}$	PRNLOC	PRINTER IN LOCAL
$\overline{S8}$	PRNOFF	PRINTER OFF
$\overline{S9}$	PNHRDY–	RECORDER NOT READY

FIGURE 3-2.2. DATA TERMINAL SERIAL DATA BUS TIMING DIAGRAM

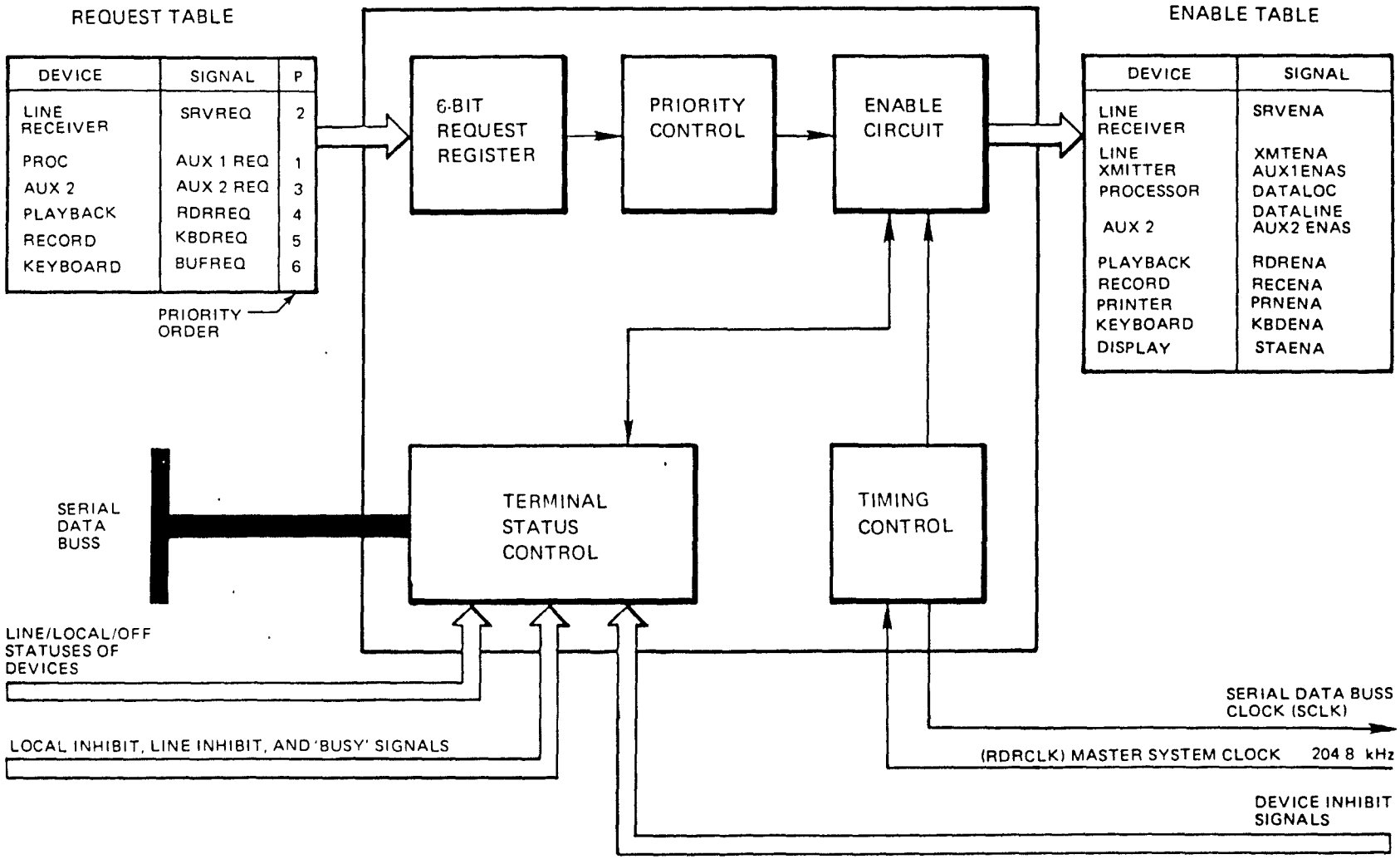


FIGURE 3-2.3. TERMINAL CONTROL BLOCK DIAGRAM

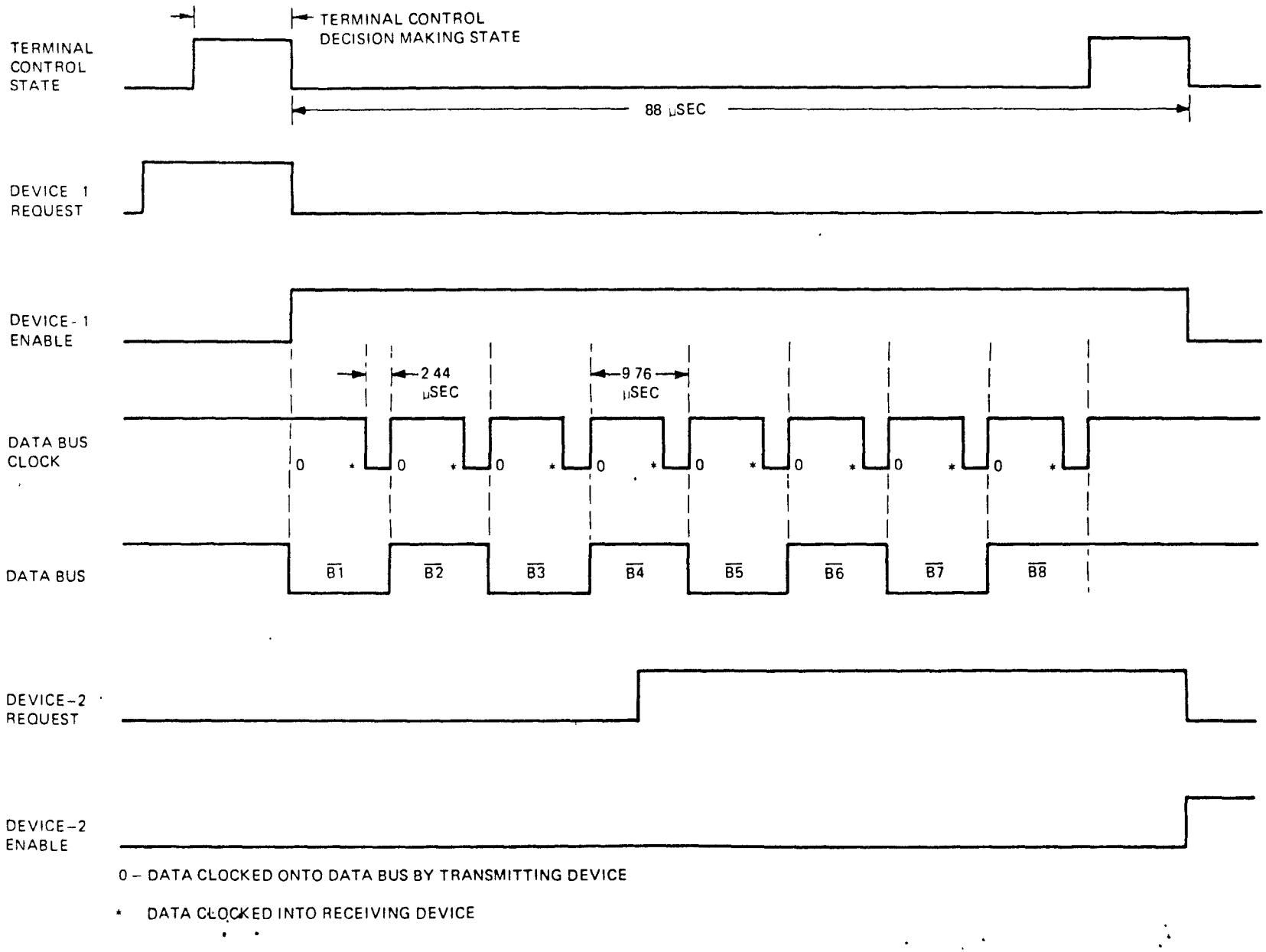


FIGURE 3-2.4. TIMING DIAGRAM, TYPICAL DATA TRANSMISSION VIA DATA BUS

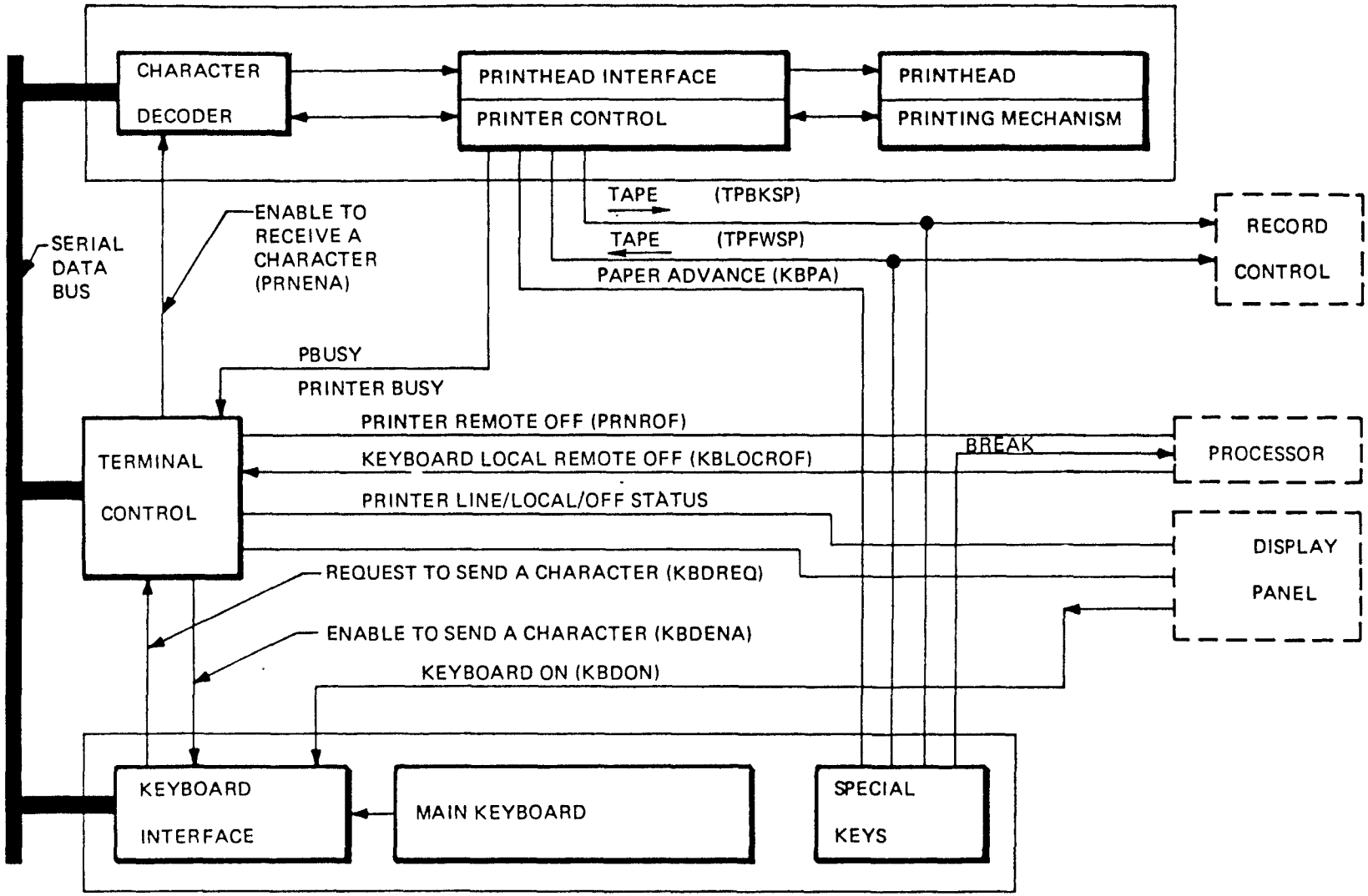


FIGURE 3-2.5. TERMINAL CONTROL, PRINTER, AND KEYBOARD BLOCK DIAGRAM

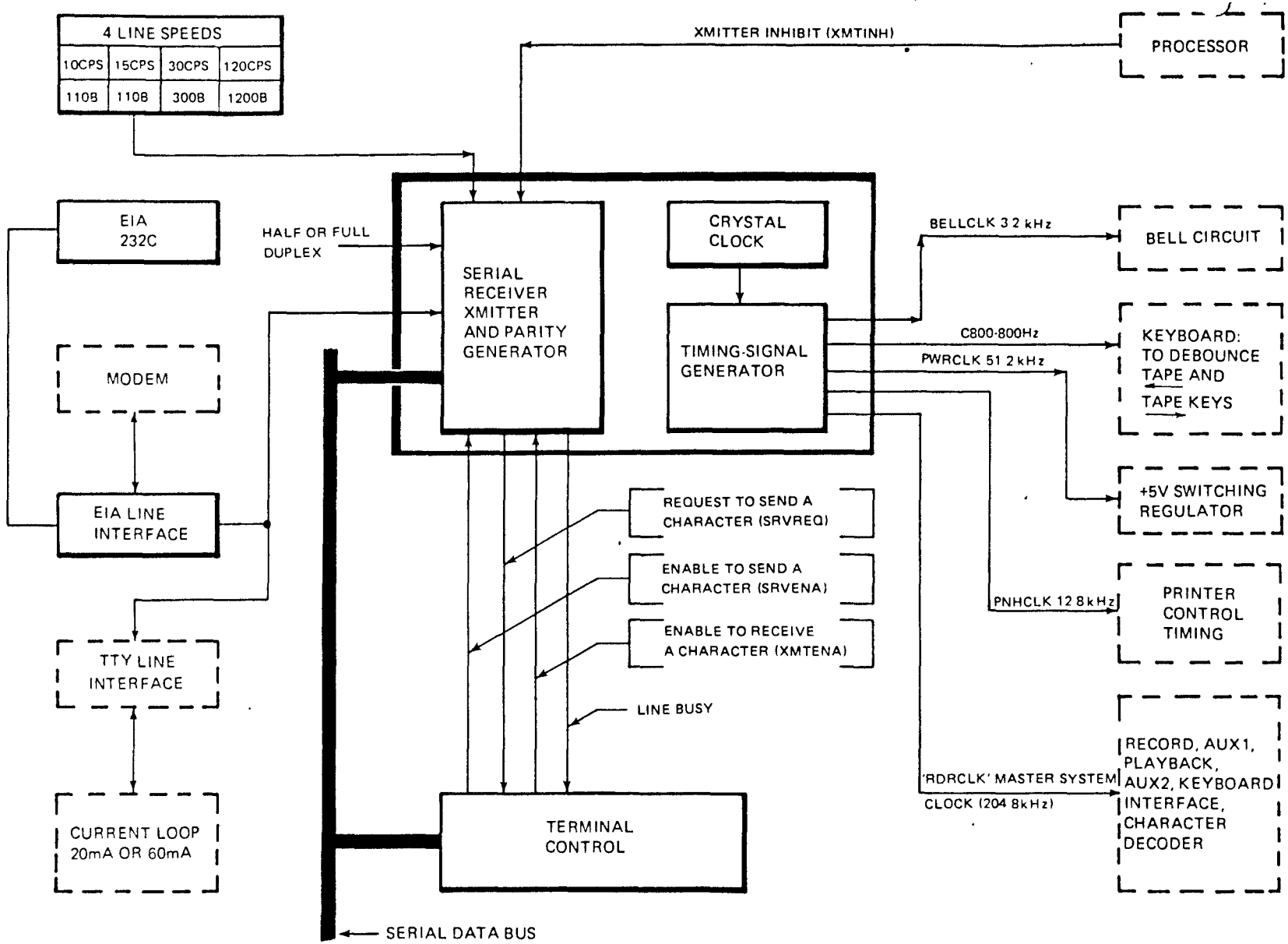


FIGURE 3-2.6. TERMINAL CONTROL, RECEIVER, TRANSMITTER, AND LINE INTERFACE (UP TO 300 BAUD)

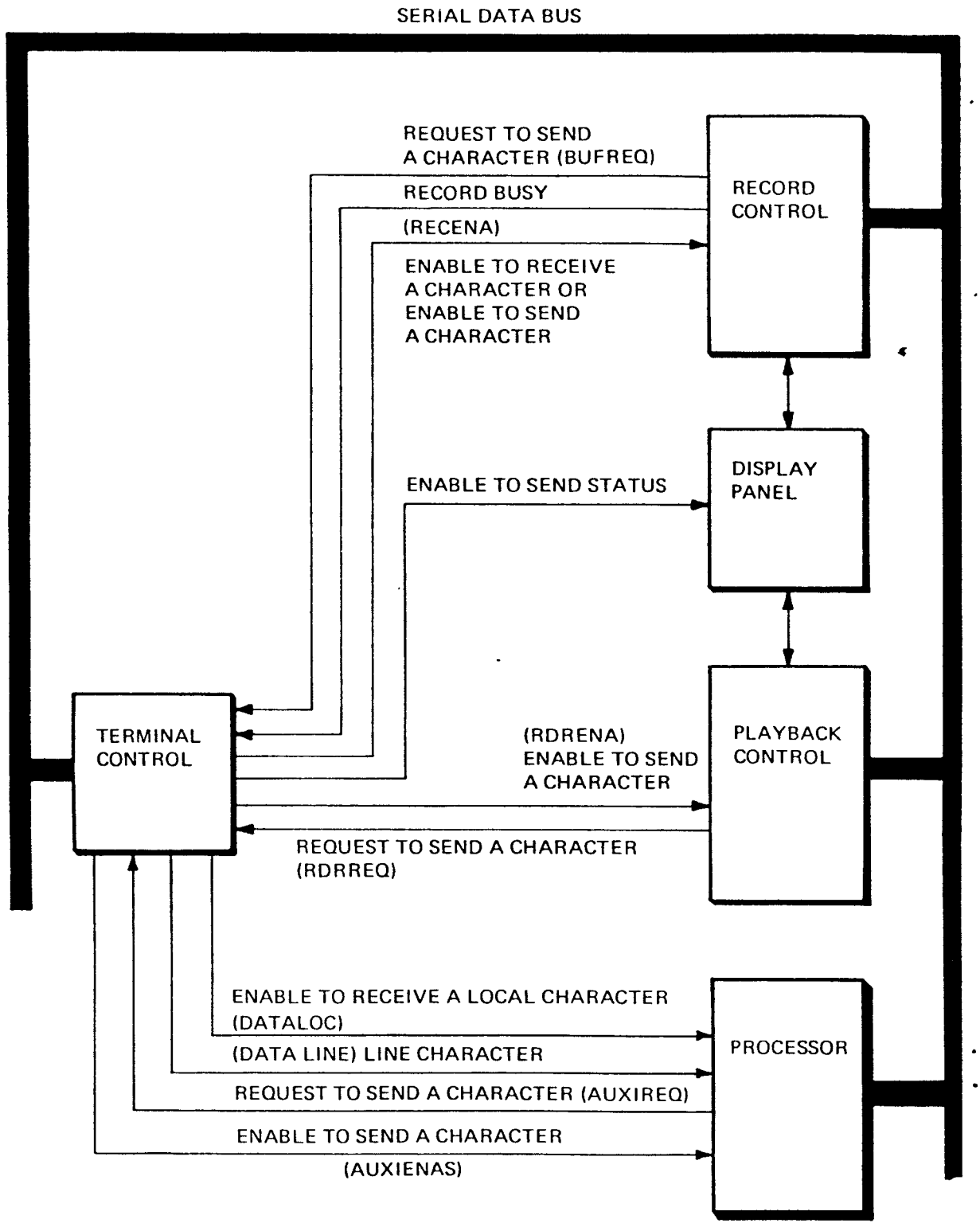


FIGURE 3-2.7. TERMINAL CONTROL, PLAYBACK, RECORD, AND DISPLAY PANEL

TABLE 3-3.1. READ-ONLY MEMORY (ROM) PROGRAM MAP

Start Address	Size	Function
0000 OCTAL	582	Common Subroutines
0582 1106_8	210	Local States 1 and 2
0792 1430_8	83	Search Program
0875 1553_8	126	Octal Loader
1001 1751	91	Break Detect Program
1092 2104	101	Power-Up Program
1193 2251	157	Transfer Program
1350 2506	759	Format Loader
2109 4055	4035	Format Program Interpreter
6144 14000	419	Line Discipline Program
6563	252	Modem Turnaround Program
6815	1339	Communications Controller
8154	38	Subroutines
58		
8192		

TABLE 3-3.2. RANDOM ACCESS MEMORY (RAM) MEMORY MAP

Start Address	Size	Function
10240	18	Supervisor Pointers
10258	3	Flags
10261	28	Local Counters
10289	87	Entry Buffer
10376	120	Registers
10496	24	Line Counters
10520	430	Communication Data Buffer
10950	1338	Format Program Storage
1288		
12288		

11K
12K

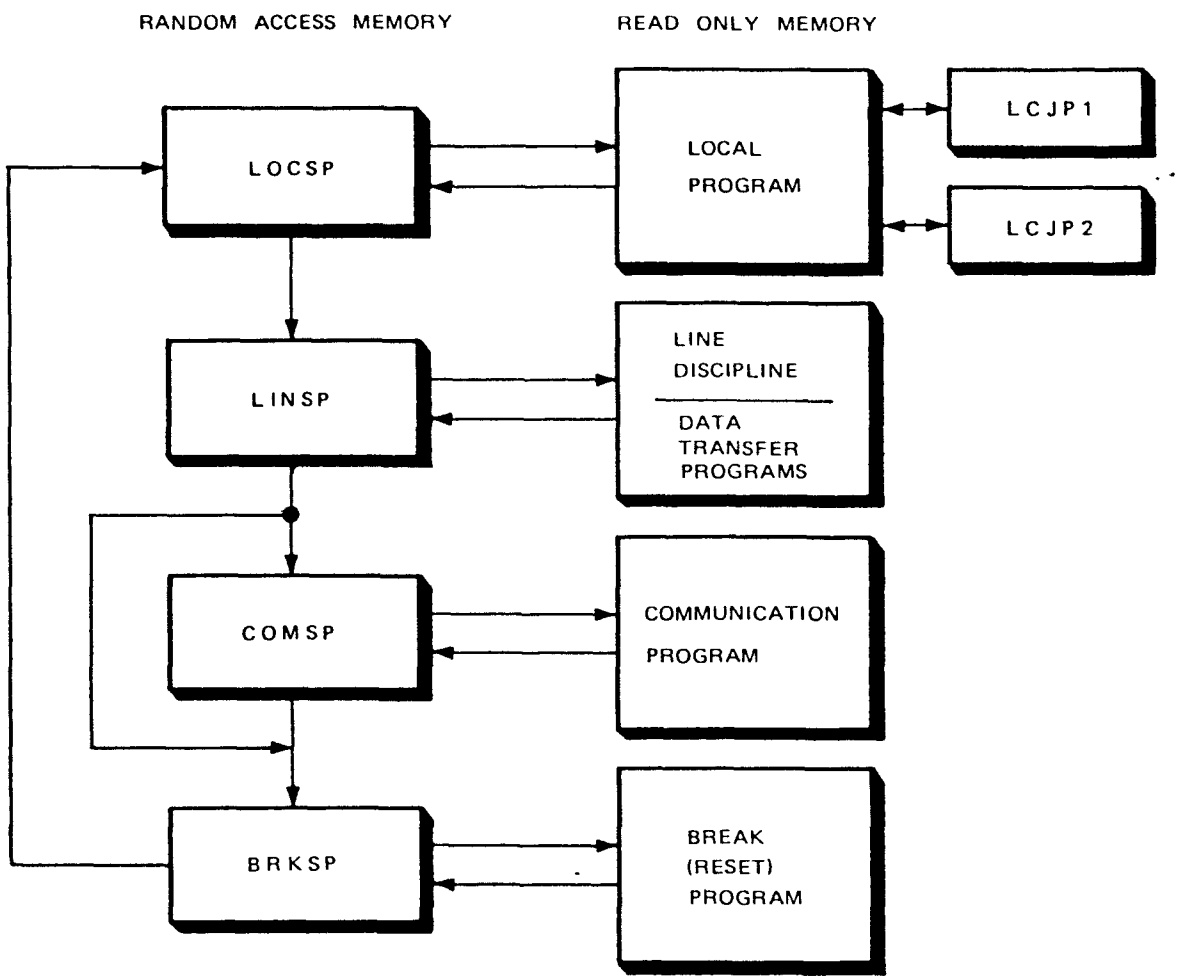


FIGURE 3-3.1. SUPERVISOR POINTER AND PROGRAM FLOW

(4) Break state pointer (BRKSP) – controls break (reset) program operation

(5) Local jump pointer I (LCJP1) – auxiliary pointer No. 1, used in local program operation

(6) Local jump pointer II (LCJP2) – auxiliary pointer No. 2, used in local program operation.

The supervisor pointers are actually call and jump instructions located in RAM which bring into execution specific programs (local, line, communication, and break) located in ROM. The ROM programs are subdivided into functional modules (states); each state pointer points to the entry address of the module to be executed. The state pointers, in turn, bring a module into execution for a specific period of time or until a certain function is completed, and then execution is passed to the next state pointer. This system of state pointer control is an efficient means to obtain a simultaneous line/local operating environment without the use of a complex interrupt scheme.

3-3.2 FLAG WORDS. The flag words consist of three words of RAM (24 bits) which communicate system status from module to module and from program to program. The three flag words are:

- Local flag (LOCFLG)

  Bit

  0 – Indicates if the search count has been reset (0 = no, 1 = yes)

  1 – Indicates if the search buffer is full (16th character input) (0 = no, 1 = yes)

  2 – Indicates data entry mode (0 = no, 1 = yes)

  3 – Indicates form abort disabled (0 = no, 1 = yes)

  4 to 7 – Spares

- Line Flag 1 (LINFLG)

  Bit

  0 – Indicates that an ETX has been transmitted in the blocked mode (0 = no, 1 = yes)

  1 – Indicates that an EOT has been received (0 = no, 1 = yes)

  2 – Indicates that the ADC has been disabled (0 = no, 1 = yes)

  3 – Indicates that an ETX has been received or a short block has been transmitted (0 = no, 1 = yes)

  4 – Indicates that a CAN has been transmitted (0 = no, 1 = yes)

  5 – Indicates that an ACK has been transmitted (0 = no, 1 = yes)

  6 – Indicates that the communications buffer is being dumped (0 = no, 1 = yes)

  7 – Indicates the terminal is in the transmit mode (0 = no, 1 = yes)

- Line flag 2 (LNFLG2)

  0 – Indicates full modem turnaround (0 = no, 1 = yes)

  1 – Indicates that a keyboard or ABM character is to be transmitted (0 = no, 1 = yes)

  2 to 7 – Spares

3-3.3 LOCAL COUNTERS. The local counters consist of the following 28 words of RAM used as storage locations for the local program:

WORD		
1	TABS	table size
2	NRP_L	new record pointer L
3	NRP_H	new record pointer H
4	NFP_L	new field pointer L
5	NFP_H	new field pointer H
6	WFP_L	working form pointer L
7	WFP_H	working form pointer H
8	$CAL1_L$	call-level-1 L
9	$CAL1_H$	call-level-1 H
10	$CAL2_L$	call-level-2 L
11	$CAL2_H$	call-level-2 H
12	CAP	call pointer and flags
13	SP_L	scratch pointer L
14	SP_H	scratch pointer H
15	SOF	start-of-field pointer
16	SOS	start-of-subfield pointer
17	ENP	entry pointer
18	NOP	working pointer
19	SIF	start-of-input-field pointer
20	MXL	maximum size storage
21	EF1L	entry flags 1
22	ENA	storage A
23	ENB	storage B
24	ENC	storage C
25	END	storage D
26	ENE	storage E
27	FIL	filler storage
28	PSH	printer storage

3-3.4 LINE COUNTERS. The line counters consist of the following 24 words of RAM used as storage locations for the line and communication programs.

WORD

1 PT1L – pointer-1 lower address

2 PT1H – pointer-2 upper address

A two-word buffer used to address a specific location (PT1)

3 PT2L – pointer-2 lower address
4 PT2H – pointer-2 upper address
A two-word buffer used to address a specific location (PT2)
5 LRC – longitudinal redundancy character
6 SCHAR – reserved location where single characters to be transmitted are stored
7 COMRET – reserved location specifying the communication return state
8 SPARE
9 DLYCLK – delay clock
10 DLYCNT – delay count
A two-word buffer where the delay real-time clock value and the delay clock counter are stored.
11 TIMCLK – time-out clock
12 TIMCNT – time-out count
A two-word buffer where the time-out real-time clock value and the time-out clock count are stored.
13 ABML – ABM lower address
14 ABMH –ABM upper address
A two-word buffer used to address a specific location in ABM.
15 ABMCNT – ABM character count
16 LNRETL – line return lower address
17 LNRETH – line return upper address
A two-word buffer specifying the line return state address.
18 to 24 – SPARES

3-3.5 LINE DATA STORAGE. The data storage area is 430 words of RAM used for buffering line data (received and transmitted). The buffer size can be either 425 or 430 characters long by setting a control PROM bit.

3-3.6 FORMAT STORAGE. The format storage area is 1338 words of RAM used in the data entry mode. With extended memory the format storage area is 1792 words; in which case 454 words of line storage are used for format program storage.

3-3.7 FORMAT LANGUAGE INTERPRETER. The format language is designed around three segments of RAM memory: the entry buffer, the format memory, and the arithmetic registers.

3-3.7.1 Entry Buffer. The entry buffer occupies 86 locations in RAM for record entry. Several pointers related to the entry buffer are described below:

a. The Start-of-Field pointer shows where a field starts in the entry buffer. A field consists of the characters between the entry pointer and the start-of-field pointer. Upon entry into local state 6 (EXECUTE mode), the start-of-field pointer is initialized to the entry buffer starting address. The start-of-field pointer is advanced in the entry buffer to the entry pointer on new field and new-field-and-jump instructions. The start-of-field pointer is reinitialized to the entry buffer starting address on record, record-and-jump, and clear-entry-buffer instructions.

If the HOME key (CAN) is detected by the input routine, the start-of-field point is reinitialized to the entry buffer starting address.

b. The Start-of-Subfield pointer shows where a subfield starts in the entry buffer. A subfield consists of the characters between the entry pointer and the start-of-subfield pointer. Upon entry into local state 6 (EXECUTE mode), the start-of-subfield pointer is initialized to the entry buffer starting address (EBSA). The start-of-subfield pointer is advanced in the entry buffer to the entry pointer on new field, new-field-and-jump, and new subfield instructions. The start-of-subfield pointer is redefined at the start-of-field pointer on a clear field instruction. The start-of-subfield pointer is reinitialized to the EBSA on record, record-and-jump, and clear-entry buffer instructions.

If the HOME key (CAN) is detected by the input routine, the start-of-subfield pointer is reinitialized to the EBSA. If the RUBOUT key (DEL) is detected by the input routine, the start-of-subfield pointer is redefined at the start-of-field pointer.

c. The Entry Pointer shows where the next character will be entered into the entry buffer. Upon entry into local state 6 (EXECUTE mode), the entry pointer is initialized to the entry buffer starting address (EBSA). This pointer is used to define the number of characters in a record, field, or subfield. The entry pointer can be advanced in the entry buffer on input type-min/max size, input type-exact size, input subfield and compare, duplicate, right justify, move: register to

subfield, load subfield, load-and-print subfield, retrieve subfield, load random character, character forward, and block forward instructions. The entry pointer is redefined at the start-of-field pointer on a clear field instruction. The entry pointer is redefined at the start-of-subfield pointer on a clear subfield instruction. The entry pointer is reinitialized to the EBSA on record, record-and-jump, and clear entry buffer instructions.

If the HOME key (CAN) is detected by the input routine, the entry pointer is reinitialized to the EBSA. If the RUBOUT key (DEL) is detected by the input routine, the entry pointer is redefined at the start-of-field pointer.

3-3.7.2 Format Memory. Format memory is basically divided into two sections: program storage and a jump table. Format programs are loaded into program storage by local state 5 (format loader). The jump table contains a specific address defined by the VT directive to local state 5. The jump table is always the last page (256 words) in memory, either page 57 or 67 (depending on the 4k option). Format programs are loaded from lower memory up, while the jump table is loaded from upper memory down, assuming efficient use of ID's. The amount of memory reserved for the jump table is only dependent on the largest binary value ID used. A number of pointers are related to the format memory:

a. The New Record pointer defines where a record starts in format memory. Upon entry into local state 6 (EXECUTE mode), the new record pointer is initialized to the format memory starting address. The new record pointer is advanced to the form pointer on each record and record-and-jump instruction.

   If the HOME key (CAN) is detected by the input routine, the working form pointer and new field pointer are redefined to the new record pointer.

b. The New Field pointer defines where a field starts in format memory. Upon entry into local state 6 (EXECUTE mode), the new field pointer is initialized to the format memory starting address. The new field pointer is advanced to the form pointer on each record, record-and-jump, new field, and new-field-and-jump instruction.

   If the HOME key (CAN) is detected by the input routine, the new field pointer is redefined to the new record pointer. If the RUBOUT key (DEL) is detected by the input routine, the working form pointer is redefined to the new field pointer.

c. The working form pointer defines the location of the format program. It could be referred to as the program counter (PC). Upon entry into local state 6 (EXECUTE mode), the working form pointer is initialized to the format memory starting address. The working form pointer is used to retrieve all characters from format memory. The working form pointer increments through the program until a jump (refers to all instructions with ID's), call, or return instruction is encountered. An ID defines a location in the jump table where an address is stored. When the program is required to jump or call, the address in the jump table specified by the ID is forced into the working form pointer, and execution continues. In a return instruction an address is taken out of the call-level-ONE or call-level-TWO pointer and forced into the working form pointer and execution continues.

   If the HOME key (CAN) is detected by the input routine, the working form pointer is redefined to the new record pointer. If the RUBOUT key (DEL) is detected by the input routine, the working form pointer is redefined to the new field pointer.

d. The Call-Level-One pointer and Call-Level-Two pointer are used for the call and return instructions. Upon entry into local state 6 (EXECUTE mode), both call pointers are initialized to the format memory starting address. In a call instruction the working form pointer is forced into one of the call pointers (the level of call determines which pointer). In a return instruction, one of the call pointers (the level of return determines which pointer) is

forced into the working form pointer and operation continues.

3-3.7.3 Format Memory Flags. A number of flags are used by the format program:

- The Printer-On Flag is used to determine if the printer should be on or off during instruction execution. Upon entry into local state 6 (EXECUTE mode), this flag is a ONE. It is set to a ZERO upon a printer-off instruction, and set to a ONE upon a printer-on instruction or any print instruction.

- Auto Skip-On Flag is used to determine if the program should automatically continue to the next instruction if the input entries reach the maximum size specified in an input instruction. Upon entry into local state 6 (EXECUTE mode), this flag is set to a ZERO; thus, no auto-skip. This flag is set to ONE on an auto-skip-on instruction, and set to a ZERO on an auto-skip-off instruction.

- Free Form Flag is used to determine if the program should automatically fill an entry (up to the maximum size specified in the input instruction) with filler characters. Upon entry into local state 6 (EXECUTE mode), this flag is set to a ZERO; thus, free form. This flag is set to a ONE or fixed form in a fixed form instruction, and is reset to a ZERO in a free form instruction.

3-3.7.4 Arithmetic Registers. The arithmetic registers consists of seven working registers, two scratch registers. and a register called an accumulator. Each register is 12 locations long: 11 locations are reserved for numeric characters and one location is reserved for a sign character. The registers are used to save numeric data and perform arithmetic operations on numeric data previously saved.

3-3.7.5 Auxiliary Pointers or Storage Locations.

- Table size is a storage location used to store the amount of memory used by the jump table.

- Working pointer is an auxiliary pointer used to maneuver characters in and out of the entry buffer.

- State-of-input-field pointer is an auxiliary pointer used to specify the first character entered into the entry buffer on an input instruction.

- Filler storage contains the filler character, specified in the fixed form instruction.

- Printer storage is a storage location used to output characters to the local data bus.

3-3.8 CONTROL PROM BIT FUNCTIONS.

Word 0
Word 0 must be a 104_8. This is a jump instruction to the processor and is required for power up.

Word 1

Bit 1	H	=	standard power-up program used
	L	=	alternate power-up program used
Bit 2	H	=	standard local ESC commands enabled
	L	=	alternate ESC command program used
Bit 3	H	=	standard line discipline program enabled
	L	=	alternate line discipline program used
Bit 4	H	=	auto-answer line discipline
	L	=	multidrop line discipline
Bit 5	H	=	ABM triggered when communications connection is established
	L	=	ABM not triggered when communications connection is established
Bit 6	H	=	answer-back memory option enabled
	L	=	ABM option disabled
Bit 7	H	=	425-character communication data buffer
	L	=	430-character communication data buffer
Bit 8	H	=	standard delay when entering transmit mode
	L	=	no delay when entering transmit mode.

Word 2

Bit 1	H	=	reverse channel operation enabled
	L	=	reverse channel operation disabled

Bit 2 Unused

Bit 3 H = bit 6 of status character is RFEED
L = bit 6 of status character is a ONE

Bit 4 H = ACK not required after transmitting an ETX block
L = ACK required after transmitting an ETX block

Bits 5 to 8 Unused.

Word 3
Bit 1 H = 2k bytes of RAM
L = 4k bytes of RAM

Bit 2 H = 2k bytes of RAM
L = 4K bytes of RAM

Bit 3 H = standard format language operation codes
L = alternate format language operation codes

Bit 4 Unused.

Word 4
Unused.

Word 5
Word 5 is an ASCII character which causes a PLAYBACK-ON command when received over the communication line or is entered from the keyboard in local mode. Bit 1 is ASCII bit 1 (LSB); bit 7 is ASCII bit 7 (MSB); and bit 8 is a parity bit. Word 5 is normally a DC1 character.

Word 6
Word 6 is an ASCII character which causes a RECORD-ON command when received over the communication line, is played back in local mode, or is entered from the keyboard in local mode. Word 6 is normally a DC2 character.

Word 7
Word 7 is an ASCII character which causes a PLAYBACK-OFF command when played back in line or local mode. Word 7 is normally a DC3 character.

Word 8
Word 8 is an ASCII character which causes a RECORD-OFF command when received over the communications line, is played back in local mode, or is entered from the keyboard in local mode. Word 8 is normally a DC4 character.

Word 9
Word 9 is an ASCII character which causes a PLAYBACK OFF command when played back in local mode. Word 9 is normally an ETX character.

Word 10
Word 10 is the number of characters in answer-back memory. Bit 1 is LSB; bit 8 is MSB.

Word 11 through Word 31
These words are the answer-back memory character sequence. Word 11 is the first character transmitted. Bit 1 of each word is bit 1 of the ASCII code; Bit 7 of each word is bit 7 of the ASCII code. Bit 8 of each word is unused.

3-4 POWER SUPPLY.

The Model 742 power supply, diagrammed in Figure 3-4.1, provides voltages of 33V unregulated, +5V regulated, +12V regulated, -5.6V regulated, and -12V regulated to the terminal. A power reset is incorporated in the circuit to reset the terminal upon power up or power failure.

The Model 742 terminal has a standard 14-amp power supply. A detailed description of the power supply and its operation are contained in the 732/733 ASR/KSR Maintenance Manual (TI Manual No. 960129-9701).

3-5 PRINTER SYSTEM.

The printer consists of seven major parts:

- Paper drive mechanism
- Printer drivers
- Printer control logic
- Character decoding
- Printhead
- Printhead interface
- Printhead compensation circuit.

The printer drivers are located on the Regulator/Amplifier PC card (slot A10), the printer control logic on the Printer Control PC card (slot A2), the character decoding on the Printer Code PC card (slot A1), the printhead interface on the Printhead Interface PC card, and the printhead

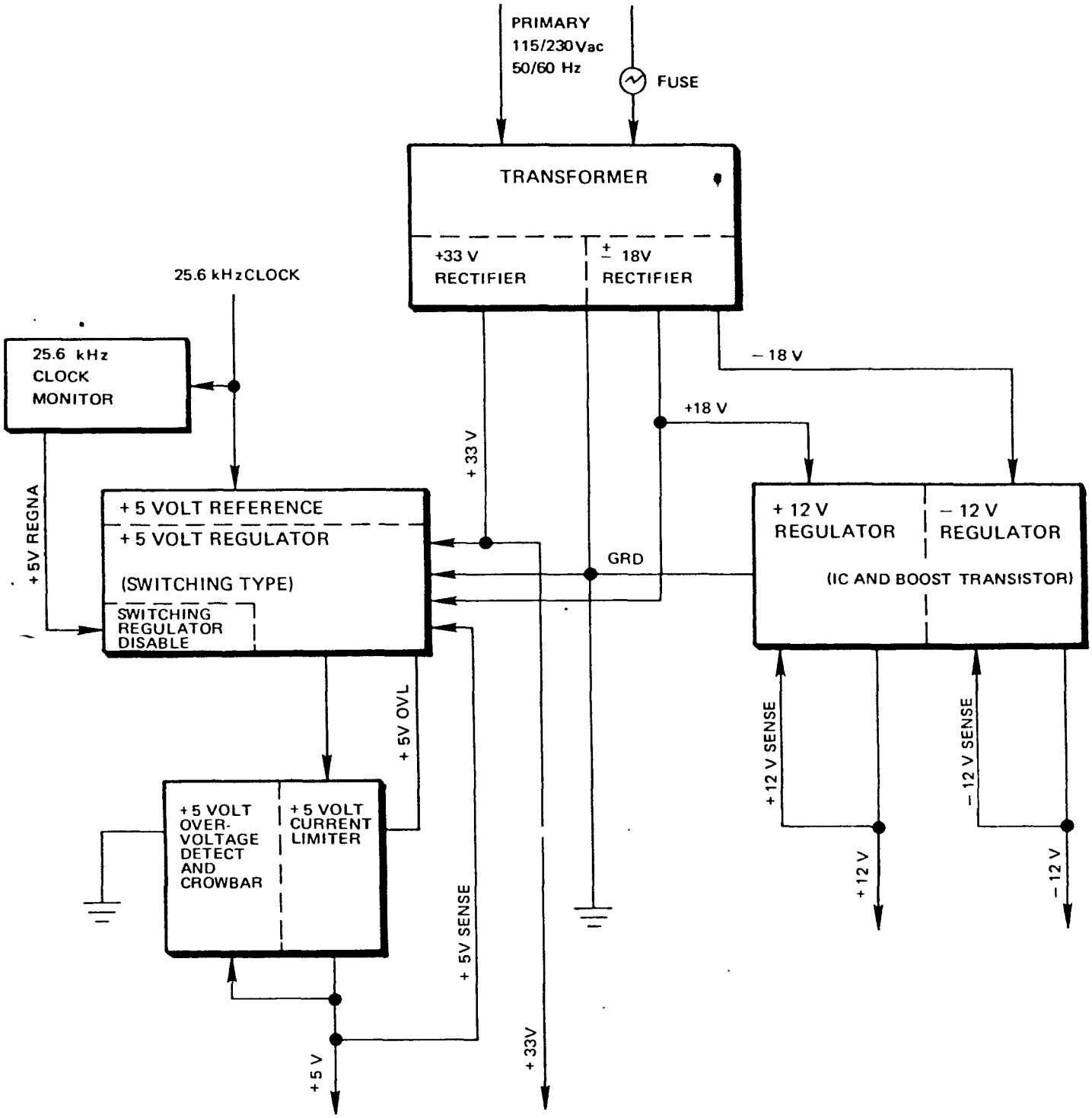


FIGURE 3-4.1. MODEL 742 DATA TERMINAL POWER SUPPLY BLOCK DIAGRAM

compensation circuit also on Printer Code PC card (slot A1). A block diagram of the printer system is shown in Figure 3-5.1. A detailed description of the printer system is ontained in the 732/733 ASR/KSR Maintenance Manual (TI Manual 960129-9701).

3-6 KEYBOARD AND KEYBOARD INTERFACE.

The Model 742 keyboard is a fully encoded, alphanumeric keyboard with two-key rollover. The interface for the keyboard is located on the Printer Code PC card. A block diagram of the keyboard interface is shown in Figure 3-6.1. A flow chart and a timing diagram are shown in Figures 3-6.2 and 3-6.3.

3-6.1 •KEYBOARD INTERFACE. Upon detection of a keyboard strobe, the parallel keyboard data is loaded into the data buffer, and the strobe flipflop is clocked. The keyboard interface then sends a keyboard request (KBDREQ) to terminal control and waits for a keyboard enable (KBDENA). Keyboard interface uses this enable and eight system clocks (SCLK) to transmit the character serially to the data bus. When this is done, the repeat key (REPEAT) is checked, and a flipflop is set to remember the state of the repeat key. The interface then checks for another strobe; if there is no strobe but the REPEAT key is depressed, another request will be generated and the same character will be retransmitted. This will continue until there is a strobe or until the REPEAT key is released. If the REPEAT key is pressed and a new keyboard strobe is received, the new character will be loaded into the data buffer, and it will then be transmitted as before. When there is no REPEAT key signal, only one character will be transmitted for each keyboard strobe (depression of a key).

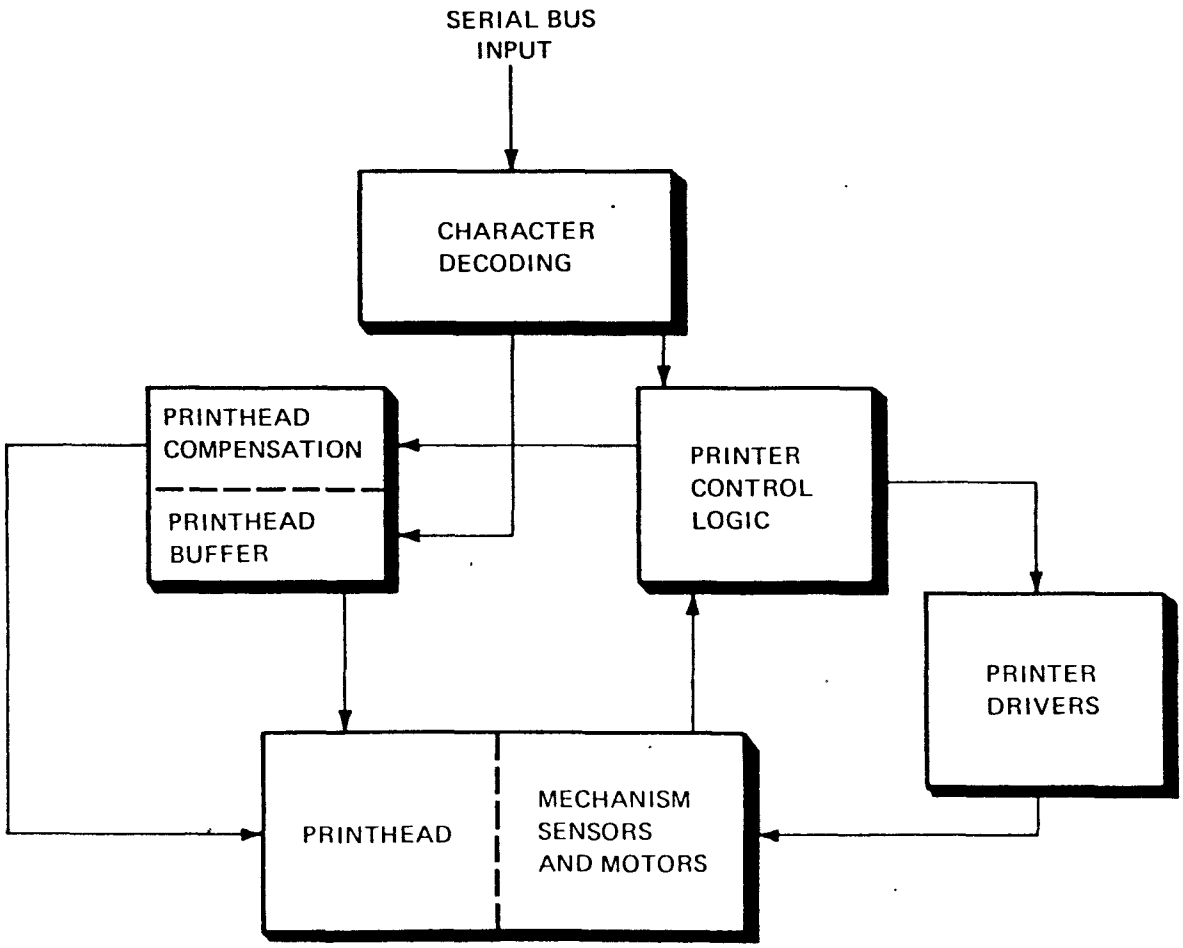


FIGURE 3-5.1. PRINTER SYSTEM BLOCK DIAGRAM

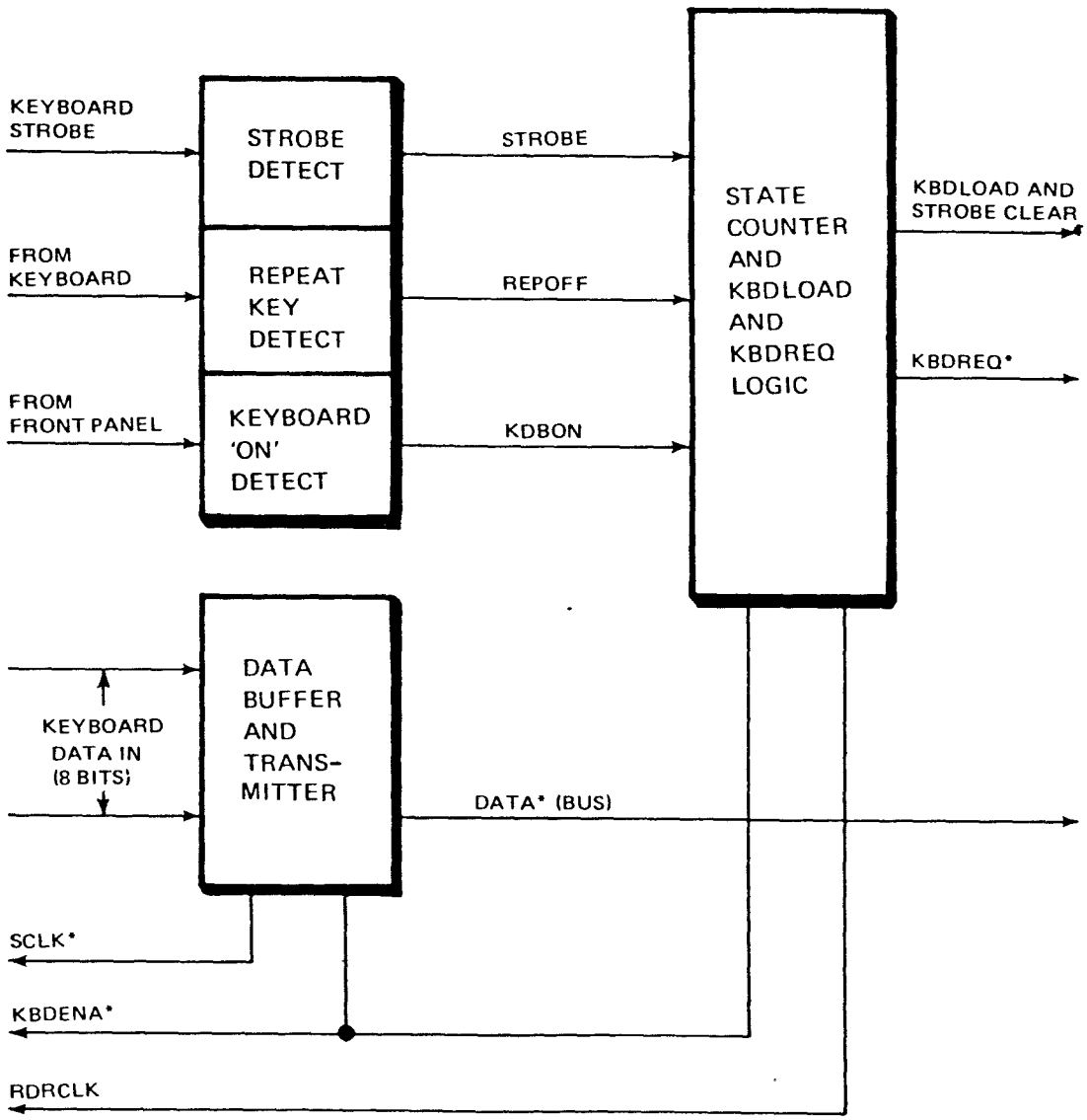


FIGURE 3 6.1. KEYBOARD INTERFACE BLOCK DIAGRAM

LINDAT (line data). For the print buffer function (BUFREQ), terminal control allows data to bypass the processor by issuing both a printer enable and a recorder enable.

When the processor makes a request (AUX1REQ), terminal control enables the processor to send (AUX1ENAS) and issues enables-to-receive to appropriate receiving devices. Devices issued enables-to-receive are those devices which are "ready" and in the same loop (line or local) as the processor as indicated by AUX1LOC.

Terminal control generates status enable whenever no requests are present, and a status enable has not been issued in the previous enable cycle (see section 3-8.3 below).

The priority structure of incoming requests is arranged as follows:

1. Auxiliary 1 (processor)
2. Serial receiver
3. Auxiliary 2
4. Playback
5. Recorder (print buffer function)
6. Keyboard.

Figure 3-8.1 shows a block diagram of terminal control. Each major function shown in the diagram is described below.

3-8.1 CLOCK GENERATION. The clock circuitry generates the timing signals used by terminal control and those clocks which transfer data within the terminal. All clocks are derived from the basic 204.8-kHz terminal clock (RDCLK). A timing diagram of the clock circuitry is shown in Figure 3-8.2. The signal SCLK is used for serial data transfer within the terminal. Sending devices put data onto the bus at the leading edge of SCLK while receiving devices capture data from the trailing edge.

3-8.2 REQUEST REGISTER. All requests are first latched upon receipt and moved synchronously to the request register with TCST1Q. A latched request is cleared when its respective enable-to-send is generated. All requests are cleared with PWRST upon applying power.

3-8.3 SERIAL STATUS REGISTER. Each time status enable. (STATENA) is generated, ASR status is placed on the serial data bus. Terminal control receives this status by enabling a serial receiver with STATENA and clocking the received data into its parallel status register with CK1–. The status comprises printer-off, printer local, keyboard lock, RFEED, recorder-on-line, reader-on-line, reader error, record-buffer-full, BOEOCA1, and BOEOCA2.

3-8.4 SIGNAL SYNCHRONIZATION. Control signals exercised by the processor are synchronized on terminal control with CK1–.

3-8.5 BUSY LOGIC. A combinational logic signal (BUSY) is generated to indicate the status of the line and local loops. The processor always checks that the particular loop to be used is not busy before issuing a request in that mode. If AUX1LOC– is a logical ZERO, BUSY reflects the status of the local loop. Likewise, a logical ONE corresponds to the line loop. The BUSY equation is

BUSY = TIMERBUSYQ + [AUX1LOC·(PBUSY·PRNLOC + RCBUFFL·RECLOC) + AUX1LOC–·(RCBUFFL·RECLOC–)]

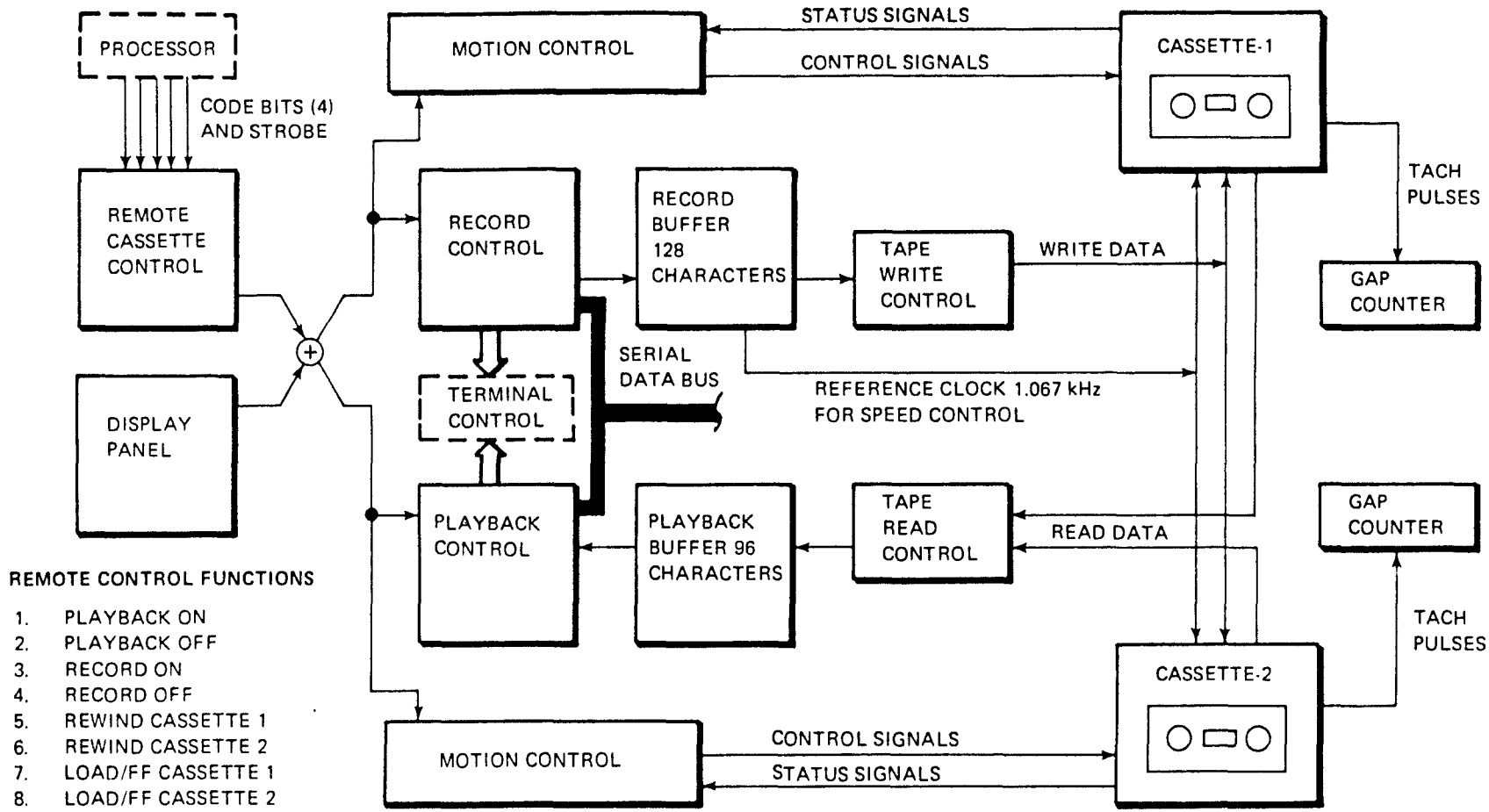
3-8.6 TERMINAL CONTROL CONTROLLER. An eight state, ROM-implemented, synchronous state controller is utilized in the terminal control design. A block diagram of the controller is shown in Figure 3-8.3.

Controller operation is illustrated in the flow charts in Appendix D.

3-8.6.1 Present ROM Address Register. This register contains the present ROM address (PRA) of the terminal, also known as the *state* of the terminal. The PRA is updated on the rising edge of each SCLK– with the next ROM address (NRA).

3-8.6.2 Decision Multiplexer. The decision multiplexer is an 8-to-1 device addressed by the PRA. Its inputs consist of all requests, device status, and control lines. As each state addresses the multiplexer, the appropriate signals required for decision making are routed to the ROM inputs.

3-8.6.3 Controller ROM. The ROM is addressed by the PRA, the outputs of the decision multiplexer, and SCLK. When SCLK is at a logic ONE, the ROM produces the NRA (see paragraph 3-8.6.1). When SCLK is at a logical ZERO, the ROM produces the appropriate enable-to-send and



REMOTE CONTROL FUNCTIONS

1. PLAYBACK ON
2. PLAYBACK OFF
3. RECORD ON
4. RECORD OFF
5. REWIND CASSETTE 1
6. REWIND CASSETTE 2
7. LOAD/FF CASSETTE 1
8. LOAD/FF CASSETTE 2
9. BLOCK FWD
10. BLOCK REV
11. CHARACTER FWD
12. CASSETTE 1 RECORD
13. CASSETTE 2 RECORD
14. CASSETTE 1 STOP
15. CASSETTE 2 STOP

FIGURE 3-9.1. CASSETTE SUBSYSTEM BLOCK DIAGRAM

3-10 1KX8 PROCESSOR PC CARD.

All data flow in the Model 742 is funnelled through the Processor PC card as shown in Figure 3-10.1. The keyboard, playback, and serial receiver send data only to the Processor PC card. This data is analyzed by the processor which then sends the data to the appropriate receiving device; i.e., printer, recorder, and/or transmitter. The Processor PC card is composed of seven major sections:

- CPU chip
- Clocks and timing
- Decode
- Power-up logic
- Memory
- Inputs
- Outputs.

Refer to the flow charts in Appendix D to help understand operation of the Processor PC card.

3-10.1 CPU CHIP. The CPU chip is a MOS, 8-bit parallel, central processor unit. The processor communicates over an 8-bit data and address bus (D0 through D7). The CPU also uses two input leads (READY and INTERRUPT) and four output leads (S0, S1, S2, and SYN) for control. Time multiplexing of the data bus permits transmission of control information, 14-bit addresses, and data. The CPU chip contains six 8-bit data registers; an 8-bit accumulator; two 8-bit temporary registers; four flag bits; and an 8-bit parallel, binary arithmetic unit which implements addition, subtraction, and logical operations. A memory stack containing a 14-bit program counter and seven 14-bit words is used internally to store program and subroutine addresses. The control portion of the CPU chip contains logic to implement a variety of register transfer, arithmetic control, and logical instructions. Most instructions are coded in one byte (8-bits); data-immediate instructions use two bytes; jump instructions utilize three bytes. The instruction set of the CPU chip consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutine (See Intel® 8008 Users Manual). Figure 3-10.2 is a CPU state transition diagram.

3-10.2 CLOCKS AND TIMING. The CPU chip is driven by two nonoverlapping clocks. Two clock periods are required for each state of the processor as shown in Figure 3-10.3. The SYN signal distinguishes between the two clock periods of each state.

The two-phase clock is generated from a single crystal (0.005 percent accurate) at a frequency of 9.8304 MHz. This signal is used to clock a parallel loaded synchronous 4-bit counter. By using the most significant bit of the shift register to clock two flipflops, new load data is derived and loaded on the carryout signal. Figure 3-10.4 diagrams the two-phase clock timing.

The timing of the other sections of the Processor PC card is generated by combinational logic using the processor states, the SYN signal, and the two-phase clock circuitry. The major timing events are as follows:

1. Lower address register – loaded on the leading edge of Q2 during the second half of the processor T1 state
2. Higher address register – loaded on the leading edge of Q2 during the second half of the T2 state
3. Memory write – data is loaded into the RAM memory on the leading edge of Q2 during the second half of the T3 state
4. Data input or output – input or output data loaded during the T3 state.

3-10.3 DECODE. The primary decode of the CPU chip is through the S0, S1, S2, and SYN signals. Table 3-10.1 lists state coding of the processor CPU chip.

A machine cycle consists of five states: two states in which an address is sent to memory (T1 and T2), one for the instruction or data fetch (T3), and two states for the execution of the instruction (T4 and T5). States T4 and T5 are skipped on certain instructions. Figure 3-10.5 illustrates processor activity during a single cycle.

An instruction may require one, two, or three machine cycles for complete execution. The first cycle is always an instruction fetch (PCI). The second and third cycles are for

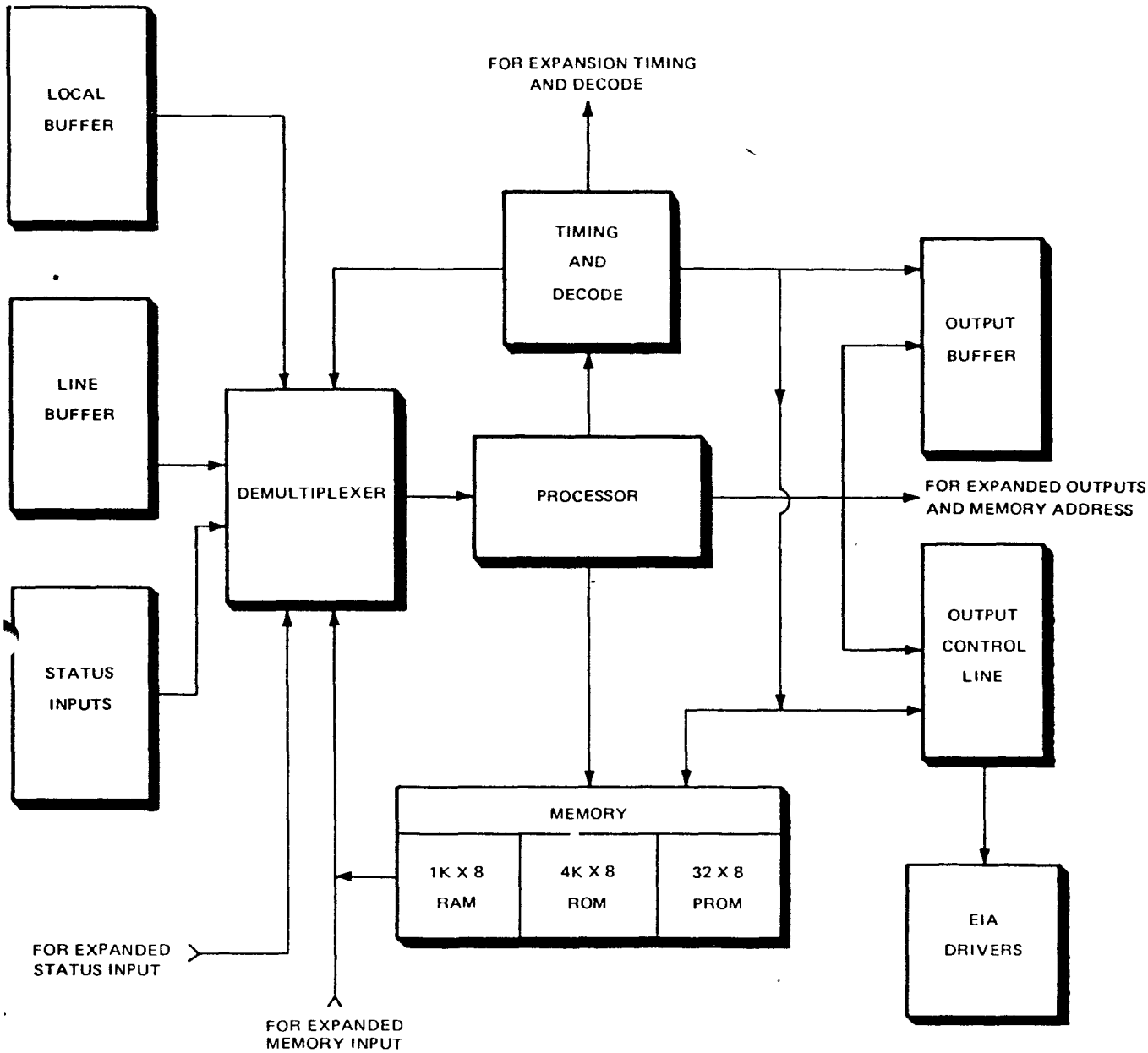


FIGURE 3-10.1. 1KX8 PROCESSOR PC CARD BLOCK DIAGRAM

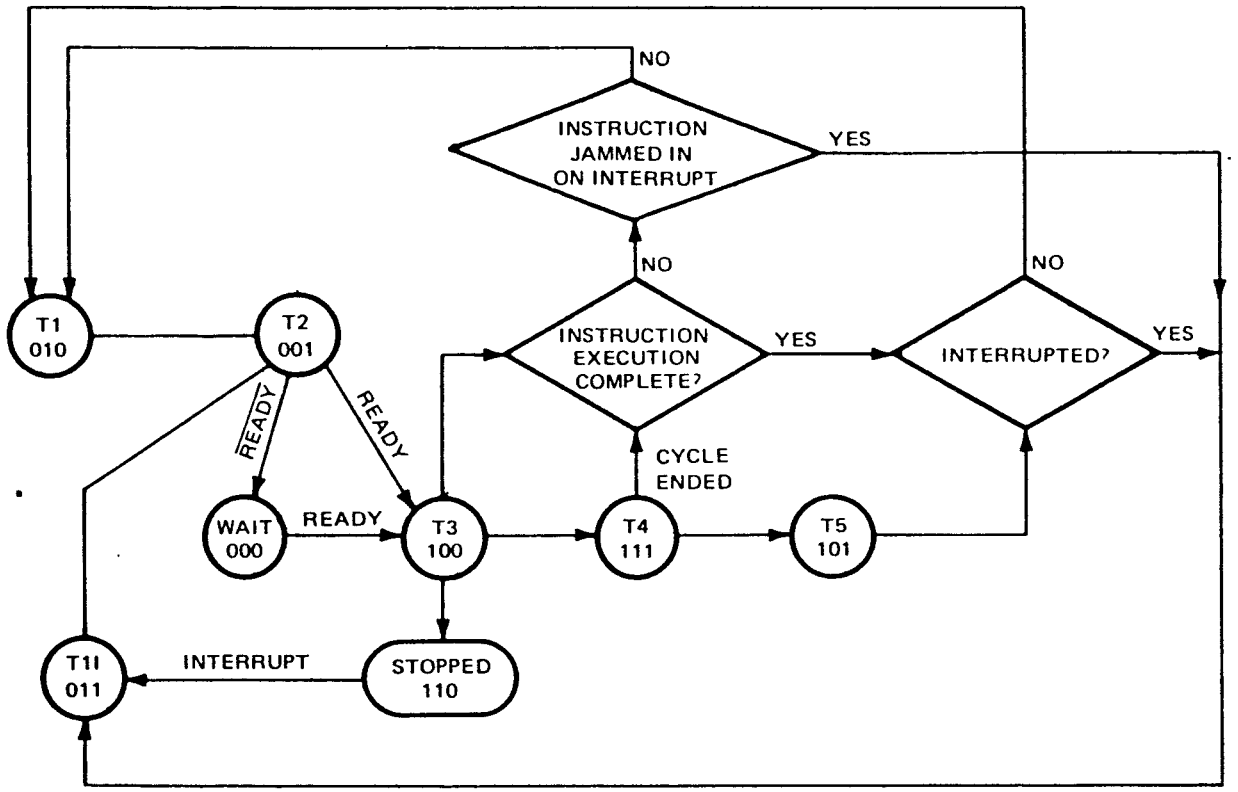


FIGURE 3-10.2. PROCESSOR PC CARD, CPU STATE TRANSITION DIAGRAM

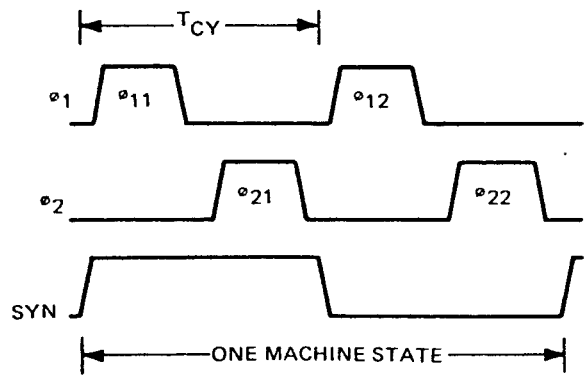


FIGURE 3-10.3. PROCESSOR PC CARD, CLOCKS TIMING DIAGRAM

TABLE 3-10.1. PROCESSOR PC CARD CPU STATE CODING

S_0	S_1	S_2	STATE
0	1	0	T1
0	1	1	T1I
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOPPED
1	1	1	T4
1	0	1	T5

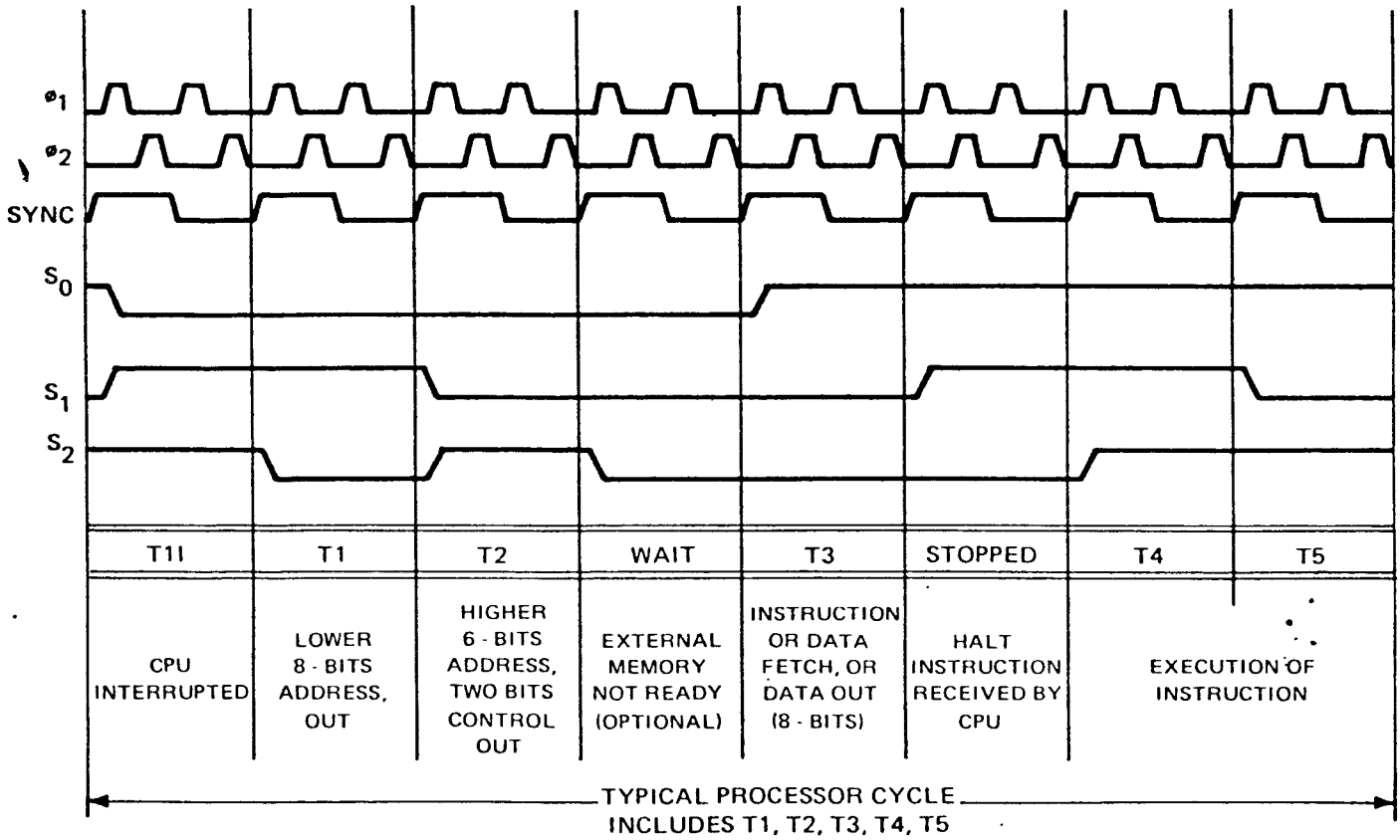


FIGURE 3-10.5. PROCESSOR PC CARD, SINGLE CYCLE ACTIVITY

data reading (PCR), data writing (PCW), or I/O operations (PCC). The cycle types are coded with two bits, H6 and H7, and are loaded into the H-register during T2. See Table 3-10.2 for bit codes of the cycle types.

The other 14 bits of the H and L registers are decoded as address lines during an instruction fetch cycle. When the second or third cycle is a PCR (memory read), the remaining 14 bits are again addresses. When the second cycle is a PCC (I/O operation), H4 and H5 are decoded to determine if the operation is an input or output operation. H4 and H5 are equal to zero on all input operations; anything other than zero indicates an output operation. H1, H2, and H3 are decoded to determine which port is being addressed. The L lines indicate what is to be done by the output port, or which input buffer (local or line buffer) is to be enabled. When the second or third cycle is a PCW (memory write), the remaining 14 bits of the H and L registers are the address of the location which will contain the data.

3-10.4 POWER-UP LOGIC. The Processor PC card uses the data terminal's master reset signal to reset the output control lines and the interrupt signal (SYNINTER). The master reset signal goes to normal level after 500 (±100) milliseconds and triggers the power-up logic. On the leading edge of the first P1 clock after master reset has gone, signal Y1INTER– is generated to perform the following:

1. Preset the H register
2. Reset the L register
3. Issue an interrupt to the CPU chip
4. Enable the memory lines to the CPU chip
5. Enable the 32 x 8 PROM address 0.

The CPU changes states to a T1I state, which resets the interrupt signal SYNINTER and accesses PROM address 0 for three consecutive cycles. The instruction the CPU chip executes from the PROM is an unconditional jump to location $004\ 104_8$. During the third cycle of the instruction execution, the CPU chip enters a T4 state and on the leading edge of the first P2 of the T4 state, the power-up logic is reset. Normal program execution continues from this address.

3-10.5 MEMORY. The 1Kx8 Processor PC card memory section contains 1024 8-bit words of RAM, 32 8-bit words of PROM, and 4096 8-bit words of ROM. All memory is handled the same way on any memory read operation. The RAM section also stores data. On a memory write instruction the RAM is addressed and enabled the same as a memory read operation, but the R/W1 signal commands the RAM to store the data at the addressed location.

3-10.6 INPUTS. The processor input logic consists of four 8-bit status ports and an 8-bit expansion port. The four status ports are a local data buffer port, a line data buffer port, and two ports consisting of 15 individual status lines. Table 3-10.3 lists the individual lines and address decodes of the ports.

3-10.7 OUTPUTS. The processor output logic consists of four control ports consisting of a parallel-to-serial data buffer, a 4-bit cassette code bit latch, and two 8-bit control latches. The 8-bit control latches furnish sixteen individually addressable control lines. Table 3-10.4 lists the individual lines and address decodes of the ports. The sixteen cassette codes are described in the 732/733 ASR/KSR Maintenance Manual (TI Manual 960129-9701).

TABLE 3-10.2. PROCESSOR H-REGISTER CYCLE TYPES AND BIT CODES

H_6	H_7	Cycle	Function
0	0	PCI	Designates the address is for a memory read (first byte of instruction)
0	1	PCR	Designates the address is for a memory read data (additional bytes of instruction or data)
1	0	PCC	Designates the data as a command I/O operation
1	1	PCW	Designates the address is for a memory write data

TABLE 3-10.3. PROCESSOR PC CARD INPUT SIGNALS

PORT 0 (H5 = 0, H4 = 0, H3 = 0, H2 = 0, H1 = 0)		
Bit		
0	Playback on-line and ready	RDRLINEF–
1	Playback error	RERRORF–
2	Cassette 1 on clear leader	BOEOCA1F
3	Cassette 2 on clear leader	BOEOCA2F
4	Recorder on-line and ready	RECLINE–
5	Printer on-line	PRNLINE
6	Playback on	RFEED
7	RDC enable switch	ON/OFF
PORT 1 (H5 = 0, H4 = 0, H3 = 0, H2 = 0, H1 = 1)		
Bit		
0	Line data ready	LINERDY
1	Local data ready	LOCRDY
2	Receive data	RCVDATA
3	Character gone	CHRGONE
4	Playback ready	RDRRDY
5	Recorder ready	RECRDY
6	High speed	HSPEED
7	Unused	
PORT 2 Serial In (H5 = 0, H4 = 0, H3 = 0, H2 = 1, H1 = 0)		
LO = 0	Local data buffer 8 bits parallel	
LO = 1	Line data buffer 8 bits parallel	

TABLE 3-10.4 PROCESSOR PC CARD OUTPUT SIGNALS

PORT 0 (H5 = 0, H4 = 1, H3 = 0, H2 = 0, H1 = 0)		
Bit		
0	Cassette strobe	CDSTB
1	First time	FSTIME
2	Keyboard paper advance	KBPA
3	Transmitter inhibit	XMTINH–
4	Processor local	AUX1LOC–
5	Duplex control	FULDPX–
*6	Request to send	RTS–
*7	Data terminal ready	DTR–
PORT 1 (H5 = 0, H4 = 1, H3 = 0, H2 = 0, H1 = 1)		
Bit		
0	Keyboard local remote off	KBLOCROF
1	Recorder remote off	RECROF
2	Printer remote off	PRNROF
3	Playback remote off	RDRROF
4	Display 1	DISPLAY1
5	Display 2	DISPLAY2
6	Display 3	DISPLAY3
7	Display 4	DISPLAY4
PORT 2 Cassette Control (H5 = 0, H4 = 1, H3 = 0, H2 = 1, H1 = 0)		
PORT 3 Serial Data Out (H5 = 0, H4 = 1, H3 = 0, H2 = 1, H1 = 1)		

*These two signals are fed through EIA drivers before going off the board.

3-11. GENERAL PURPOSE EXPANSION PC CARD.

The General Purpose Expansion PC card is an extension of the 1KX8 Processor PC card. All basic control lines, data lines, and address lines are supplied by the 1KX8 Processor PC card via a 50-pin top access cable (TI Part No. 969625-0001). Since the two PC cards are so interrelated, knowledge of the Processor PC card (Section 3-10) will aid comprehension of the Expansion PC card. The General Purpose Expansion PC card, diagrammed in Figure 3-11.1, contains three major sections:

- Memory
- Inputs
- Outputs.

A flow chart illustrating Expansion PC card operation is contained in Appendix D.

3-11.1 MEMORY. The General Purpose Expansion Memory consists of 1k x 8-bit words of RAM, 4096 x 8-bit words of ROM, and optional 4096 x 8-bit words of PROM. The 4k of ROM is a continuation of the Processor PC card's 4k ROM memory, and the 1k of RAM is a continuation of the Processor PC card's RAM. Table 3-11.1 lists the address decode of the H address register bits for the General Purpose Expansion memory.

The 2kx8 ROMs are addressed by the H address register bits H2, H1, H0, and all 8 bits of the L address register. Figure 3-11.2 is the ROM timing diagram. Data from the ROMs are multiplexed to the CPU chip via I0 through I7. The 1kx8 RAMs are addressed by the same bits as the ROMs. Figure 3-11.3 is the RAM timing diagram. Data from the RAMs are multiplexed to the CPU chip through tristate busses to the data bus (I0 to I7).

The Expansion PC card is also wired to accommodate 2k words of PROM (selectable at one of two addresses) and its associated circuitry. These components are not installed, but may be used in future options or special applications.

3-11.2 INPUTS. The Expansion PC card contains four input ports which are multiplexed to the expansion lines (EX0 through EX7). The decode for each input port is specified by H address register bits H1 and H2. Table 3-11.2 lists the decode and ports.

3-11.2.1 Real-Time Clock. The real-time clock is an 8-bit counter driven by the terminal system clock (800 CLK). The maximum time indicated by one full cycle of the clock is 160 milliseconds.

3-11.2.2 Station ID Code. The station identification code is implemented through the seven pencil switches. The pencil switch (PS1 through PS7) forms a 7-bit ASCII character. An additional optional pencil switch module (seven switches) can be added and multiplexed to the same input port via bit 0 of the L address register.

3-11.2.3 Terminal Status. The following terminal status information is input to the Expansion PC card from the motherboard:

- LINEBUSY–
- PBUSY
- TERLINE–
- BREAK–
- BUSY–

EIART, EIASH, and EIADSR are converted to TTL signals, and combined with the previous five signals, form the terminal status input port. The miscellaneous input port bits are FTSW (footswitch), INP1 and INP2 (extra input lines from XA2), and TS1 and TS2 (LINE PROTOCOL switch S1), and the following EIA signals converted to TTL levels: EIADCD, EIASB, and ETADATAIN.

3-11.2.4 Output Port. The main function of the output port is to control the option panel display LEDs. Output data in the form of a ONE or a ZERO is sent to an 8-bit addressable latch. Lines L2–, L1–, L0– from the address register supply the address of the latch bit affected. Seven of the output bits inverted by U32, and U34 control seven LEDs on the option panel.

An EIA driver inverts the eighth bit (RVCH) and sends it out as RVCHXMT. The EIA driver also inverts the TTL signal TTYDATOT and sends it out as EIADZOUT on the J2 connector. Ring indicator RI2 is buffered and drives the eighth LED on the option panel. The Expansion PC card is also wired for another optional addressable latch.

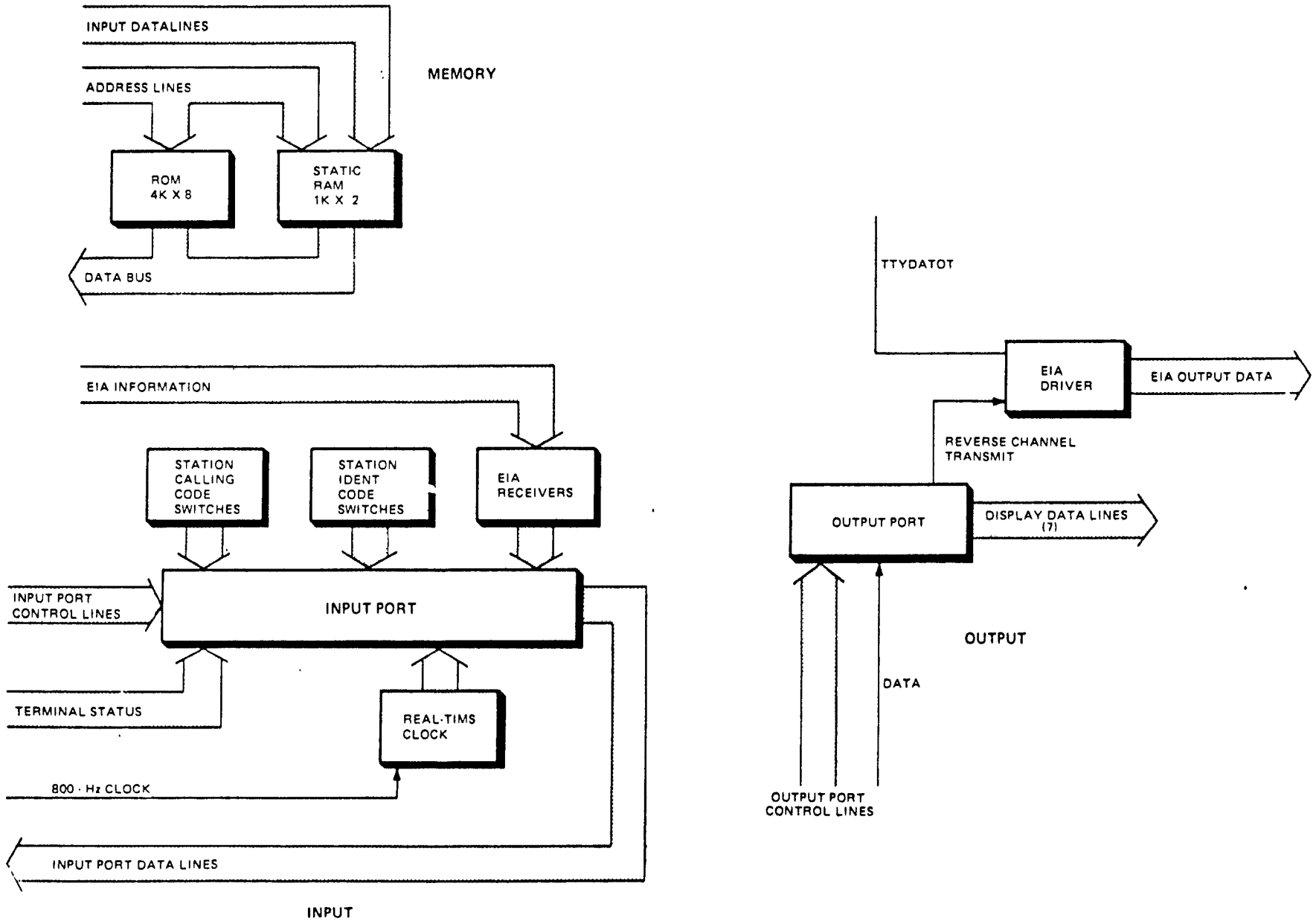


FIGURE 3-11.1. GENERAL PURPOSE EXPANSION PC CARD BLOCK DIAGRAM

TABLE 3-11.1. GENERAL PURPOSE EXPANSION PC CARD MEMORY DECODE

H-Register Bits	H5–	H4–	H3–
RAM	0	1	0
Optional PROM	0	1	1
2kx8 ROM	1	0	0
2kx8 ROM	1	0	1

TABLE 3-11.2. GENERAL PURPOSE EXPANSION PC CARD INPUT PORTS

H2–	H1–	Input Port
0	0	Real-Time Clock
0	1	Station Identification Code
1	0	Terminal Status
1	1	Miscellaneous

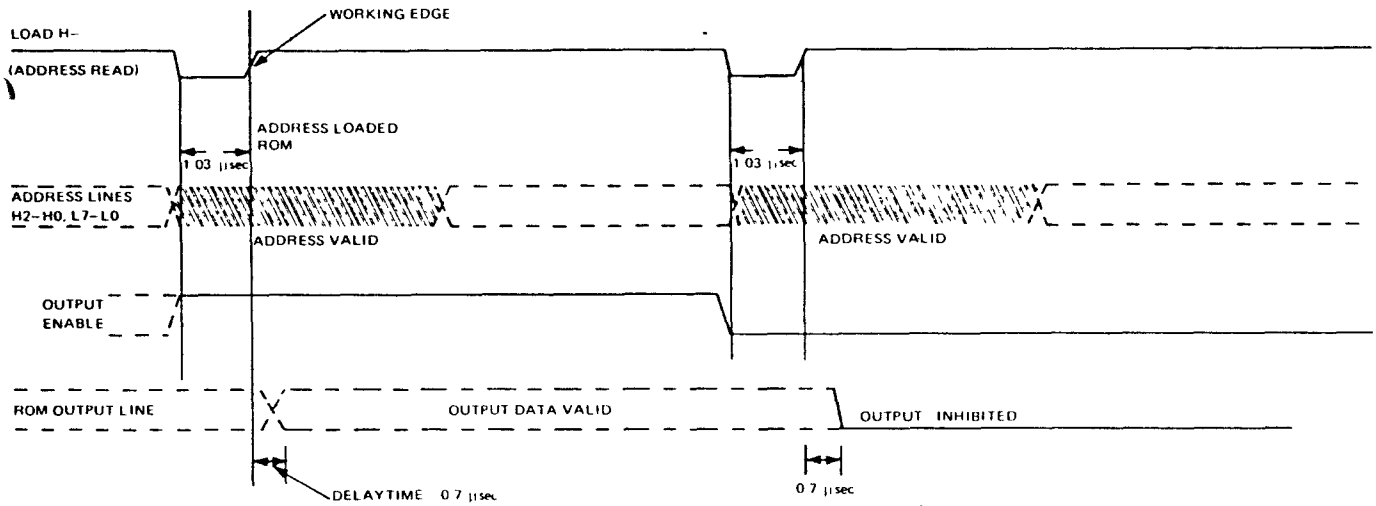


FIGURE 3-11.2. GENERAL PURPOSE EXPANSION PC CARD ROM MEMORY TIMING DIAGRAM

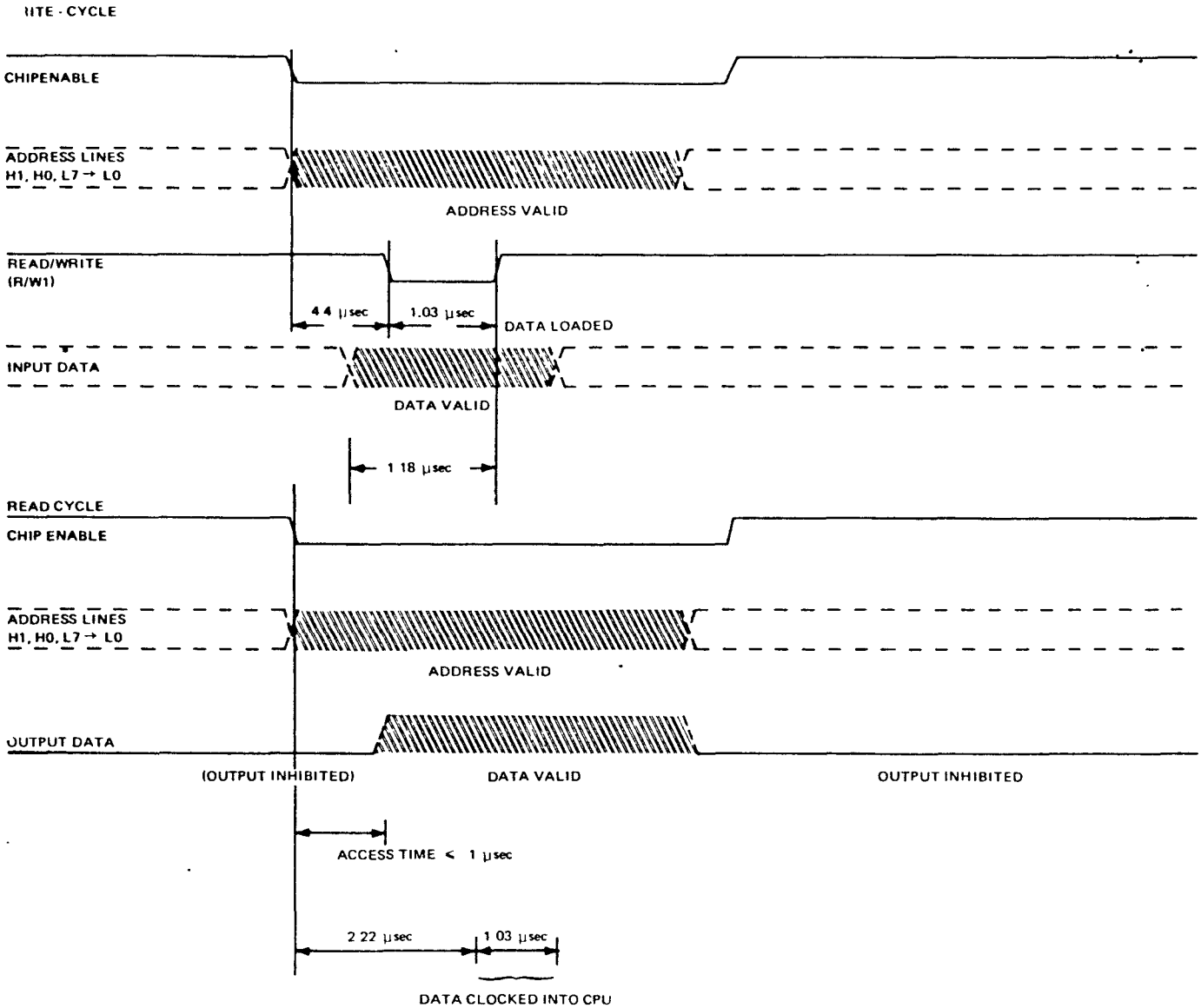


FIGURE 3-11.3. GENERAL PURPOSE EXPANSION PC CARD RAM MEMORY TIMING DIAGRAM

3-12 1200-BAUD MODEM PC CARD.

The 1200-baud modem converts asynchronous data into frequency-shift keyed (FSK) tones for presentation to a Bell type-CBS Data Access Arrangement (DAA) and provides the control necessary for automatically answering and manually originating calls over the Bell Direct Distance Dial network. The modem is compatible with Bell type-202C data sets and interfaces to a Bell type-CBS DAA. The standard functions of the modem include transmit, receive, and automatic answer.

A signal interface block diagram for the modem is shown in Figure 3-12.1 and pin assignments are listed in Table 3-12.1. All signal interface levels to the modem are RS232C-compatible.

3-12.1 INTERFACE SIGNALS. The CBS DAA interface signals are as follows:

- Data Tip is one of the pair for connection to the telephone line; it is signal common.
- Data Ring is the other of the pair for connection to the telephone line.
- Data Access is held ON by the modem to request a data path to the telephone line.
- Off Hook is held ON by the modem to answer and maintain a call.
- Coupler Cut-Through is held ON by the DAA when a data path has been established to the telephone line.
- Switch Hook is held ON by the DAA when the receiver has been lifted from the cradle for manual origination of calls.
- Signal Ground is the return path for control signals.
- Ring Indicator is held ON by the DAA while a ringing signal is present.

The terminal interface signals are as follows:

- Transmit Data is the data to be converted to FSK tones for presentation to the DAA.
- Receive Data is data which has been converted from FSK tones to RS232C-levels representing the MARK/SPACE condition of the telephone line.

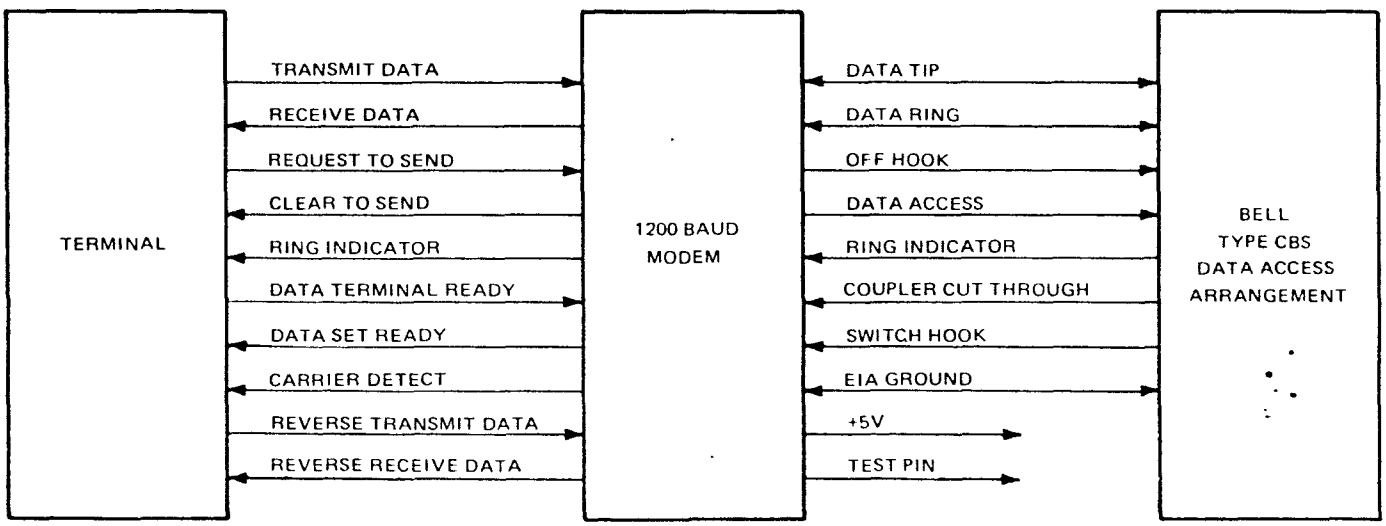


FIGURE 3-12.1. 1200-BAUD MODEM SIGNAL INTERFACE BLOCK DIAGRAM

TABLE 3-12.1. 1200-BAUD MODEM PIN ASSIGNMENTS

	Signal	Pin	Jumper Pin
Signal Interface:	Transmit Data	6	–
	Receive Data	C	–
	Request to Send	12	7
	Clear to Send	E	–
	Ring Indicator	19	5
	Data Terminal Ready	H	–
	Data Set Ready	D	–
	Carrier Detect	4	–
	Reverse Transmit Data	9	–
	Reverse Receive Data	11	–
	Data Tip	16	8
	Data Ring	17	13
	Off Hook	18	10
	Data Access	U	14
	Coupler Cut Through	V	15
	Switch Hook	T	R
	EIA Ground	F	–
	Test Pin	X	–
Power Interface:	Ground	1,2,42,43, A,B,X,Y	–
	+5V	41,W	–
	+12V	40,V	–
	-12V	39,U	–

- Request to Send notifies the modem that the terminal wants to transmit data.
- Clear to Send is held ON by the modem, notifying the terminal that it is ready to transmit data.
- Ring Indicator is held ON by the modem when it detects the presence of a ringing signal.
- Data Terminal Ready is held ON by the terminal when it is ready for the modem to answer calls and enable communication; this signal goes OFF when the terminal wants the modem to discontinue a call.
- Data Set Ready is held ON by the modem after a call has been answered, and a communication path is established.

- Carrier Detect is held ON by the modem when the receiver has detected the presence of carrier for 40 (±10) milliseconds and the modem is in the receive mode. Presence of carrier means that a MARK or SPACE frequency of detectable amplitude and all other frequencies are detected.

3-12.2 OPERATING SEQUENCES. The sequences of operation for the modem functions are given below.

3-12.2.1 Auto Answer. The modem automatically answers calls in the following sequence:

1. Senses ringing condition on the ring indicator (RI) line
2. If Data Terminal Ready line is on, the modem sets a latch, causing the off hook (OH) line and data access line to come on. The modem forces a 2025 (±1.0 percent) Hz answer tone to be transmitted for at least three seconds after coupler cut through (CCT) comes on
3. Senses coupler cut through, then holds data set ready line on as long as CCT line is on.

The modem discontinues a call in the following sequence:

1. Senses data terminal ready (DTR) line going off, then resets the latch causing off hook (OH) line and Data Access line to go off
2. Senses coupler cut through line going off then holds the data set ready line off.

3-12.2.2 Receive to Transmit Mode Transition. The modem enters the transmit mode in the following sequence:

1. Senses Request to Send line coming on
2. Switches and holds on the clear to send line after a delay of 200 (±20) milliseconds
3. Releases the transmitter squelch and squelches the receiver line to hold it in the MARK state
4. Assumes the transmit mode.

3-12.2.3 Transmit to Receive Mode Transition. The modem enters the receive mode in the following sequence:

1. Senses the request to send line going off
2. Switches the clear to send line
3. Transmits soft carrier (900 Hz) for 25 (±5) milliseconds
4. Squelches the transmitter
5. Releases receiver squelch after the soft carrier is transmitted
6. Assumes the receive mode
7. Enables carrier detect after MARK or SPACE frequency is present for at least 40 (±10) milliseconds.

3-12.2.4 Manual Origination of Calls. Manual origination of calls is enabled by the modem in the following manner:

1. The modem senses switch hook (SH) when the handset is lifted from the telephone deskset cradle.
2. When DTR is on and SH is on, the modem sets a latch, causing the off hook and data access lines to come on.
3. The modem senses CCT coming on and then holds the DSR line on as long as CCT is on.

The modem discontinues a manual call in the same sequence described in paragraph 3-12.2.1 above.

3-13 STATUS DISPLAY PANEL.

The status display panel consists of eight indicating units with wiring provided for four additional indicating units, two optional inputs, and a ground line. Each indicating unit consists of a light-emitting diode (LED) and a bias resistor. When a logic HIGH signal is presented to one of the input lines (LED1 to LED7 or RIOT), the corresponding LED extinguishes. When a logic LOW signal is presented to one of the input lines, the corresponding LED illuminates.

SECTION IV

BASIC EQUIPMENT PC CARDS AND FUNCTIONS

4-1 GENERAL.

The following standard equipment PC cards are installed in the Model 742 Programmable Data Terminal as shown in Figure 4-1. Schematics for the PC cards are contained in Appendix C.

4-2 KSR (KEYBOARD) UNIT.

4-2.1 POWER MODULE MOTHERBOARD. The KSR motherboard provides interconnections between all other PC cards in the KSR section. Mounted on the motherboard are the power supply filter capacitors, the 5-volt crowbar SCR, and bleeder resistors for the filter capacitors. The keyboard, printer drive assembly, bell, power module, cassette system, and output connectors plug into the power module motherboard.

4-2.2 REGULATOR/AMPLIFIER. This PC card contains the motor drivers for the print head-stepping and paper advance motors and the printhead-lift solenoid driver. This PC card also contains the 4-volt switching regulator.

4-2.3 CONTROL REGULATOR. This PC card contains the power-on reset circuit and the positive 12-volt and negative 12-volt regulators. It also contains the auxiliary/reference 5-volt supply, the 5-volt regulator oscillator, the 5-volt regulator driver, and the 5-volt crowbar.

4-2.4 PRINTER CODE (ASCII). This PC card contains the keyboard interface which converts parallel data from the keyboard to serial data for the data bus. It also contains the character generator which converts 8-bit data from the data bus to 35 bits for the printhead. The Printer Code PC card also decodes printer control characters. The printhead compensation and driver circuits are on this PC card along with the contrast adjustment and overvoltage protection for the printhead. The driver circuit for the bell is also on this PC card.

4-2.5 PRINTER CONTROL. The Printer Control PC card has the circuitry to step and damp the printhead, backspace the printhead, and lift the printhead. It includes a column counter and decoders to decode column 80, column 72 (end-of-line bell), and column 12 (carriage return brake). This PC card also contains the carriage return and carriage return brake circuits. Signals for line feed and paper advance are generated on this board. A switch is provided to change from single-line feed to double-line feed. The timing for the print pulse and the printer-busy signal is also generated on this PC card.

4-2.6 TERMINAL CONTROL. The Terminal Control PC card checks the status of all devices (line/local/off), accepts requests, and sets priorities. It uses the status and priorities to determine which devices receive enable signals. Terminal control generates these enables plus the eight clocks used to clock data to and from the data bus. Terminal control also generates the busy signal.

4-2.7 1200 DUAL FORMAT TRANSMIT/RECEIVE. The Transmitter/Receiver PC card contains the EIA interface circuits and the line receiver and transmitter. The ASCII receiver circuits receive data from the line at 10, 15, 30, and 120 characters per second (CPS), and clocks this data to the data bus with an enable and eight clocks from terminal control. The transmitter circuits on this PC card accept data from the data bus using an enable and eight clocks, add parity and START and STOP bits, and then clock this data to the line interface at the appropriate line speed. The SPEED switch (LO, MED, HIGH) is located on this card along with the FULL/HALF DUPLEX switch and the break circuit. The line-busy signal is generated on this card. This PC card also contains the crystal oscillator and countdown circuits which generate all master clocks used in the data terminal in addition to the receiver/transmitter clocks.

4-2.8 1KX8 PROCESSOR. The 1KX8 Processor PC card contains the 8-bit parallel CPU chip, a memory section, an input section, an output section, a two-phase clock circuit, and a connector for expansion. The memory section consists of two 2K ROM's, a 1kx8 RAM, and a 32x8 PROM. The input section has two 8-bit serial-to-parallel buffers and two 8-bit status ports, which consists of 15

internal status conditions of the various devices on the data bus, including four concerning the processor. The output section consists of a parallel-to-serial 8-bit buffer, a 4-bit latch for the cassette control lines, and two 8-bit dressable latches for the 16 individual control lines, two of which go to EIA drivers. The two-phase clock circuit is composed of a crystal oscillator and countdown circuits which generate the two-phase nonoverlapping clocks required by the CPU chip. The 50-pin top access connector provides all necessary signals for expanding memory, inputs, or outputs.

4-2.9 PRINTHEAD INTERFACE. The Printhead Interface PC card plugs into the Printer Code PC card and the printhead connects to this card. It consists of a 35-bit serial-to-parallel converter and 35 buffers. The card accepts serial data from the character generator and converts it to parallel data and buffers for the printhead.

4-2.10. GENERAL PURPOSE EXPANSION. The General Purpose Expansion PC card operates as an extension of the Processor PC card. It provides additional memory and increased input and output port capability. The additional memory consists of 1000 words of RAM, 4000 words of ROM, and an optional 2000 words of PROM, selectable at one of two addresses. The information channeled through the input port includes:

- All EIA input information
- Station identification code
- Real-time clock
- Footswitch status
- Break status
- Optional operator input information from the status display.

The output port controls the LEDs on the status display panel with the exception of the ring indicator (RI) signal which follows EIA RI provided to the terminal. It also controls the status of RVCHXMT which is converted to EIA levels and sent to J1 and J2. Provision is made for a second optional port. This PC card also converts TTYDATOT to EIA levels and jumpers reverse channel information from J1 to J2.

4-2.11 STATUS DISPLAY PANEL. This PC card contains the LED's and associated current-limiting resistors driven from the General Purpose Expansion PC card. Its function is to provide visual information to the operator concerning various states of the terminal. The status display PC card also contains wiring provisions for four additional indicators and two inputs.

4-3 ASR MODULE (UPPER UNIT).

4-3.1 ASR MODULE MOTHERBOARD. The ASR motherboard connects all PC cards in the ASR unit with each other and with the tape transports. The motherboard is connected to the KSR motherboard through a 36-conductor cable.

4-3.2 DISPLAY. The Display PC card contains the switches and indicators to operate the ASR. There are four 3-position switches to place the keyboard, printer, playback, and recorder on LINE, OFF, or LOCAL. Each transport has two switches: one for REWIND and one for LOAD and FF (fast forward). There is also a mode selection switch to place the transports in RECORD or PLAYBACK. The Playback Control has three momentary switches with debounce circuits for continous START/STOP, BLOCK FORWARD/REVERSE, and CHARACTER FORWARD. The Record Control has one momentary switch for ON/OFF, one momentary switch with debounce circuits for PRINT buffer/ERASE and one two-position switch for CONT/LINE format. The Display PC card also has LED'S and drivers to indicate the following conditions for each cassette: indicators for mode (PLAYBACK/RECORD), READY, and END of tape. The Playback Control has indicators for playback ON and playback ERROR. The Record Control has an 8-bit character display and a record-ON indicator.

4-3.3 MOTION CONTROL. The Motion Control PC card accepts inputs from the switches on the Display PC card and from the transport sensors (EOT, BOT, cassette in place, door closed, write tab, etc.) and generates signals to indicate record READY, Playback READY, recorder on-LINE, and playback on-LINE. This card also generates forward, reverse, and fast signals for the transports and the load signal for the gap counter. Circuits which identify and remember which end of the tape is which are also on this PC card.

4-3.4 REMOTE CASSETTE CONTROL. This PC card has the gap counters and mode control for both cassettes. The block reverse function of playback control is located on this PC card. The playback timers (TR3/4T, TR5/4T, and TR21/4T) are located on this PC card along with the tape-erase circuits. This card also contains the decoding for remote control of the cassettes. Four code bits and a strobe are decoded into the following 15 different functions:

1. Playback on
2. Playback off
3. Record on
4. Record off
5. Rewind cassette 1
6. Rewind cassette 2
7. Load/fast forward cassette 1
8. Load/fast forward cassette 2
9. Block forward
10. Block reverse
11. Character forward
12. Cassette 1 record
13. Cassette 2 record
14. Cassette 1 stop
15. Cassette 2 stop.

4-3.5 PLAYBACK CONTROL. The Playback Control PC card contains the playback control (continuous, block forward, and character forward) and tape read controller circuits. The playback buffers with their address counters are also on this PC card in addition to the character counter which is used for playback control and the tape read control and stop-on-read-error circuits.

4-3.6 RECORD BUFFER CONTROL. This PC card contains the 1024-bit record buffer with the punch address counter, tape write address counter, and the address select gates. The punch address register, which is used in the editing function, is on this PC card along with the memory timing circuits and the reference clocks (TRFCLKA and TRFCLKB) for the transports. Also on this card are the serial-to-parallel-to-serial registers which accept data from the line, decode and add the carriage return and end-of-block bit, and convert back to serial for the memory. The character display register also is located on this PC card.

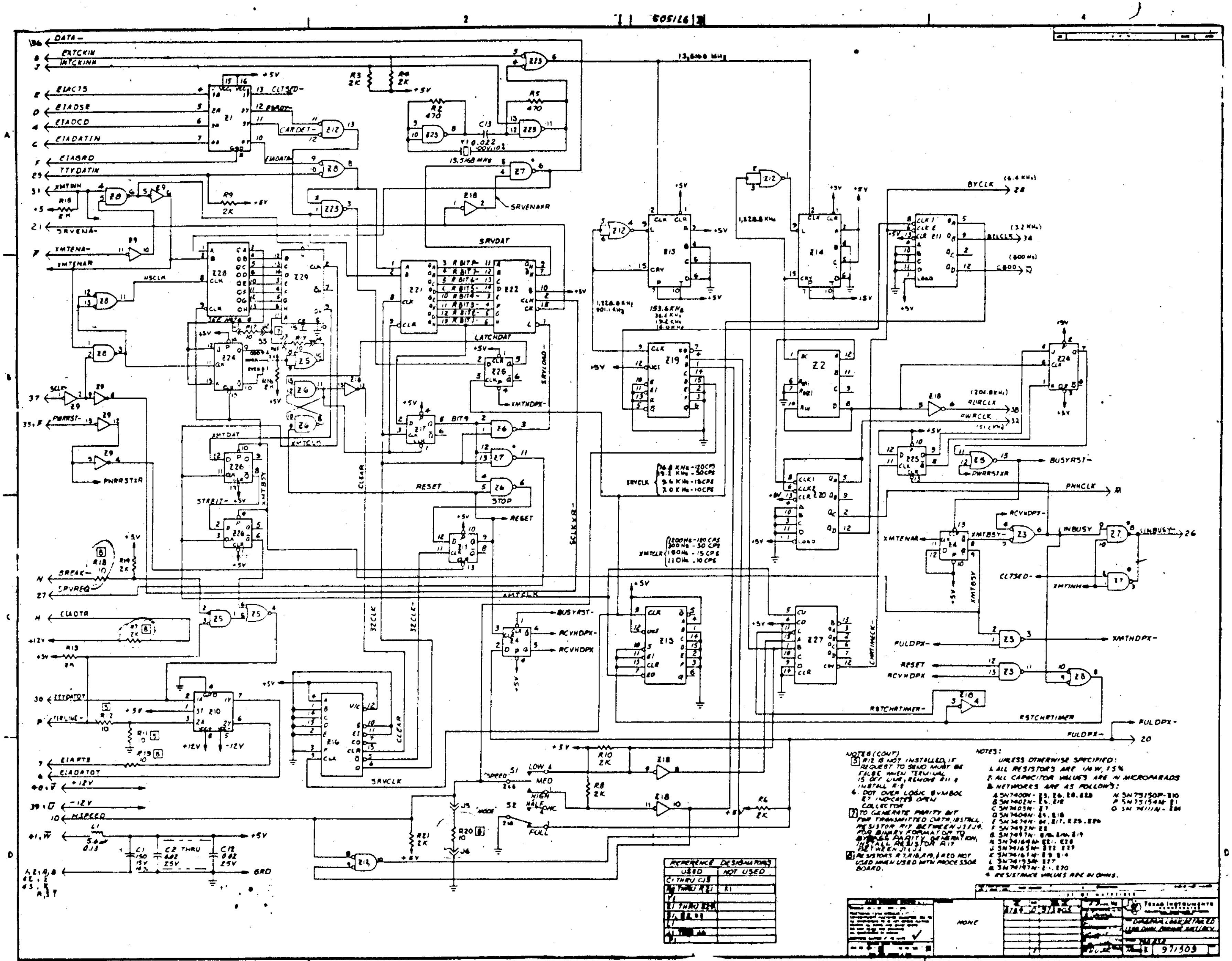
4-3.7 TAPE READ/WRITE. The Tape Read/Write PC card contains the tape read circuit which converts phase-encoded (PE) data from the transport into binary data and the tape write circuit which converts binary data from the write data register into PE data to go to the transport. It also contains the tape write controller which formats the data as follows: preamble, 86 data characters or nulls, two block check characters (nulls), and a postamble. The block character counter and the block counter are also located on this PC card.

4-3.8 RECORD CONTROL. The Record Control PC card contains the flipflops to synchronize the signals from the record switches (PRINT, ERASE, record ON, and manual STOP) and the state counters for the recorder. The punch character counter and character backspace counter with decoding for count = 0 and count = 86 are included on this PC card along with the punch counter buffer register.

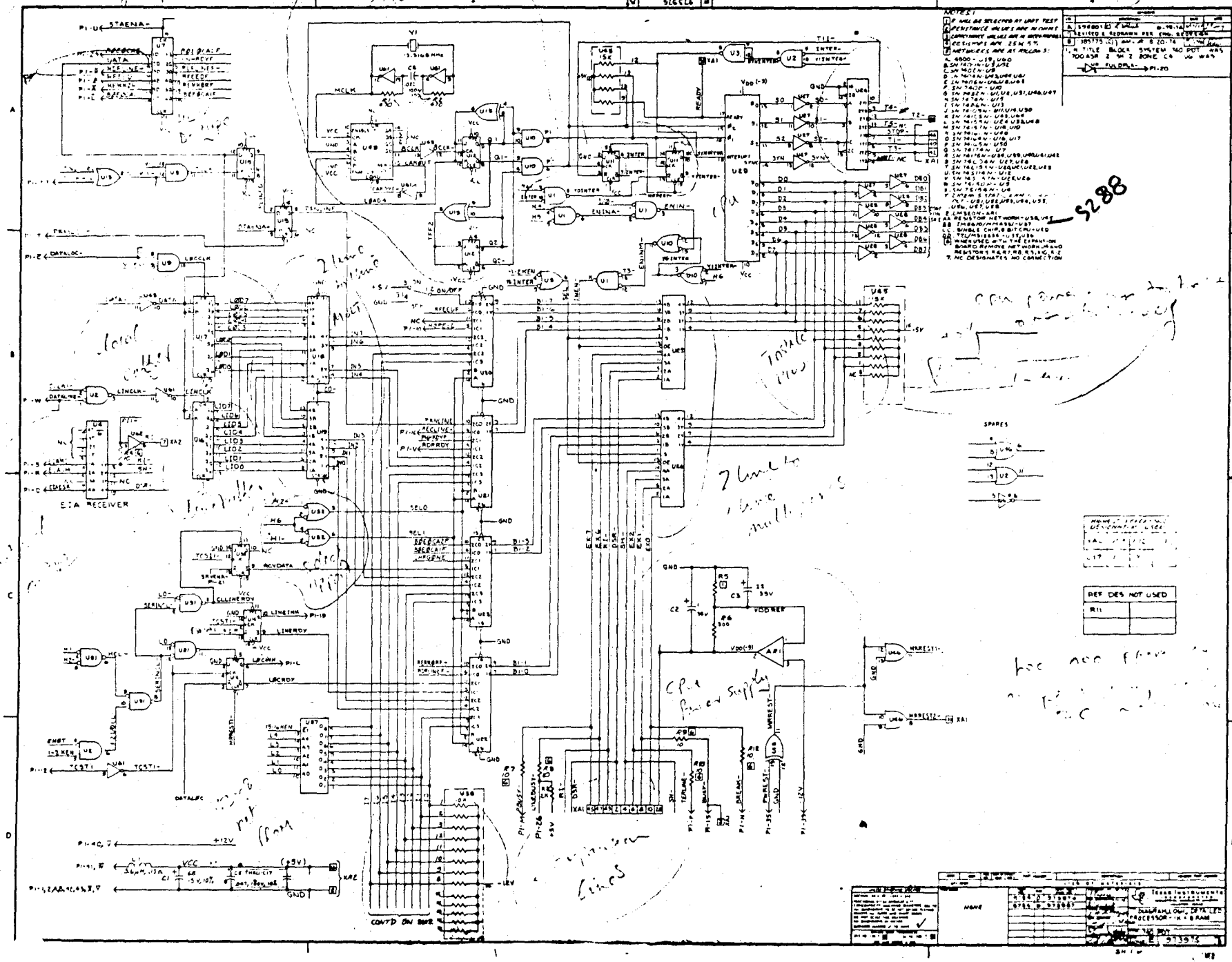
TABLE 5-1. FAILURE ANALYSIS CHART, MODEL 742 PROGRAMMABLE DATA TERMINAL

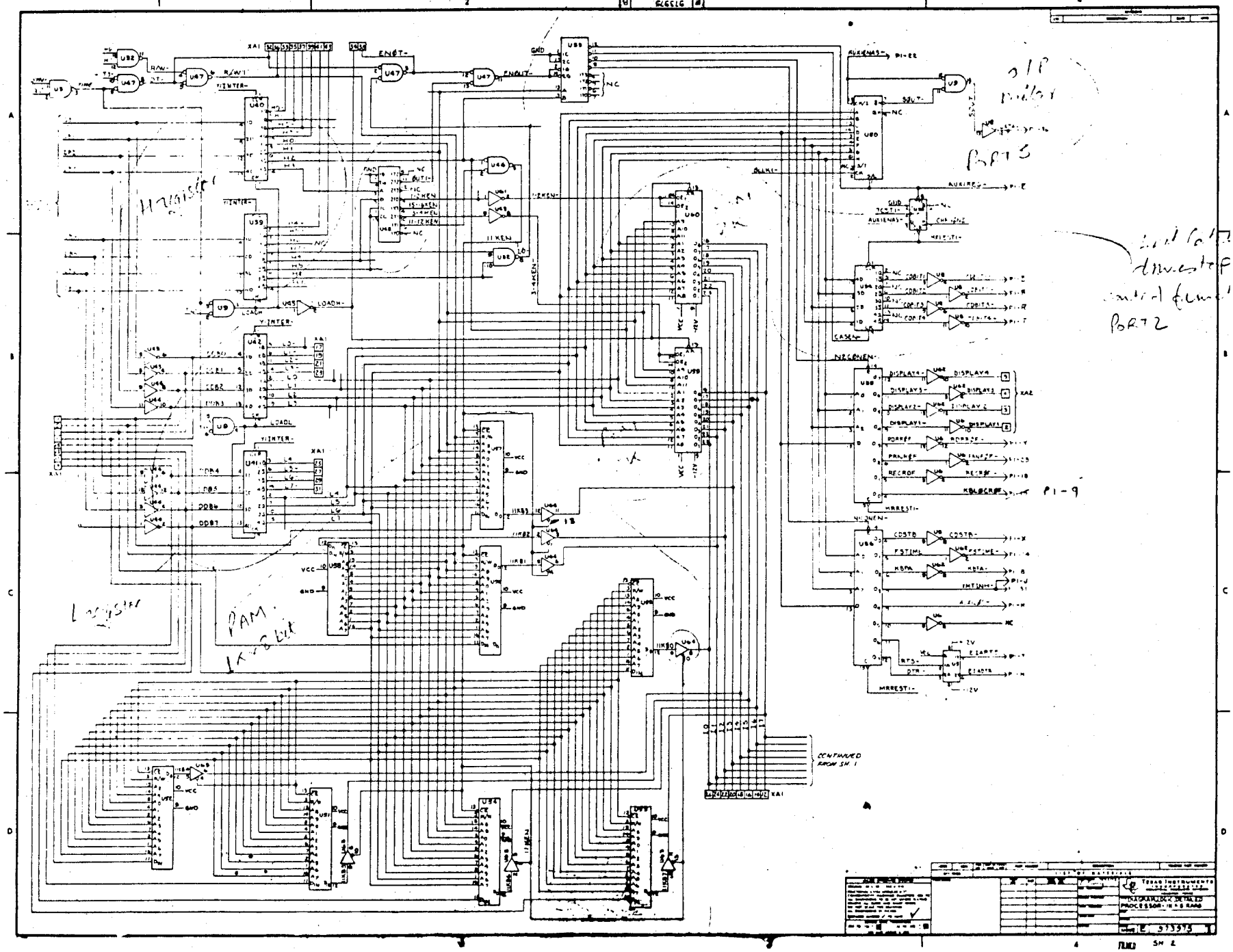
Symptom	Power Assembly	Drive Assembly	Keyboard	Regulator/Amplifier Card	Control/Regulator Card	Printer Code Card	Printer Control Card	Terminal Control Card	1200 Dual Format Card	Line Interface Card	Processor or Expansion Cards	Printhead Interface	Printhead	Status Panel
Terminal Completely Inoperative	1			3	2			5	6		4			
Printhead Does Not Return when Power Applied	1	4		3	2		5							6
Printhead Returns To Wrong Column		1		2			3							
Paper Advance Inoperative		3	4	2			1							
Paper Advance Continuous			2								1			
Will Not Print Although Head Steps						1					1	2	3	
Printhead Oscillates		2		3			1							
Printhead Steps Erratically		2		3			1							
Printhead Does Not Lift On Paper Advance		1		2			3							
Keyboard Inoperative Except Paper Advance			2			3		4			1			
Specific Keys Will Not Print			1			2								
Serial Data Not Transmitted								3	2	1	4			
Serial Data Not Received								3	2	1	4			
Carriage Return Too Slow		1					2							
Does Not Print All Elements		3				4						2	1	
Printhead Does Not Step		2		1			4	3						
No NORMAL Mode Light When Power Applied											1			2
BREAK Key Will Not Return Terminal To NORMAL Mode			3								1			2
Auto Search Control Does Not Function			3								1			
Remote Device Control Does Not Function								4	3	2	1			
Auto Answer Control Does Not Function								3		1	2			
Answer-Back Memory Does Not Function								3		2	1			
Terminal Fails to Receive Station ID (Multidrop)								3		2	1			
Status Display Lamps Fail to Light											2			1

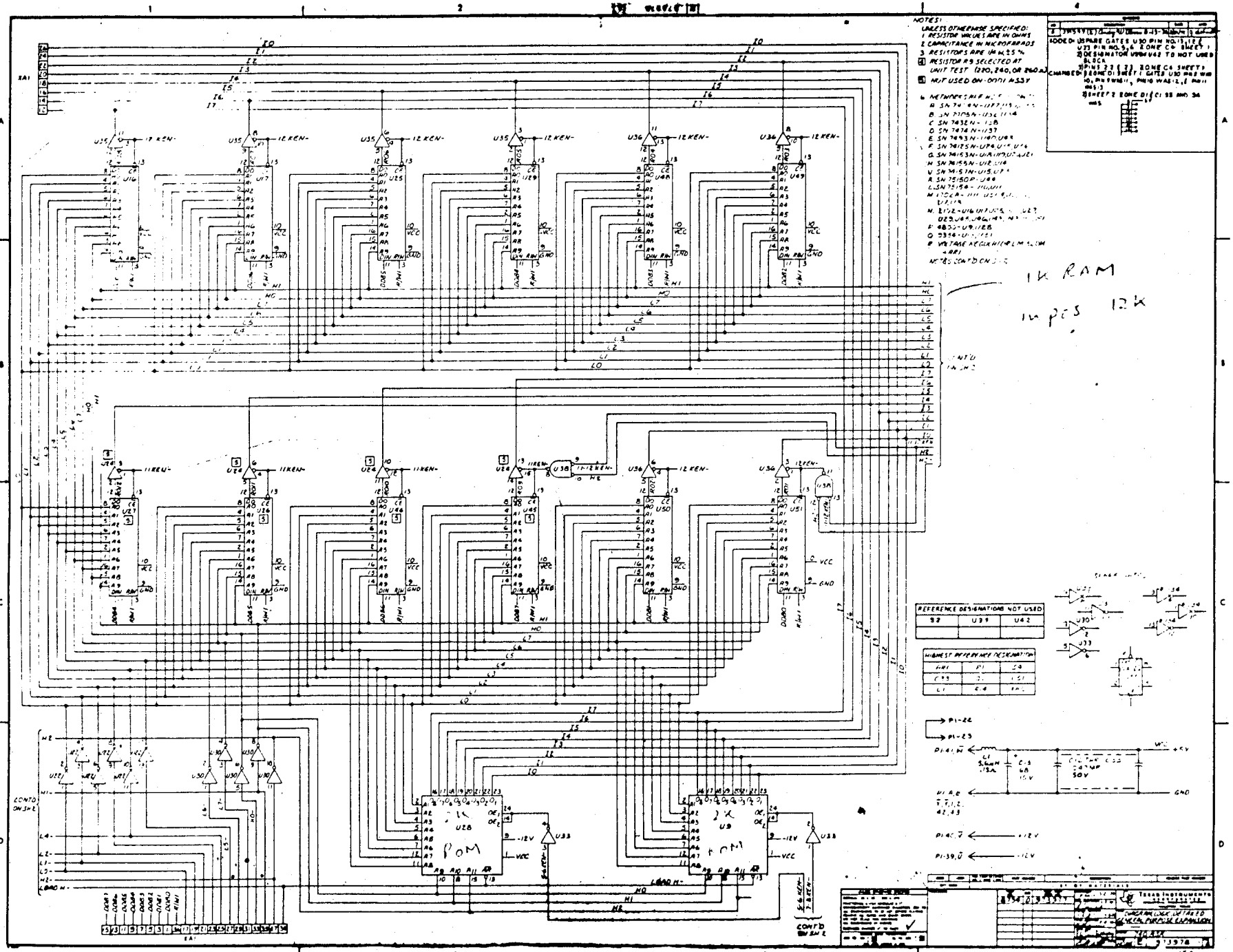
NOTE: Numbers within boxes indicate order of failure probability.

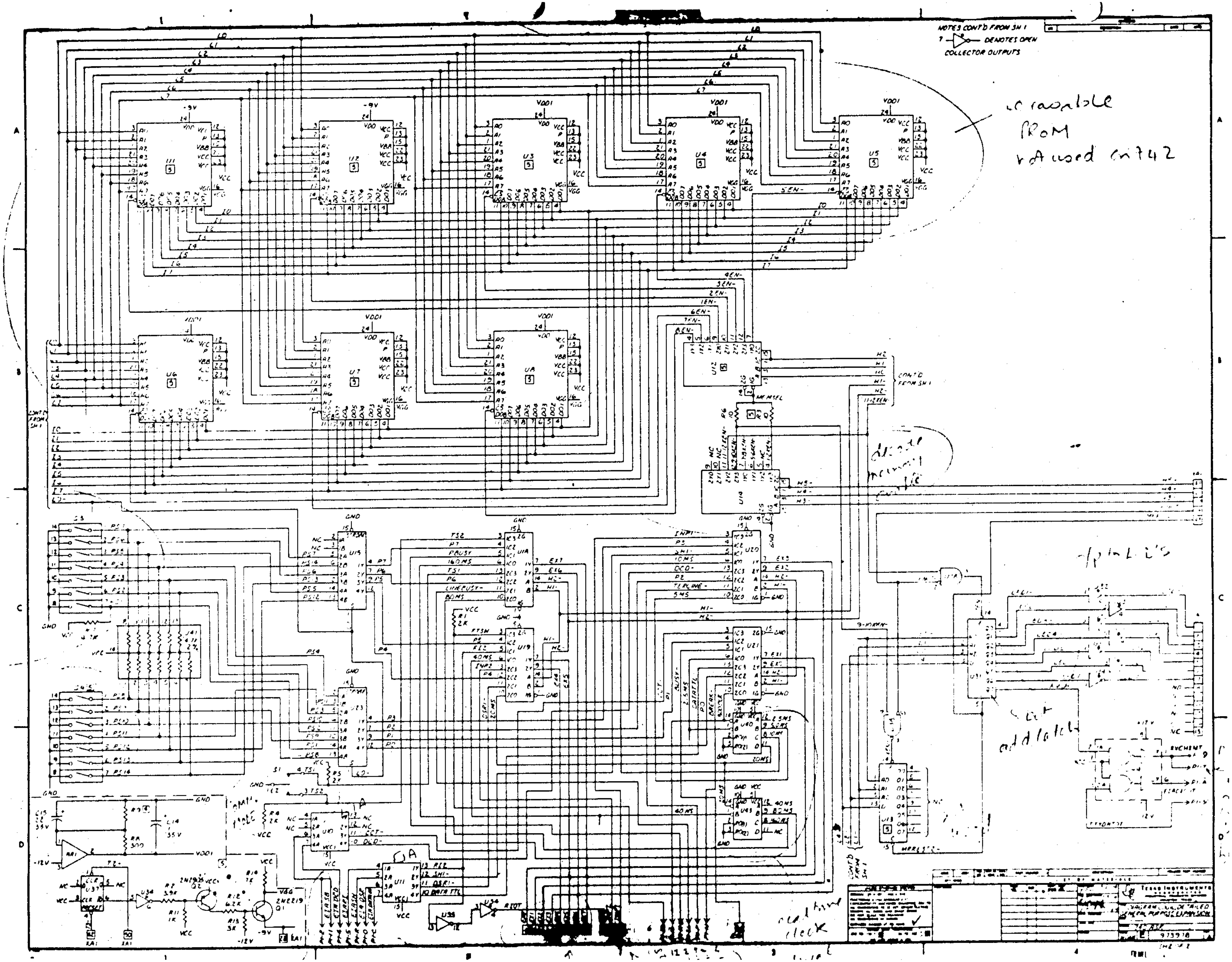


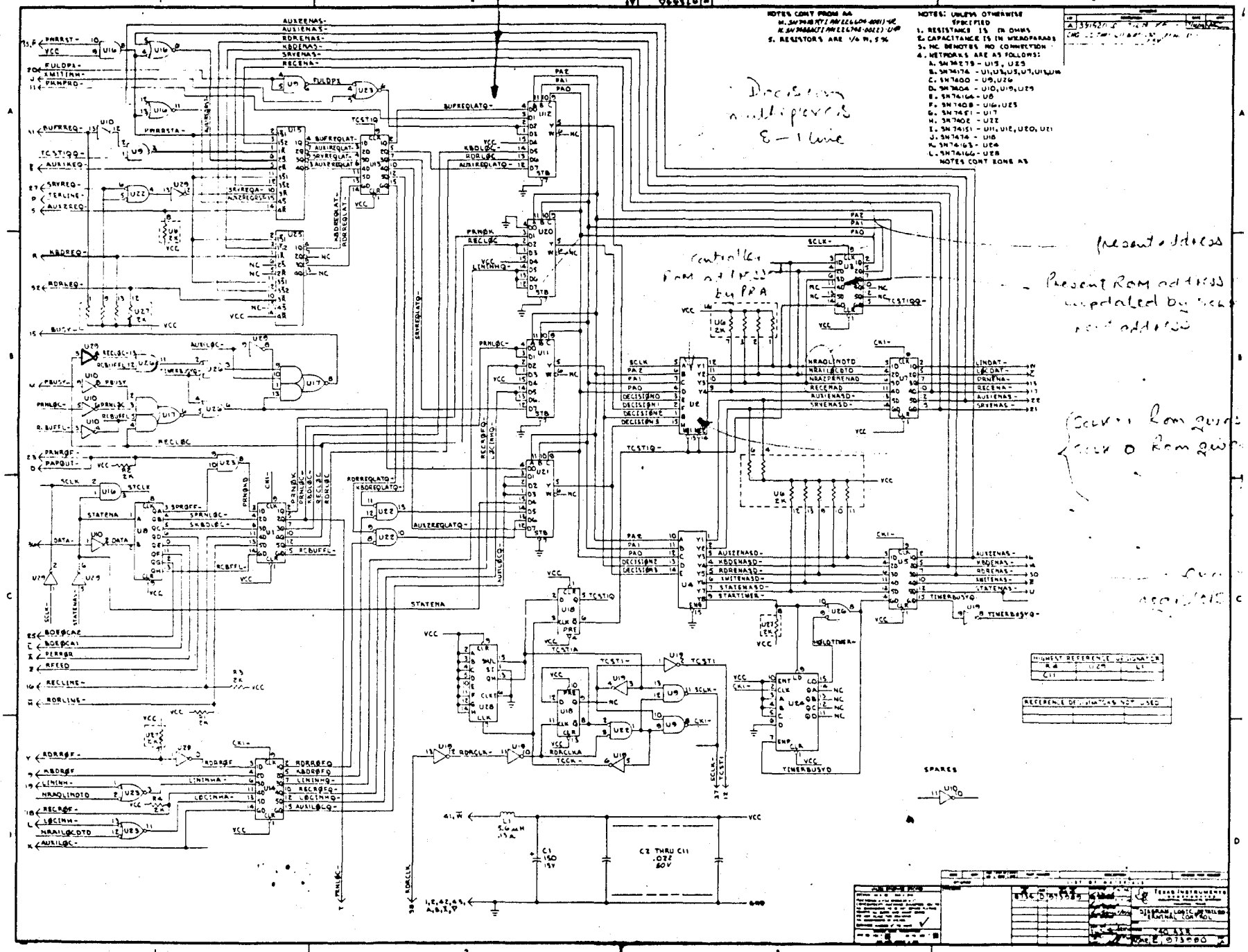
DATA-
EXTCKIN
INTCKINN
EIACTS
EIADSR
EIADCD
EIADATIN
EIABRD
TTYDATIN
XMTINH
SRVENA-
XMTENA-
XMTENAR
PWRRST-
BREAK-
SRVREQ
EIADTR
TTYDATOT
EIARTS
EIADATOT
HSPEED
CLTSED-
CARDET-
EMDATA
13.5168 MHz
SRVENAXR
SRVDAT
LATCHDAT
RESET
STOP
XMTCLK
SRVCLK
BUSYRST-
RCVHDPX-
RCVHDPX
BYCLK
BITCLK
RDRCLK
PWRCLK
BUSYRST-
PWRCLK
LINBUSY
XMTHDPX-
FULDPX-
RSTCHRTIMER-
RSTCHRTIMER
SPEED
LOW
MED
HIGH
HALF
FULL
GRD
NOTES(CONT)
5 R12 IS NOT INSTALLED IF REQUEST TO SEND MUST BE FALSE WHEN TERMINAL IS OFF LINE, REMOVE R11 & INSTALL R12
6. DOT OVER LOGIC SYMBOL INDICATES OPEN COLLECTOR
7 TO GENERATE PARITY BIT FOR TRANSMITTED DATA, INSTALL RESISTOR R17 BETWEEN J3/J4. FOR BINARY FORMAT OR TO BYPASS PARITY GENERATION, INSTALL RESISTOR R17 BETWEEN J1 & J2
8 RESISTORS R7, R18, R19, & R20 NOT USED WHEN USED WITH PROCESSOR BOARD.
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE 1/4 W, ±5%
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. NETWORKS ARE AS FOLLOWS:
4. RESISTANCE VALUES ARE IN OHMS.
REFERENCE DESIGNATIONS
USED
NOT USED
NONE
TEXAS INSTRUMENTS
971509


EIA RECEIVER
CONTD ON SHT 2
SPARES
REF DES NOT USED
R11
5288




1K RAM
IMPLIES 12K
1K PROM
2K PROM


NOTES CONT'D FROM SH 1
DENOTES OPEN COLLECTOR OUTPUTS
CONT'D FROM SH 1
973978


NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE IS IN OHMS
2. CAPACITANCE IS IN MICROFARADS
3. NC DENOTES NO CONNECTION
4. NETWORKS ARE AS FOLLOWS:
A. SN74279 - U15, U25
B. SN74174 - U1,U3,U5,U7,U11,U13
C. SN7400 - U9,U26
D. SN7404 - U10,U19,U29
E. SN74164 - U8
F. SN7408 - U16,U25
G. SN7451 - U17
H. SN7402 - U22
I. SN74151 - U11,U12, U20, U21
J. SN7474 - U18
K. SN74163 - U24
L. SN74166 - U28
NOTES CONT FROM 4A
NOTES CONT DONE AS
Decision multiplexer 8 - 1 line
Present Address
Present RAM address incremented by clock
control RAM address by PRA
SCLK 1 RAM 2 WR
CLK 0 RAM 2 WR
SPARES
HIGHEST REFERENCE DESIGNATOR
REFERENCE DESIGNATORS NOT USED
973990