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TEXAS INSTRUMENTS

TM 990

TM 990/310
I/O Expansion Module

MICROPROCESSOR SERIES™

User's Guide

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SECTION 1

INTRODUCTION

1.1 GENERAL

The TM 990/310 is a 48-bit input/output board designed for use with the TM 990/1XX series of Texas Instruments microcomputers. Figure 1-1 is a photograph of the board identifying the edge connectors and principle components of the board.

The TM 990/310 board offers the following features:

- 48 bits individually programmable as inputs or outputs; 27 of these bits may be programmed as logic-zero-sensitive interrupts, rather than inputs or outputs.
- Three negative edge-triggered interrupts and three positive edge-triggered interrupts; each of the six interrupts are edge-detected, stored, and have unique software resets. The edge inputs are pulse shaped by Schmitt trigger circuits.
- Backplane interrupt priority is determined by wires installed on two 16-pin platforms.
- Board CRU base address is changed by altering the contents of S1, a four-switch DIP.
- All 48 input/output signals may be echoed back into the CRU via STCR instructions.
- Compatible with TM 990 CRU bus.
- CRU addressing provided for up to 14 cards per system.
- In multiple card I/O systems, CRU addressing can be switch selected such that all CRU addresses are consecutive.
- Contains three programable interval timers.
- Plugs into TM 990/510 or equivalent* chassis.
- Inputs and outputs are TTL compatible.
- May be used with wire-wrap, solder, or ribbon cable edge connectors.

1.2 SPECIFICATIONS

Power requirements: +5 V, $\pm$5%, 800 mA.

Temperature Requirements:

Operating Temperature	0° C to 70° C
Storage Temperature	-65° C to 150° C

* Equivalent chassis include the TM 990/520, /530, /510A, and /520A.

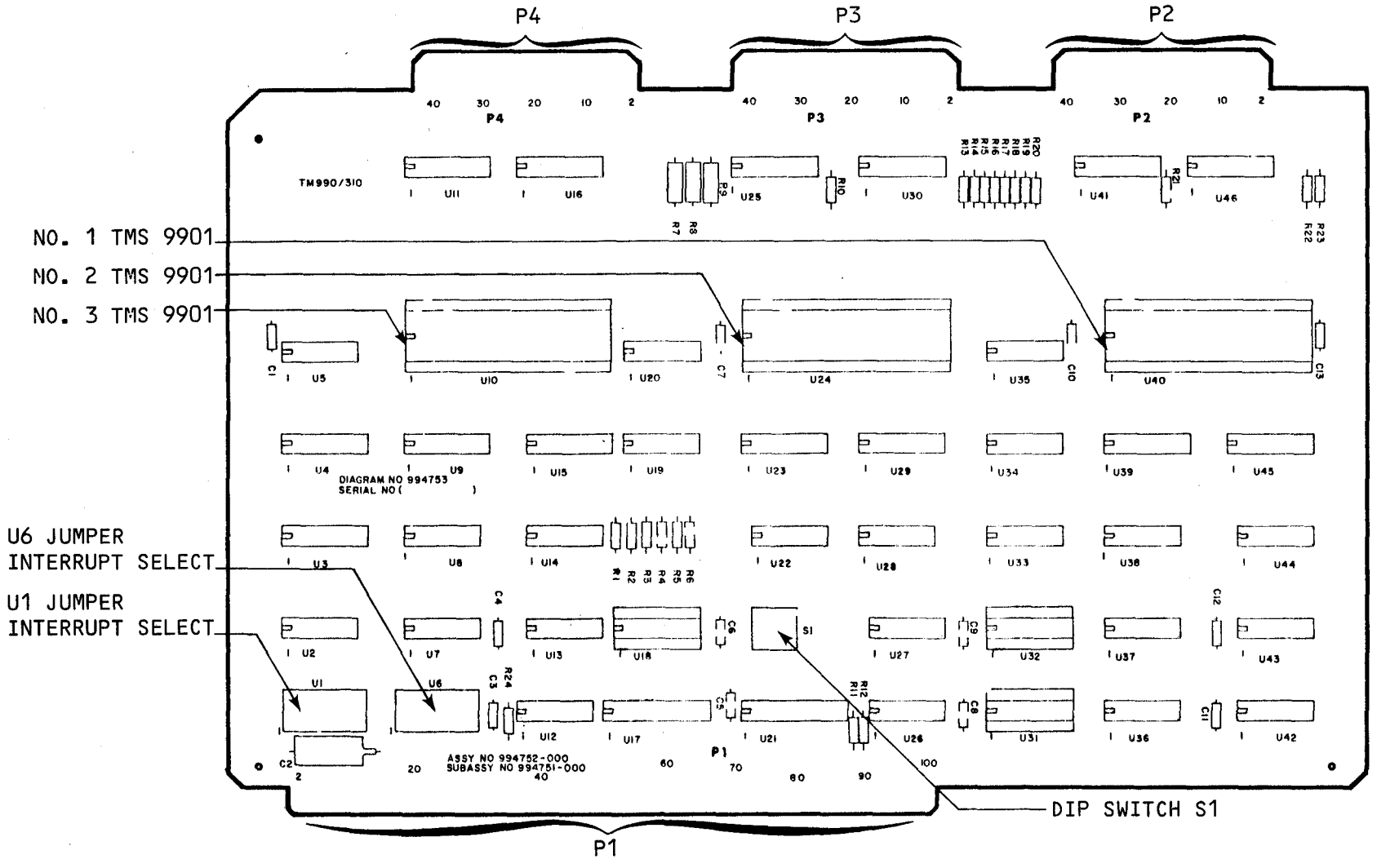


FIGURE 1-1. TM 990/310 48-I/O MODULE

Physical Characteristics:

Width:	28 cm (11 inches)
Height:	19 cm (7.5 inches)
Thickness:	0.16 cm (0.062 inch)
Component height:	12.7 mm (0.50 inch) maximum

Edge Triggered Interrupt Inputs:

Positive-going threshold voltage:	1.9 V max.
Negative-going threshold voltage:	0.5 V min.
Hysteresis:	0.4 V max.
Allowed voltage range:	-0.3 V to 7.0 V
Input current:	-2.72 mA @ V_{IN} = 0.4V
	-1.22 mA @ V_{IN} = 2.7 V

Programmed Inputs:

High-level input voltage:	2.0 V, minimum
Low-level input voltage:	0.8 V, maximum
Allowed voltage range:	-0.3 V to 7 V
Input current:	- 1.01 mA maximum @ 0.4 V

Programmed Outputs:

High-level output voltage:	2.4 V, minimum @ -300 uA
	2.0 V, minimum @ -460 uA
Low-level output voltage:	0.56 V, maximum @ 2.3 mA
Maximum user current sink:	2.2 mA

1.3 APPLICABLE DOCUMENTS

- TMS 9900 Microprocessor Data Manual
- TMS 9901 Programmable Systems Interface Data Manual (provided in Appendix E).
- TM 990/401 TIBUG Monitor Listing
- TM 990/100MA User's Manual
- Model 990 Computer, TMS 9900 Microprocessor Assembly Language Programmer's Guide (P/N 943441-9701)
- TM 990/507 Cable and 5MT System User's Guide

SECTION 2

INSTALLATION AND OPERATION

2.1 GENERAL

This section describes:

- Equipment required for TM 990/310 board operation.
- Switch array S1 on the TM 990/310 board used to select TMS 9901 CRU base address.
- Jumper platforms U1 and U6 used to select interrupt level when an interrupt occurs at one of the three TMS 9901's on the board.
- Installation of the board into a microcomputer system.
- Programs to check out board operation.

It is presumed that the user is familiar with the TMS 9901 as well as the hardware and programming aspects of the host microcomputer. This data is available in the following manuals:

- TMS 990/1XX Microcomputer User's Guide
- TMS 9901 Programmable Systems Interface Data Manual

A copy of the latter manual can be found in Appendix D.

2.2 REQUIRED EQUIPMENT

To use the TM 990/310 effectively, the user must also supply the following equipment:

- Power Supplies:

  +5 V $\pm$5%, 3 A
  +12 V $\pm$5%, 0.5 A
  -12 V $\pm$5%, 0.5 A

- Host Microcomputer: One of the TM 990/1XX series; in the following examples, the TM 990/100MA-1.
- Chassis: TM 990/510 card cage (or equivalent)
- Edge Connectors: Three 40-pin (0.1 inch centers) PCB edge connectors. Will mate to TI H421111-20 (wire-wrap), Viking 3VH20/1JN5 (solder), 3M 3464-0001 (ribbon cable), or equivalent. A three-connector kit TM 990/521, is available from Texas Instruments.
- Terminal Device: Any RS-232-C device operable at a baud rate of 110, 300, 1200, or 9600 baud or an ASR33 Teletype modified for 20 mA current loop operation.

2.3 BOARD SWITCHES, JUMPERS, CONNECTORS

2.3.1 CRU Address Selection and Switch Array S1

The three TMS 9901's on the TM 990/310 board are addressed through the system's address bus when a CRU instruction is executed (LDCR, STCR, TB, SBO, and SBZ). Before execution, a CRU software base address is placed into register 12; the resulting bits 3 to 14 (4 to 14 on the TM 990/180M) contain the CRU hardware base address as further explained in your microcomputer user's guide.

Switch S1 allows you to select the CRU hardware base address in increments of $C0_{16}$ that you can use to address a particular TMS 9901. Figure 2-1 shows the switch S1 settings and the resulting CRU hardware (B) and software base addresses. The resulting CRU base address is the one that addresses the no. 1 TMS 9901 (accessed through edge connector J2). As shown at the bottom of Figure 2-1, the other TMS 9901's are addressed using the base address plus a designated displacement.

The first 32 CRU bits addressed are bits 0 to 31 (0 to $1F_{16}$) at the TMS 9901 which select:

- Interrupt or clock mode (bit 0 select)
- Interrupt mask or clock interval (bits 1 to 15)
- Data output or input (bits 16 to 31)

Further data is available in the TMS 9901 data manual (Appendix E).

As shown in Figure 2-1, two of the next 16 bits addressed will reset edge-triggered interrupts (INT5- and INT6-) that have been triggered at the TMS 9901. INT5- is a negative edge-triggered interrupt , and INT6- a positive edge-triggered interrupt. Edge-triggered interrupts will remain active until reset by an LDCR instruction of prescribed address (e.g., a pulse at CRU base address B + 0024_{16} resets interrupt 5 at no. 1 TMS 9901 and B + 0025_{16} resets interrupt 6 at the same TMS 9901).

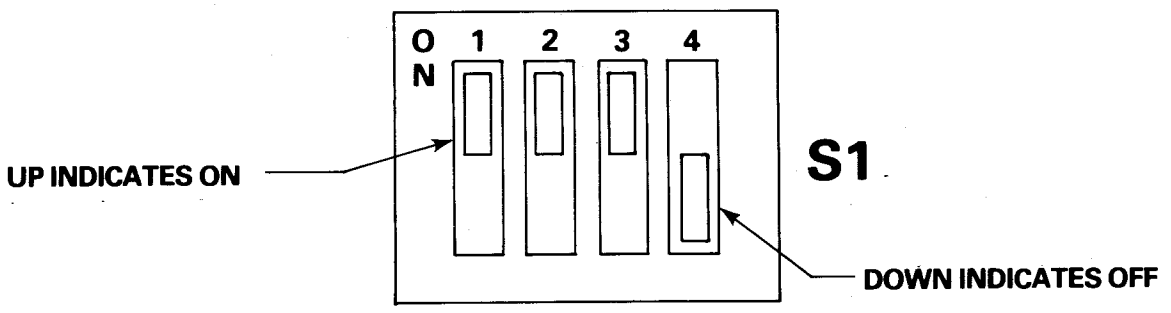
As shown in Figure 2-1, the next 16 bits can be read (echoed) in order to test a bit pattern output from the TMS 9901. The bit pattern output is stored in a buffer that can be read (using the STCR instruction) and compared to the bit pattern sent. For example, the following code will read the value output at no. 1 TMS 9901 location at CRU software base address 0200_{16} (as selected at switch S1):

```
LI      R12, >0260      Set CRU address
STCR    R1,0            Store 16-bits output in R1
```

2.3.2 Interrupt Level Selection on Jumper Plugs U1 and U6

When any interrupt is recognized at a TMS 9901 on the TM 990/310, a signal (INTREQ-) is issued from the TMS 9901 on the I/O board to the backplane and then to the TMS 9901 on the microcomputer board. There it is monitored for priority, and, if enabled, a signal is issued to the microprocessor to obtain Workspace Pointer (WP) and Program Counter (PC) values from interrupt traps in lower memory.

The user can select the interrupt level or levels (up to 3 are possible) by wiring jumpers at platforms U1 and U6, shown in Figure 1-1 in the lower left corner of the board. Note that each TMS 9901 may be jumpered to unique backplane priority levels, or all three may be jumpered to the same backplane priority level (the TM 990/310 is initially jumpered for all three TMS 9901's dedicated to backplane priority interrupt 4).

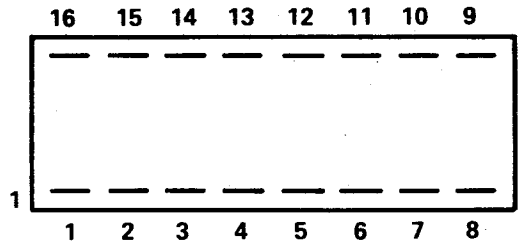


S1 SWITCH SETTINGS 1	2	3	4	EQUALS BINARY	TM 310 BOARD CRU HARDWARE (B) BASE ADDRESS (BASE 16)	CORRESPONDING REGISTER 12 CONTENTS (CRU SOFTWARE BASE ADDRESS) (BASE 16)
ON	ON	ON	ON	0	0100	0200
ON	ON	ON	OFF	1	01C0	0380
ON	ON	OFF	ON	2	0280	0500
ON	ON	OFF	OFF	3	0340	0680
ON	OFF	ON	ON	4	0400	0800
ON	OFF	ON	OFF	5	04C0	0980
ON	OFF	OFF	ON	6	0580	0B00
ON	OFF	OFF	OFF	7	0640	0C80
OFF	ON	ON	ON	8	0700	0E00
OFF	ON	ON	OFF	9	07C0	0F80
OFF	ON	OFF	ON	A	0880	1100
OFF	ON	OFF	OFF	B	0940	1280
OFF	OFF	ON	ON	C	0A00	1400
OFF	OFF	ON	OFF	D	0AC0	1580
OFF	OFF	OFF	ON	E	NOT USED	NOT USED
OFF	OFF	OFF	OFF	F	NOT USED	NOT USED

DEVICE	ADDRESSED USING CRU HARDWARE BASE ADDRESS (B) AND DISPLACEMENT	CORRESPONDING CRU SOFTWARE BASE ADDRESS R12 CONTENTS (BASE 16)	NUMBER OF BITS
No. 1 TMS 9901 (P2)	*B + 0000 to B + 001F	R12 + 0000 to R12 + 003E	32
Edge-triggered $\overline{INT5}$ reset	B + 0024	R12 + 0048	1
Edge-triggered $\overline{INT6}$ reset	B + 0025	R12 + 004A	1
Echo	B + 0030 to B + 003F	R12 + 0060 to R12 + 007E	16
No. 2 TMS 9901 (P3)	B + 0040 to B + 005F	R12 + 0080 to R12 + 009E	32
Edge-triggered $\overline{INT5}$ reset	B + 0065	R12 + 00CA	1
Edge-triggered $\overline{INT6}$ reset	B + 0066	R12 + 00CC	1
Echo	B + 0070 to B + 007F	R12 + 00E0 to R12 + 00FF	16
No. 3 TMS 9901 (P4)	B + 0080 to B + 009F	R12 + 0100 to R12 + 013F	32
Edge-triggered $\overline{INT5}$ reset	B + 00A4	R12 + 0148	2
Edge-triggered $\overline{INT6}$ reset	B + 00A5	R12 + 014A	1
Echo	B + 00B0 to B + 00BF	R12 + 0160 to R12 + 017E	16

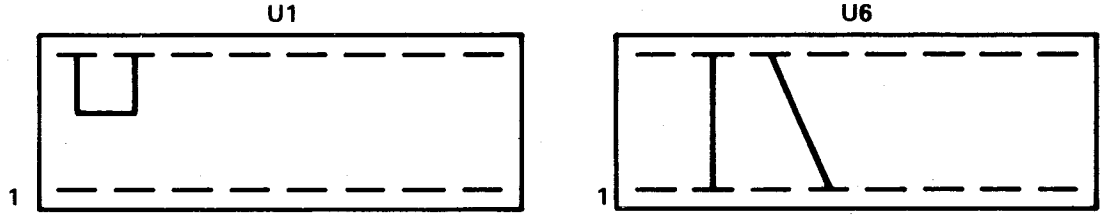
*B is the hardware base address computed in the table in the middle of this figure.

FIGURE 2-1. USE OF SWITCH S1 TO SET CRU ADDRESS MAP



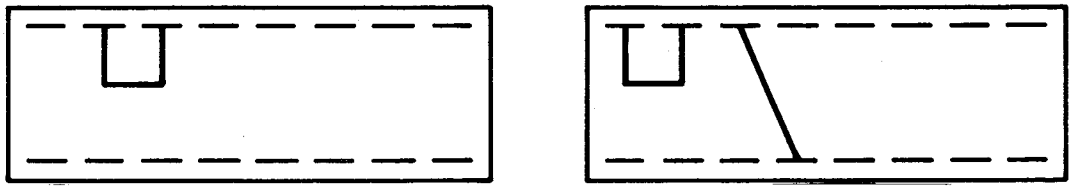
TO BACKPLANE	INT1.B	U6-1	U6-16	TMS 9901 #3 INT
	INT2.B	U6-2	U6-15	TMS 9901 #2 INT
	INT3.B	U6-3	U6-14	TMS 9901 #1 INT
	INT4.B	U6-4		
	INT5.B	U6-5		
	INT6.B	U6-6		
	INT7.B	U6-7		
	INT8.B	U6-8		
	INT9.B	U1-1	U1-16	TMS 9901 #3 INT
	INT10.B	U1-2	U1-15	TMS 9901 #2 INT
	INT11.B	U1-3	U1-14	TMS 9901 #1 INT
	INT12.B	U1-4		
	INT13.B	U1-5		
	INT14.B	U1-6		
	INT15.B	U1-7		
		U1-8		

EXAMPLE 1



Select interrupt level 4 for TMS 9901 no. 1; level 2 for TMS 9901 no. 2 and 3.

EXAMPLE 2



Select interrupt level 4 for all three TMS 9901's on I/O board.

NOTE: TM 990/310 is factory wired to priority 4 for all three TMS 9901's.

FIGURE 2-2. INTERRUPT PRIORITY JUMPER WIRING AT U1 AND U6

As shown in Figure 2-2, a wire is attached to pins 16, 15, and 14 to respectively select the interrupt level sent by the no. 1, and no. 2, and no. 3 TMS 9901's on the I/O board. Note that pins 14, 15, and 16 of U1 are connected to pins 14, 15, and 16 of U6. Thus the configuration in the second example of Figure 2-2 will cause interrupts at all three I/O board TMS 9901's to go to INT4 at the TMS 9901 on the microcomputer board. This is the configuration as wired at the factory.

As explained in the microcomputer user's guide, vector addresses have been programmed into TIBUG EPROM for interrupt traps 3 and 4 on the TM 990/100MA. The user can program these RAM locations for use as an interrupt handler as described in the microcomputer user's guide. On the TM 990/180M, vector addresses have been programmed into EPROM for interrupts 1 and 2.

2.3.3 Edge Connectors P1, P2, P3, and P4

Edge connectors P2, P3, and P4 interface directly to the I/O board TMS 9901's through onboard series resistors. TMS 9901 signatures at these connectors are listed in Table 2-1.

TABLE 2-1. EDGE CONNECTOR (P2, P3, P4) PIN ASSIGNMENTS

PIN NUMBER	SIGNATURE	
P2, P3, P4 - 20	P0	TMS 9901 I/O Signals
22	P1	
14	P2	
16	P3	
18	P4	
10	P5	
12	P6	
24	$\overline{\text{INT15}}$/P7	
26	$\overline{\text{INT14}}$/P8	
28	$\overline{\text{INT13}}$/P9	
30	$\overline{\text{INT12}}$/P10	
32	$\overline{\text{INT11}}$/P11	
34	$\overline{\text{INT10}}$/P12	
36	$\overline{\text{INT9}}$/P13	
38	$\overline{\text{INT8}}$/P14	
40	$\overline{\text{INT7}}$/P15	
6	Negative edge-triggered INT5	
8	Positive edge-triggered INT6	
1	+12V	
2	−12V	
3	+5V	
4	Spare	
All Remaining Pins	Ground	

NOTES

1. Connector P2 connects to the lowest addressed TMS 9901, P3 connects to the next addressed TMMS 9901, and P4 connects to the highest addressed TMS 9901.

2. If you want to make your own cable, be aware that the connector plugs of various vendors, including TI, do not necessarily use the numbering schemes on the board edge connector. ALWAYS refer to the board edge when wiring a connector.

TMS 9901 pins P0 to P5 act as data out or data in lines, depending on how the TMS 9901 is programmed (input or output mode).

If programmed to the interrupt mode, an active low signal to even-numbered pins 24 to 40 will cause activation of signal INTREQ- to the TMS 9901 on the microcomputer board. The level to the microcomputer board is selected by the jumpers at U1 and U6 as described in paragraph 2.3.2.

A negative-going signal to pin 6 or positive-going signal to pin 8 will also cause INTREQ- to be active.

CAUTION

The voltage at pins 1, 2, and 3 goes through 2.2 ohm, 0.5W series limiting resistors. Power in excess of this rating could destroy the resistors; thus caution should be taken to prevent excess current (250 mA maximum recommended).

Table 2-2 is a list of the signals at connector P1 which interfaces to the backplane of the TM 990/510 chassis.

TABLE 2-2. TM 990/310 CHASSIS INTERFACE CONNECTOR (P1) SIGNAL ASSIGNMENTS

P1 PIN	SIGNAL		P1 PIN	SIGNAL
57	A0.B		13	INT2.B-
58	A1.B		15	INT3.B-
59	A2.B		18	INT4.B-
60	A3.B		17	INT5.B-
61	A4.B		20	INT6.B-
62	A5.B		6	INT7.B-
63	A6.B		5	INT8.B-
64	A7.B		8	INT9.B-
65	A8.B		7	INT10.B-
66	A9.B		10	INT11.B-
67	A10.B		9	INT12.B-
68	A11.B		12	INT13.B-
69	A12.B		11	INT14.B-
70	A13.B		14	INT15.B-
71	A14.B		3	+5V
72	A15.B		4	+5V
24	ϕ3.B-		97	+5V
87	CRUCLK.B-		98	+5V
30	CRUOUT.B		1	GND
29	CRUIN.B		2	GND
88	IORST.B-		99	GND
16	INT1.B-		100	GND

2.4 INSTALLATION

The following procedure is for a TM 990/310 module used with a TM 990/100MA-1 CPU (with TIBUG installed on EPROM):

a. Attach jumper J1 to the P1-18 position on the TM 990/100MA board. This provides interrupt level 4 from the backplane to the TM 990/310.

b. Wire the voltages into the terminal strip in the chassis, switch on the power supplies, and check the voltages. Switch off power. Set all switches on S1, the dual in line package (DIP) on the TM 990/310 board, to the ON positions (CRU software base address of 0200_{16}).

c. Install the TM 990/100MA-1 and TM 990/310 circuit boards in the chassis. Attach the terminal connector to J2 on the TM 990/100MA-1. Note that the TM 990/310 board has only one ejector in order to accomodate three external connectors.

d. Power up the terminal device and switch on the power supplies.

e. Actuate the RESET switch on the TM 990/100MA-1 board and press the letter A key or a carriage return (CR) on the terminal device. TIBUG, the debug monitor program, will output an initialization message.

2.5 BOARD CHECKOUT

Software routines that can be loaded and executed by the user, using the TIBUG monitor, are provided in Section 5.

SECTION 3

THEORY OF OPERATION

3.1 GENERAL

This section describes the theory of operation for the TM 990/310 I/O board. The block diagram in Figure 3-1 defines the basic blocks that comprise the TM 990/310.

3.2 CRU ADDRESS DECODING

Figure 3-2 is a schematic of CRU address decoding. The following terms are generated by the CRU address coding

MUXEN0- MUXEN1- MUXEN2- MUXEN3- MUXEN4- MUXEN5-	Echo multiplexer enables
9901SEL.0- 9901SEL.1- 9901SEL.2-	TMS 9901 enables
IR.00- IR.01- IR.02- IR.03- IR.04- IR.05-	Buffered interrupt resets

These terms are combinational functions of the address lines, and vary with the settings of switch S1. Three 74S287's generate the terms SEL1, SEL2, and SEL3 which provide enable inputs to the combinational logic that generates the device enables.

The address lines to the 74S287's are provided by the four switch outputs and backplane address lines A5 through A8. Individual 74S287's are enabled, depending on the state of address lines A3 and A4. Since each switch setting represents 192 ($C0_{16}$) CRU addresses, the 74S287's are programmed to generate three outputs (SEL1, SEL2, SEL3) which individually enable 64 different CRU addresses. Each group of 64 encompasses one TMS 9901, the I/O echo and interrupt resets.

3.3 TMS 9901 LOGIC

The three TMS 9901's are enabled by CRU address decoding logic outputs. As shown in Figure 3-3, the select inputs, S0 through S4, are connected to backplane address lines A10, A11, A12, A13, and A14. These TMS 9901 inputs select the individual data bits and control functions within the TMS 9901.

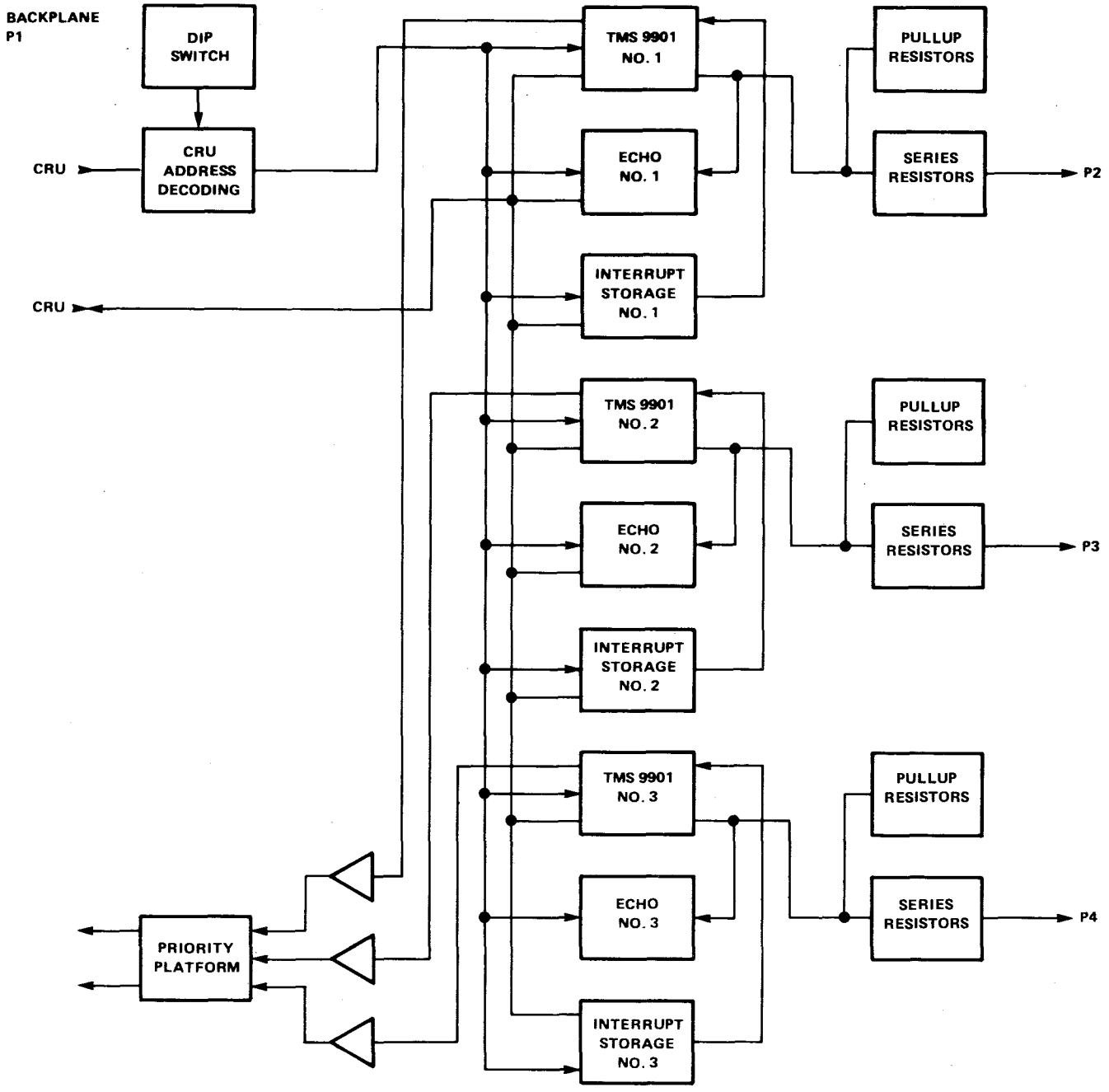


FIGURE 3-1. TM 990/310, 48-BIT INPUT/OUTPUT BOARD SIMPLIFIED BLOCK DIAGRAM

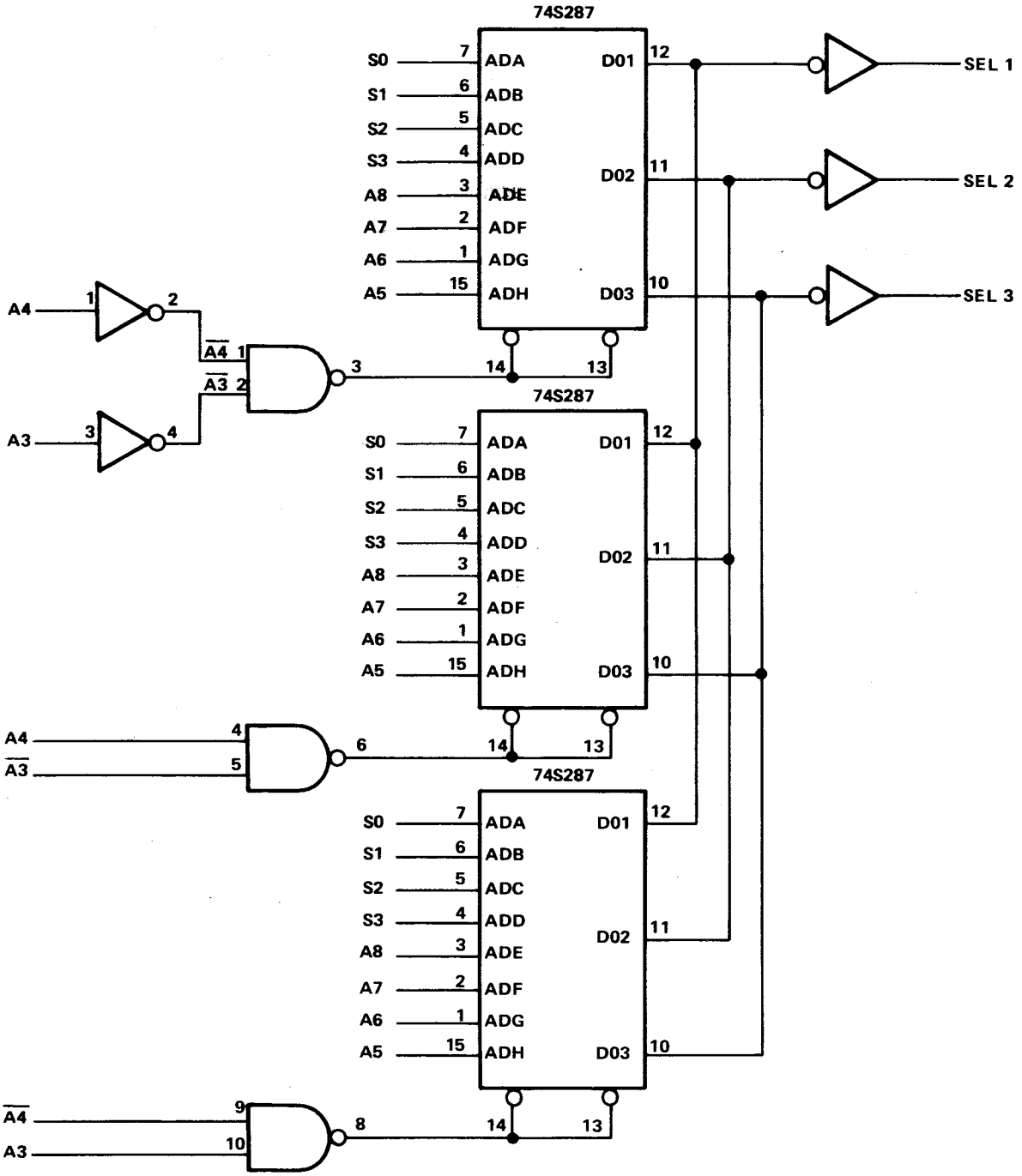


FIGURE 3-2. CRU ADDRESS DECODING

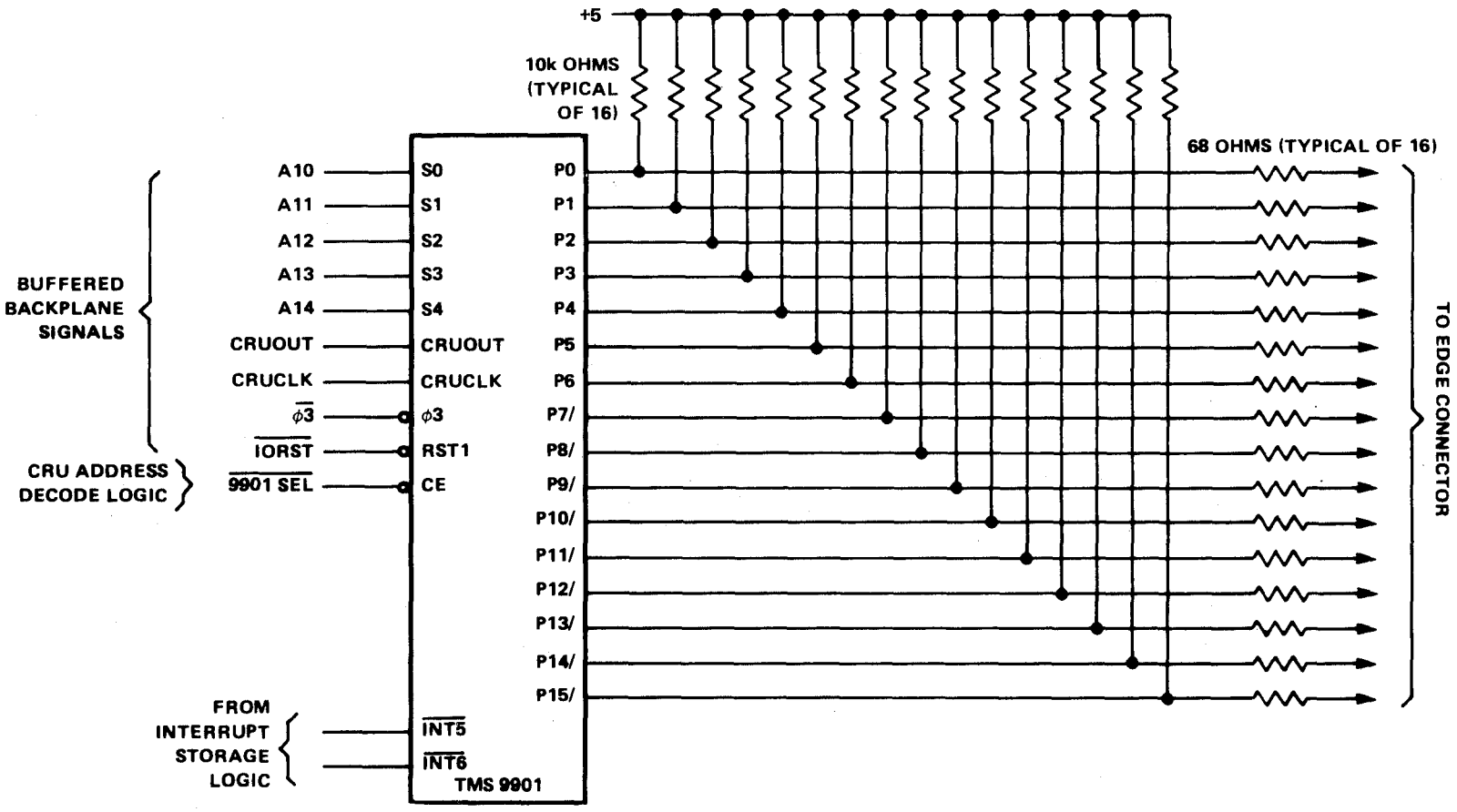


FIGURE 3-3. TMS 9901 LOGIC (TYPICAL OF 3)

The CRU interface signals CRUOUT, CRUCLK, and CRUIN control input and output between the TMS 9901 and the CRU. The INTEQ- output of each TMS 9901 is an input to the 7407 open collector buffers. The backplane reset signal is connected to each TMS 9901 reset input, and the backplane phase-1 clock is connected to each TMS 9901 clock input.

Each of the 16 I/O bits of each TMS 9901 is connected to a 10K ohm pullup resistor and an echo multiplexer input as well as a 68-ohm series resistor connected to the appropriate pin of one of the three board edge connectors. The INT5- and INT6- inputs of each TMS 9901 are connected to latched interrupt lines.

It should be noted that since the TMS 9901 interfaces to the serial CRU, the TMS 9901 lines, when outputting data, will assume their output state one bit at a time.

3.4 DATA ECHO LOGIC

The data echo logic shown in Figure 3-4 is implemented with six 74LS251 multiplexers. Each multiplexer is enabled by a CRU address decoding output. The appropriate data bit is switched through the multiplexer onto the CRUIN line by the state of backplane address bits A14, A13, and A12.

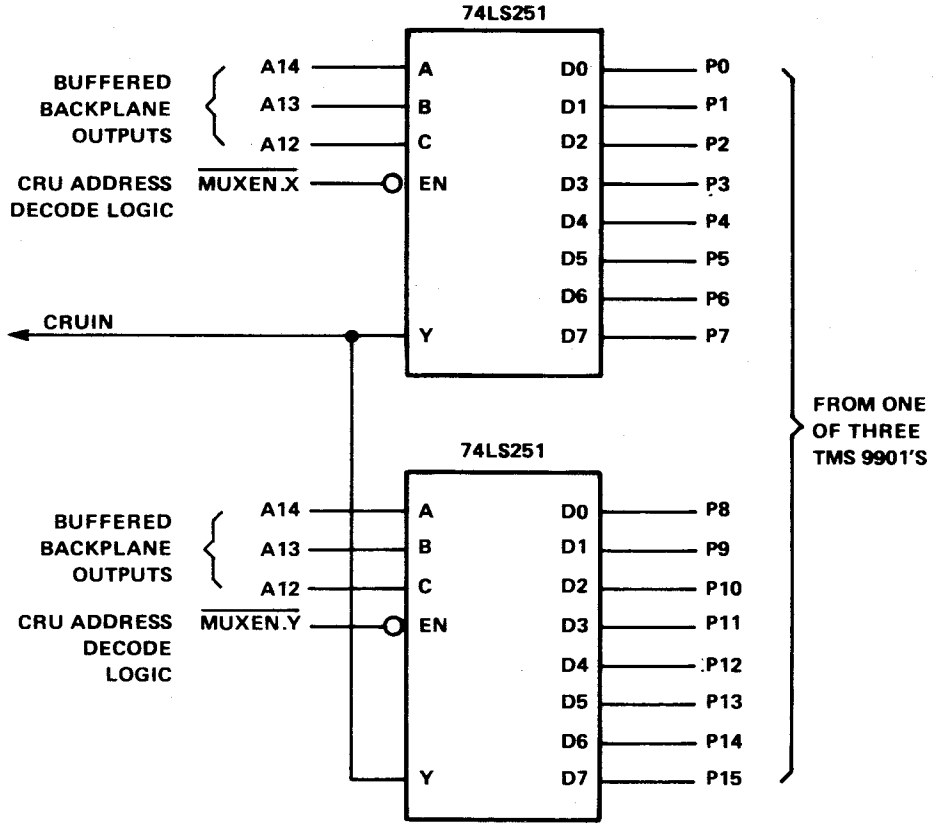


FIGURE 3-4. ECHO LOGIC (TYPICAL OF 3 CIRCUITS)

3.5 INTERRUPT BUFFER LOGIC

The interrupt buffers are composed of 74LS74 D flip-flops as shown in Figure 3-5. Each interrupt input from the appropriate edge connector is pulse shaped through 74LS132 Schmitt trigger circuits. For the three negative-edge INT5- inputs, the 74LS132 output provides the clock input to the 74LS74. The D input is tied high and the CLEAR input is the logical NOR of the appropriate software reset bit and the backplane reset signal. The 74LS74 clock inputs for the positive-edge triggered INT6- interrupts are 74LS04 ouputs. The 74LS04 input is provided by the Schmitt trigger output. Each TMS 9901 INT5- and INT6- input is provided by the false 74LS74 outputs.

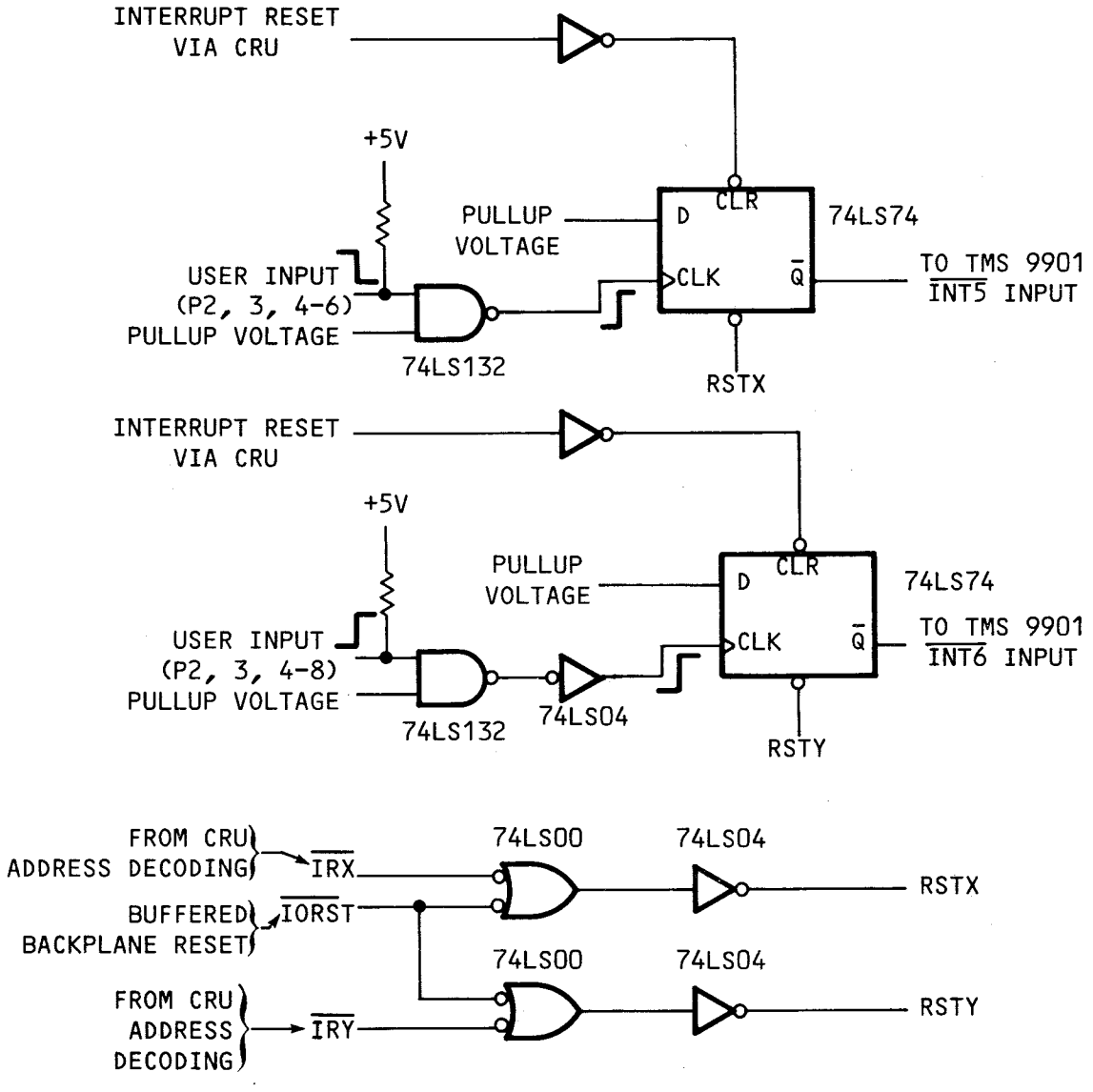


FIGURE 3-5. INTERRPUT STORAGE LOGIC

3.6 INTERRUPT PRIORITY LOGIC

The three 7407 open collector interrupt outputs are connected to two 16-pin platforms as shown in Figure 3-6. Wires installed on these platforms determine the backplane priority of the three TMS 9901 interrupts. All three TMS 9901 interrupts are initially jumpered to interrupt priority level 4.

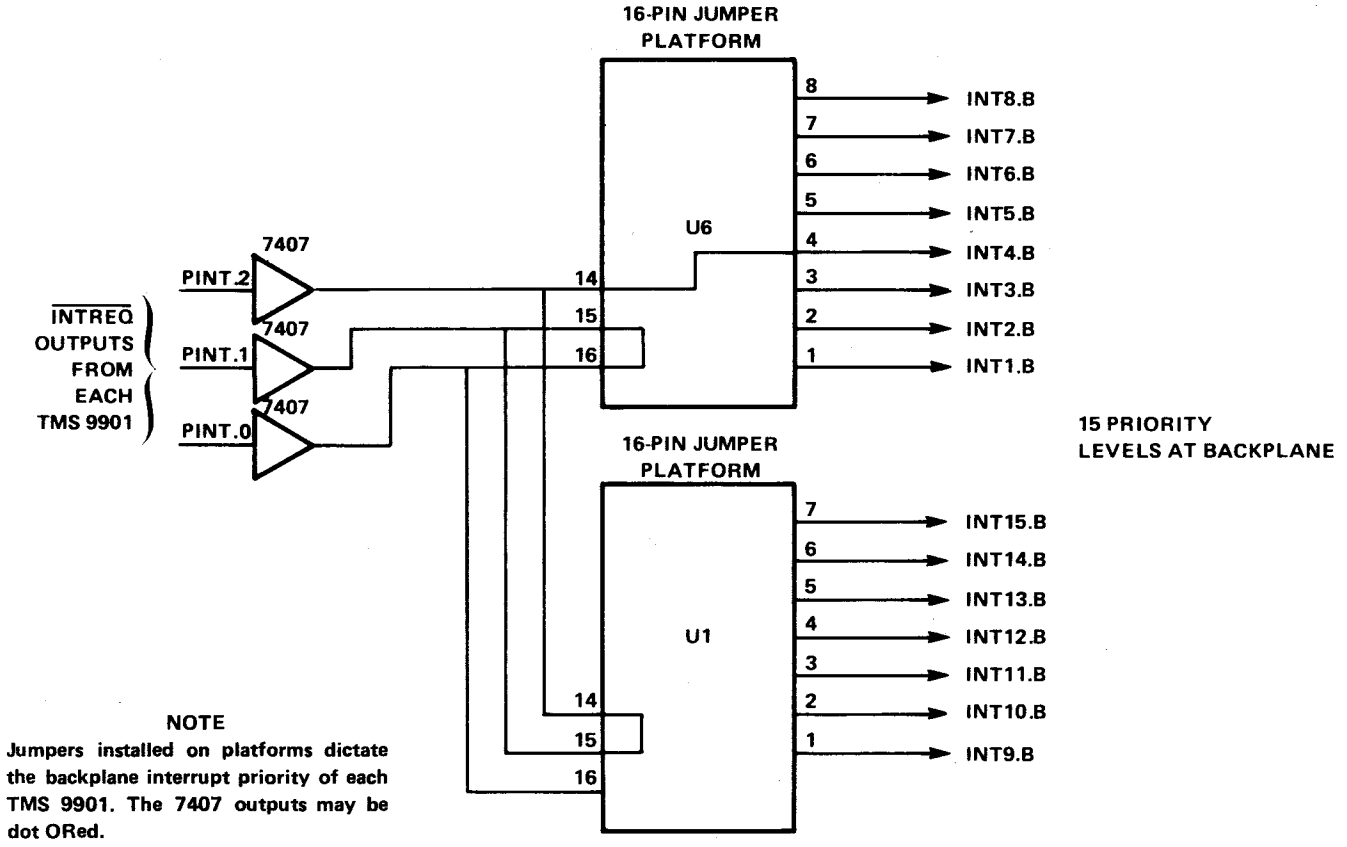


FIGURE 3-6. INTERRUPT PRIORITY LOGIC

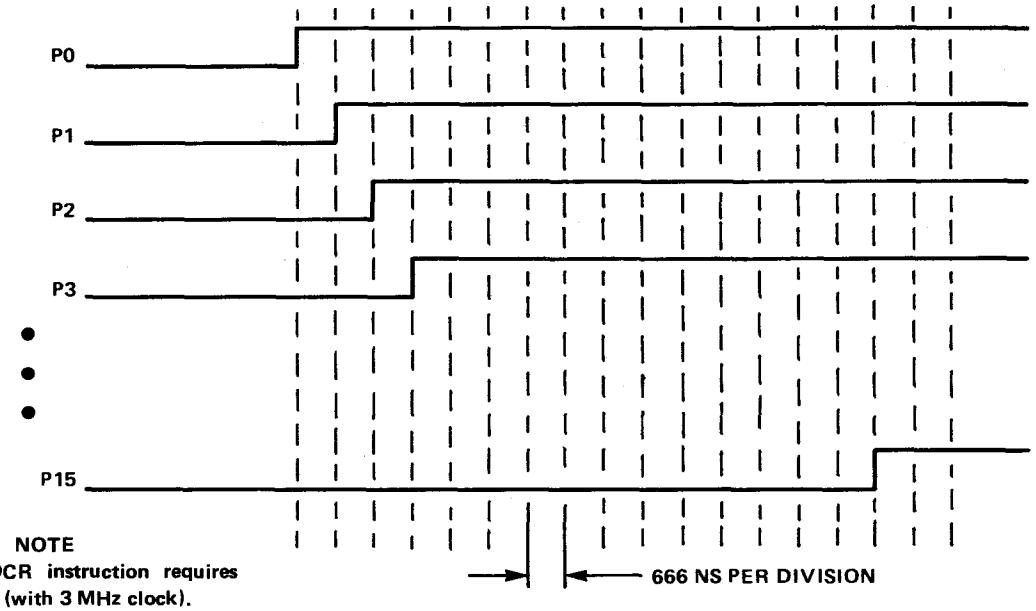
3.7 HARDWARE INTERFACE

The TM 990/310 user interface is implemented through three identical 40-pin edge connectors. (See Section 1.2 for signal characteristics.) Each of these connectors provide data I/O, interrupt inputs, and power (Table 2-1 lists these functions).

3.7.1 TMS 9901 I/O Lines

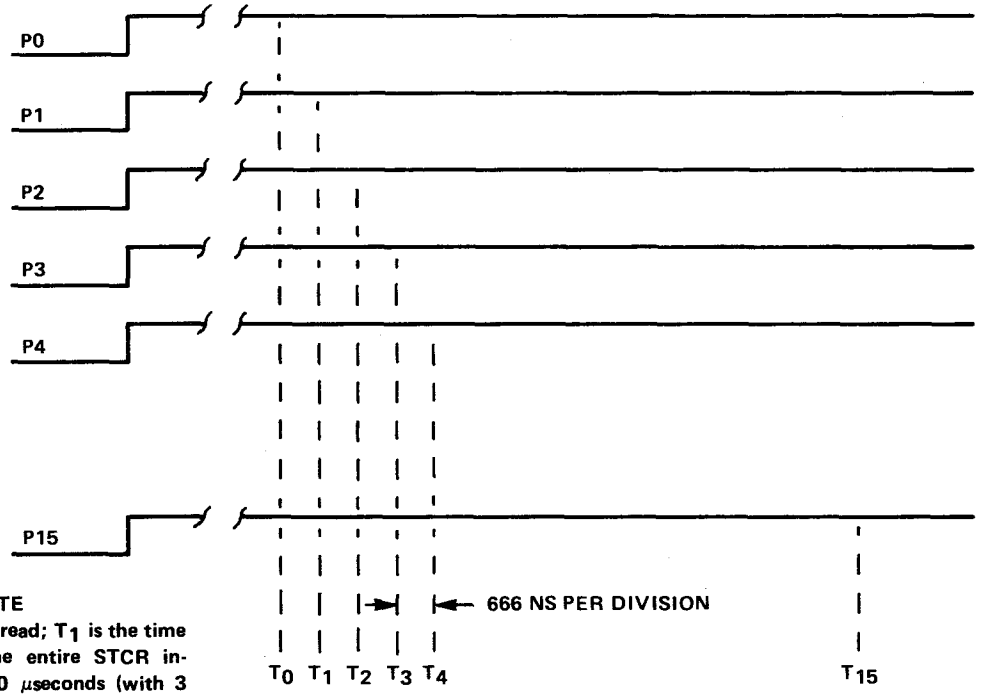
Sixteen TMS 9901 lines are individually programmable as inputs or outputs. Nine of these lines (INT15/P7 to INT7/P15) may be programmed as either unbuffered, logic-zero-activated interrupts or as inputs or outputs. A TMS 9901 I/O line, when in output mode, buffers the data output from memory and this data remains stable until changed. Since the TMS 9901 interfaces through the serial CRU, the I/O lines programmed as outputs assume their programmed state in serial fashion if data is output via a LDCR instruction that addresses successive bits.

The timing diagram in Figure 3-7 illustrates the timing for an LDCR utilizing all 16 I/O lines as outputs. Data input via the TMS 9901 I/O lines is accepted serially, one bit at a time; therefore, since there is no input data storage, the system timing must ensure that the input data remains stable until the software has read the data via a TB or STCR instruction. Figure 3-8 illustrates the timing for a 16-bit STCR operation.



NOTE
The entire LDCR instruction requires 17.33 μseconds (with 3 MHz clock).

FIGURE 3-7. TM 990/310 OUTPUT TIMING FOR LDCR WITH 16 BITS OF ONE'S



NOTE
T_0 is the time P_0 is read; T_1 is the time P_1 is read, etc. The entire STCR instruction requires 20 μseconds (with 3 MHz clock).

FIGURE 3-8. TM 990/310 INPUT TIMING FOR STCR READING 16 BITS OF ONE'S

3.7.2 Edge-Triggered Interrupts

There is one positive edge-triggered (connector pin 8) interrupt and one negative-edge triggered (connector pin 6) interrupt. These interrupt lines pass through Schmitt trigger circuits.

3.7.3 Power Outlets at Connectors

5V, 12V, and -12 V are available at the connectors. Each voltage is in series with a 2.2 ohm, 0.5 watt resistor to limit maximum current drawn from these lines.

CAUTION

Excessive current drawn from any of these supplies will cause a significant voltage drop across the resistor or, if large enough, will destroy the resistor. If the user wishes to utilize current from tnese voltages, the required current must be added to the specified value for the appropriate backplane power supply. User circuits must allow for the resulting voltage drop across these resistors.

SECTION 4

APPLICATIONS

4.1 GENERAL

For the user requiring high ouput power drive or input/output optical isolation, the TM 990/512 prototyping board may be utilized for the required circuitry.

4.2 OUTPUT SIGNAL CONDITIONING, MEDIUM POWER

This is shown in Figure 4-1. For TM 990/310 outputs requiring current drive greater than 2.6 mA but less than 40 mA, the SN7406 hex open collector inverting buffer is recommended. Note that this device will withstand a maximum pullup voltage of 30 volts. A typical application of the SN7406 is driving LED's.

To condition TM 990/310 data bits 0 through 5 as buffered outputs, the circuitry shown in Figure 4-1 is recommended.

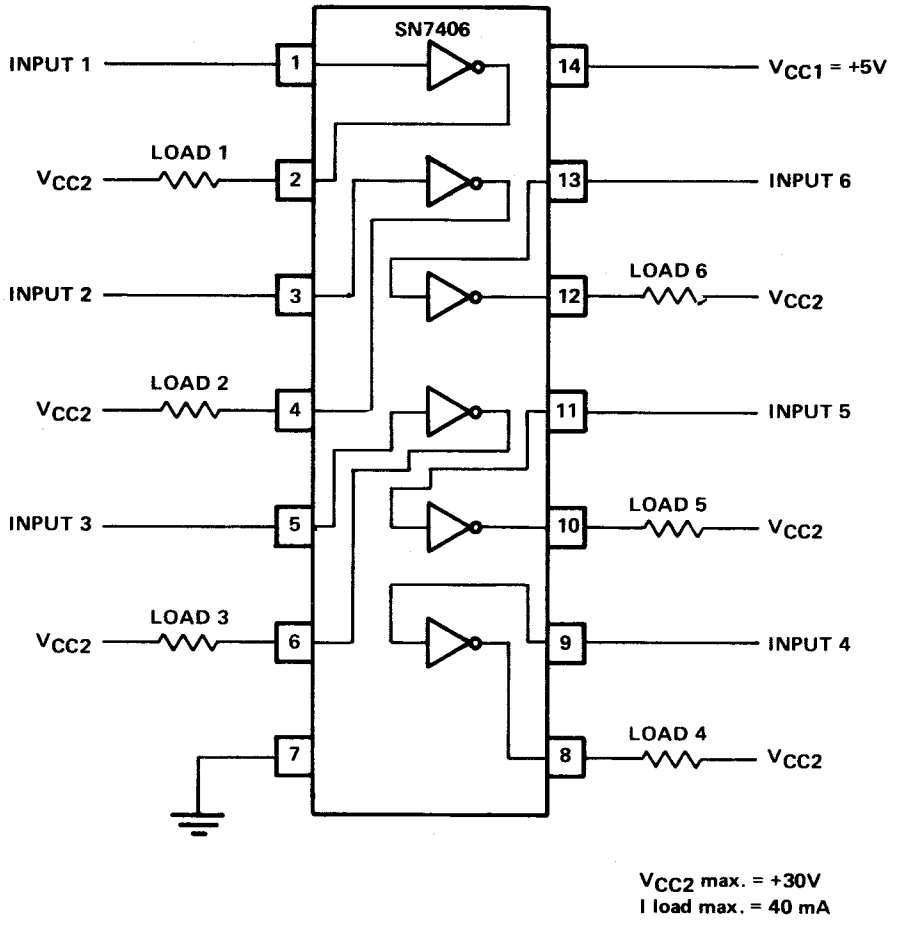


FIGURE 4-1. MEDIUM-POWER OUTPUT SIGNAL CONDITIONING CIRCUIT

4.3 OUTPUT SIGNAL CONDITIONING, HIGH POWER

For TM 990/310 outputs requiring more current drive than supplied by the SN7406 but less than 300 mA, the SN75460 open collector power buffer is recommended. The device will withstand a pullup voltage of 30 volts.

To drive 24-volt relays with TM 990/310 data bits 0 and 1, the circuitry shown in Figure 4-2 is recommended. The 19 V Zenier diode prevents damage to the SN75460 if the 5V supply is inactive while V_{cc2} is active.

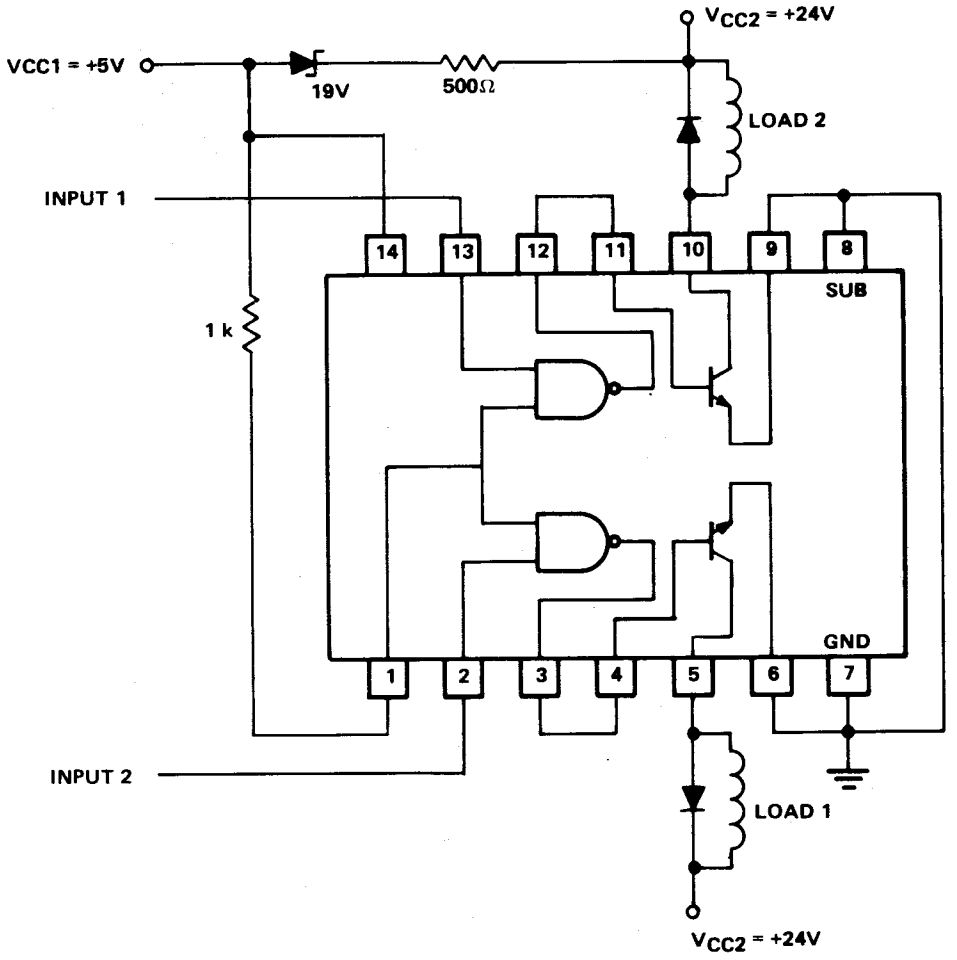


FIGURE 4-2. HIGH POWER OUTPUT SIGNAL CONDITIONING CIRCUIT

4.4 OUTPUT SIGNAL CONDITIONING, OPTICAL ISOLATION

For the user who requires TM 990/310 output isolation, the TIL 111 optical coupler is recommended for current output drive up to 20 mA. If more current drive is required, the optical coupler output must drive a buffer circuit such as the SN75460 to provide the current drive. It should be noted that the optical coupler output breakdown voltage is 30 volts.

Figure 4-3 illustrates a 20 mA optically isolated circuit. To condition TM 990/310 data bit 0 as an optically-coupled 300-mA output, the circuitry illustrated in Figure 4-4 is recommended.

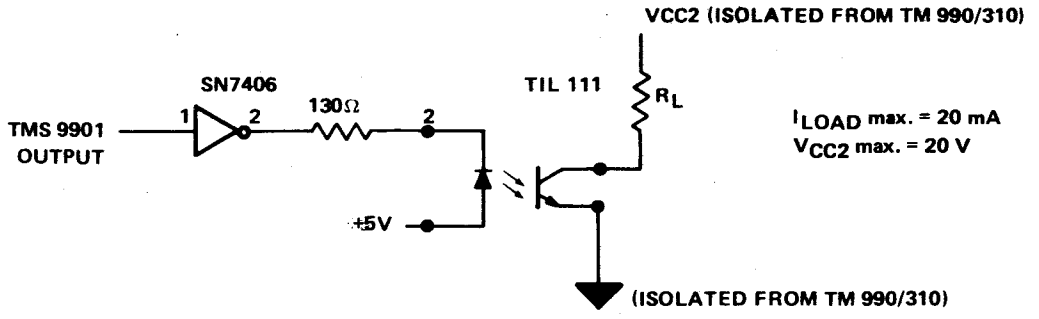


FIGURE 4-3. MEDIUM POWER OPTICAL ISOLATOR CIRCUIT

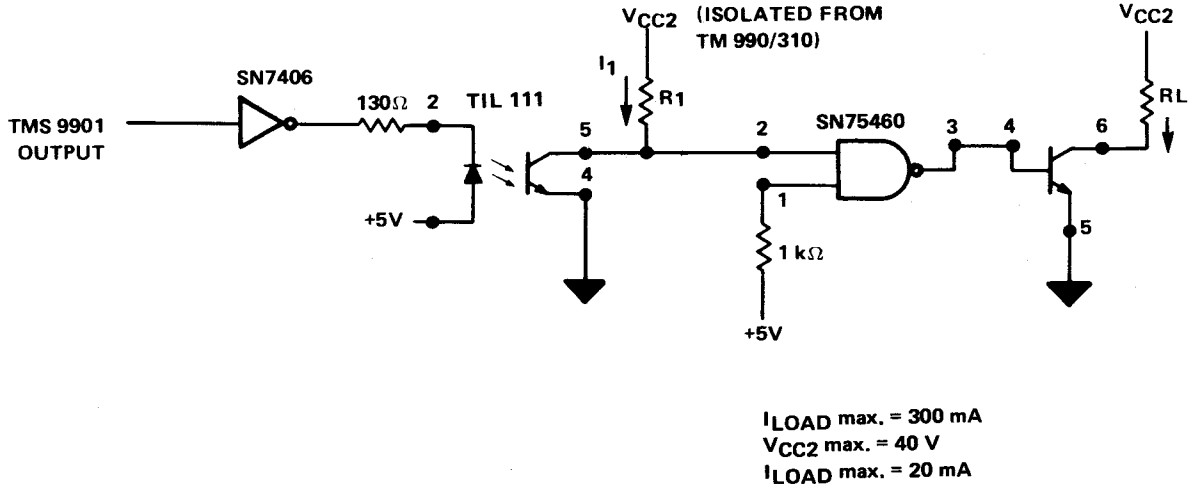


FIGURE 4-4. HIGH POWER OPTICAL ISOLATOR CIRCUIT

4.5 LOGIC TESTING

The TM 990/310 provides an ideal method to check circuit boards and other logic networks. The diagram in Figure 4-5 illustrates a circuit board tester with the capability to generate and check a total of 96 bits. For example, the tester could be programmed to output patterns on 80 pins and check resulting signals on 16 pins. A typical software sequence would be as follows:

a. Set all 96 bits (all three TMS 9901's) to input mode (set bit 15, RST2, to zero at each TMS 9901).

b. Output a test pattern to the selected 80 bits (outputting data to a bit automatically switches the bit to output mode).

c. Echo the output data, and verify that no output bits are shorted on the board being tested.

d. Input the resulting output signals from the board being tested, and compare for valid operation.

e. Repeat steps b, c, and d for as many test patterns as required.

Note that this test configuration will provide 2.2 mA per bit to the board under test. If more current drive is required, high current amplifiers should be implemented on a TM 990/512 prototyping board.

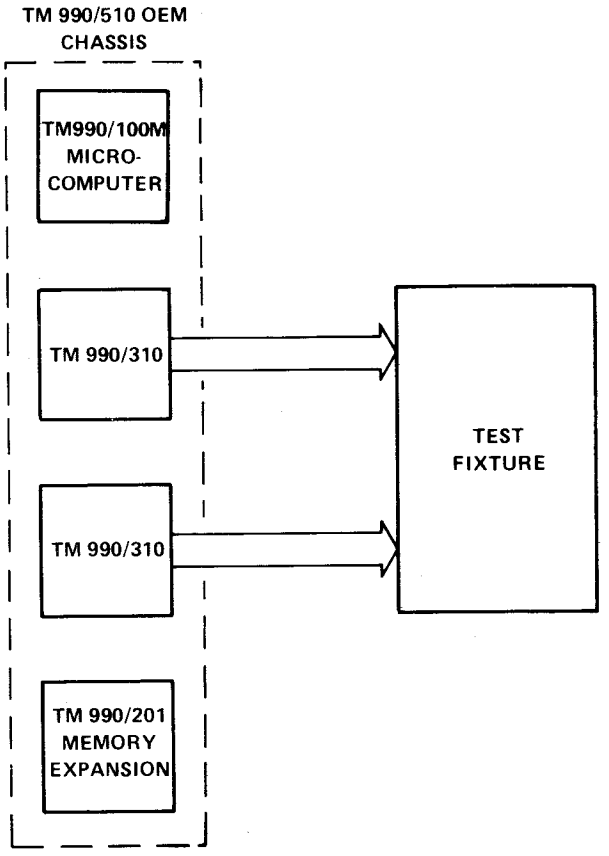


FIGURE 4-5. TYPICAL TESTING CONFIGURATION

4.6 5MT INPUT/OUTPUT SYSTEM

For industrial automation applications involving programmable control of ac and dc switches, solenoid valves, or pilot lights, the TM 990/310 will interface to 5MT I/O modules installed on a mounting baseplate. The 5MT system features the following characteristics:

- 3.8 kVdc optical coupler isolator
- LED indicator lights
- Plug-in modules
- Terminal strip on mounting baseplate for field-wired devices

- Designated to meet UL50B spacing requirements
- Meets NEMA ICS2-230 noise immunity standard for industrial controls and MIL-STD-461A, conducted and radiated susceptibility
- Module-to-module isolation

The 5MT uses a baseplate which may contain up to 16 plug-in modules. Connection between the TM 990/310 and 5MT is by a TM 990/507 cable as shown in Figure 4-6. Further information is available in the TM 990/507 and 5MT System User's Guide.

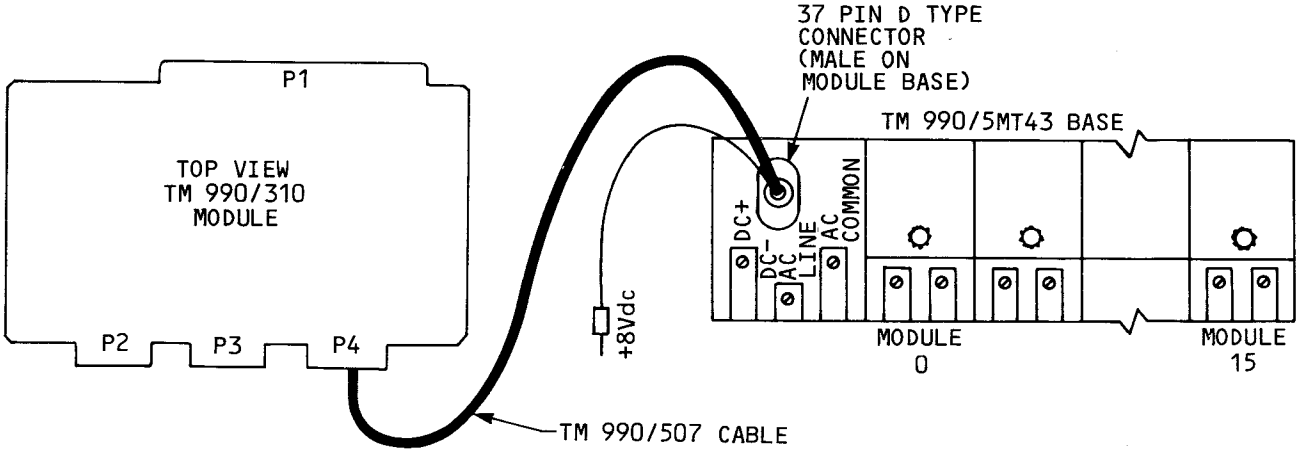


FIGURE 4-6. 5MT CIRCUITRY

- 5MT14-30CL DC Output Module - enables the TM 990/310 to control high power dc outputs.
- 5MT12-40AL AC Output Module - enables the TM 990/310 to control high power ac outputs.
- 5MT13-D03L DC Input Module - converts high voltage dc inputs to voltage inputs compatible with the TM 990/310.
- 5MT11-A05L AC Input Module - converts high voltage ac inputs to voltage inputs compatible with the TM 990/310.

The following operational characteristics must be considered when using the 5MT module:

a. The reset signal (from the logical OR of power-up reset, the RESET switch on the microcomputer board, or the RSET external instruction) will force all 48 I/O bits to the high state; therefore, all 5MT outputs will be initially active. The user who finds this feature undesirable may use an output-data-clear instruction in the reset interrupt subroutine. This would require the user to modify TIBUG, the debug monitor, or replace the TIBUG entirely.

b. The user may supply a 7-9 volt V_{CC2} voltage.

Table 4-1 indicates the requirements for the cable between the TM 990/310 and the 5MT baseplate. Further information on the 5MT series may be obtained from:

Texas Instruments Incorporated
Industrial Controls
34 Forest
Attleboro, MA. 02703

TABLE 4-1. 5MT CONNECTOR WIRING

SIGNAL		5MT D CONNECTOR	TM 990/310 EDGE CONNECTOR
Data Bit/Module	5	1	10
Data Bit/Module	4	2	18
Data Bit/Module	2	3	14
Data Bit/Module	0	4	20
Data Bit/Module	7	5	24
Data Bit/Module	9	6	28
Data Bit/Module	11	7	32
Data Bit/Module	13	8	36
Data Bit/Module	15	9	40
Ground/Module	2	10	13
Ground/Module	0	11	19
Ground/Module	5	12	9
Ground/Module	7	13	23
Ground/Module	9	14	27
Ground/Module	11	15	21
Ground/Module	13	16	35
Ground/Module	15	17	39
Ground/Module	NC	18	–
Ground/Module	NC	19	–
Ground/Module	NC	20	–
Data Bit/Module	3	21	16
Data Bit/Module	1	22	22
Data Bit/Module	6	23	12
Data Bit/Module	8	24	26
Data Bit/Module	10	25	30
Data Bit/Module	12	26	34
Data Bit/Module	14	27	38
Ground/Module	3	28	15
Ground/Module	1	29	21
Ground/Module	4	30	17
Ground/Module	6	31	11
Ground/Module	8	32	25
Ground/Module	10	33	29
Ground/Module	12	34	33
Ground/Module	14	35	37
VCC2		36	–
AC Common		37	–

NOTE: 5MT D CONNECTOR IS AMP 205713-1

SECTION 5

TM 990/310 PROGRAMMING

5.1 GENERAL

This section describes how to use the CRU to access the TM 990/310 and how to do the following:

- Set and use input and output
- Use the clock
- Use interrupts

5.2 PROGRAMMING CONSIDERATIONS

The following sections contain points which should be kept in mind while writing software for the TM 990/310 or while studying the examples.

5.2.1 Input/Output

The 16 I/O pins of the TMS 9901 will be set to the input mode by any of the following:

1. Activating the RESET switch on the microcomputer board (TM 990/1XX).
2. Completion of a powerup reset.
3. Execution of the RESET external instruction.
4. Writing a zero to CRU bit 15 of a TMS 9901 while it is in the clock mode.

All 48 I/O bits on the TM 990/310 will be reset by 1, 2 or 3 above. Only one specified TMS 9901 will be reset by number 4 above.

Bits are set as output bits by writing a value to them. Once addressed as outputs, bits remain outputs until reset.

Since all 48 I/O bits have pullup resistors, all bits wired as outputs (to relays, solenoids, LED's, etc.) will be put in the logic one state by any reset condition, until changed by user software.

CAUTION

Once a bit is set as an output, do not attempt to use it as an input before it is reset or the output buffers may be damaged.

5.2.2 Interrupts

At each P2, P3 and P4 connector, nine of the 16 I/O lines can be used as logic zero interrupts (active low). These are the INT7-/P15 through INT15-/P7 lines at the TMS 9901.

The TMS 9901 responds to a negative-edge-triggered interrupt at its INT5- input and a positive-edge-triggered interrupt at its INT6- input. The edge-triggered interrupts, levels 5 and 6 of each TMS 9901, must be software reset with CRU output instructions (see Table 5-1).

NOTE

INT1-, INT2-, INT3-, and INT4- to each TMS 9901 are unused. (INT5- and INT6- are edge-triggered interrupts, and INT7- to INT15- are shared with I/O ports P15 to P7 respectively.)

A backplane reset or execution of the RSET external instruction resets all edge-triggered interrupts and sets all three TMS 9901's to input mode.

Jumper platforms U1 and U6 are wired at the factory so that all interrupts at P2, P3 and P4 will result in a level 4 interrupt input to the TMS 9901 on the microcomputer board. It might be advantageous, from a software point of view, to have the individual TMS 9901's dedicated to three different interrupts. They can be changed as explained in paragraph 2.3.2.

The interrupt levels of the three TMS 9901's should not be confused with backplane priority. Each TMS 9901 has a maximum of fifteen interrupt levels (four are always unused) which may be enabled or disabled by the TM 990/310 software. Backplane priority refers to the TMS 9900 priority levels. For example, all interrupt levels of the TM 990/310 are initially wired to backplane priority 4 (connect to bus pin INT4-).

5.3 EXAMPLE PROGRAMS

The following switch S1 settings are assumed for all of the following examples:

	1	2	3	4	
Switch No's =	ON	ON	OFF	ON	(Hexadecimal)

This setting corresponds to CRU base addresses (hexadecimal) as follows:

Port	TMS 9901	Hardware Base Address	Software Base Address
P2	TMS 9901 No.1	0280	0500
P3	TMS 9901 No.2	02C0	0580
P4	TMS 9901 No.3	0300	0600

A complete CRU map of the three ports is given in Table 5-1.

NOTE

Each port uses an address space of 64 CRU bits. As shown in Table 5-1, port addresses are contiguous with port P2 the lowest address followed by P3 which is followed by P4.

TABLE 5-1. CRU MAP (SHEET 1 OF 2)

Software Displacement$_{16}$[1]						
TMS 9901 No.1 (P2)	TMS 9901 No.2 (P3)	TMS 9901 No.3 (P4)	P2/P3/P4 Pin No.	CRU[2] Bit	CRU[3] Read	CRU[5] Write
0	80	100	-	0	Control Bit	Control Bit
2	82	102	-	1	- /CLK1	MASK1/CLK1
4	84	104	-	2	- /CLK2	MASK2/CLK2
6	86	106	-	3	- /CLK3	MASK3/CLK3
8	88	108	-	4	- /CLK4	MASK4/CLK4
A	8A	10A	6	5	INT5/CLK5	MASK5/CLK5
C	8C	10C	8	6	INT6/CLK6	MASK6/CLK6
E	8E	10E	40	7	INT7/CLK7	MASK7/CLK7
10	90	110	38	8	INT8/CLK8	MASK8/CLK8
12	92	112	36	9	INT9/CLK9	MASK9/CLK9
14	94	114	34	10	INT10/CLK10	MASK10/CLK10
16	96	116	32	11	INT11/CLK11	MASK11/CLK11
18	98	118	30	12	INT12/CLK12	MASK12/CLK12
1A	9A	11A	28	13	INT13/CLK13	MASK13/CLK13
1C	9C	11C	26	14	INT14/CLK14	MASK14/CLK14
1E	9E	11E	24	15	INT15/INTREQ	MASK15/RST2-
20	A0	120	20	16	IN0	OUT0
22	A2	122	22	17	IN1	OUT1
24	A4	124	14	18	IN2	OUT2
26	A6	126	16	19	IN3	OUT3
28	A8	128	18	20	IN4	OUT4
2A	AA	12A	10	21	IN5	OUT5
2C	AC	12C	12	22	IN6	OUT6
2E	AE	12E	24	23	IN7/INT15[4]	OUT7
30	B0	130	26	24	IN8/INT14	OUT8
32	B2	132	28	25	IN9/INT13	OUT9
34	B4	134	30	26	IN10/INT12	OUT10
36	B6	136	32	27	IN11/INT11	OUT11
38	B8	138	34	28	IN12/INT10	OUT12
3A	BA	13A	36	29	IN13/INT9	OUT13
3C	BC	13C	38	30	IN14/INT8	OUT14
3E	BE	13E	40	31	IN15/INT7	OUT15
40	C0	140	-	32	-	-
42	C2	142	-	33	-	-
44	C4	144	-	34	-	-
46	C6	146	-	35	-	-
48	C8	148	-	36	-	INT5 Reset (P1,P3 only)
4A	CA	14A	-	37	-	INT6 Reset(P1,P3) INT5 Reset (P2)
4C	CC	14C	-	38	-	INT6 Reset (P2 only)
4E	CE	14E	-	39	-	-

TABLE 5-1. CRU MAP (SHEET 2 OF 2)

Software Displacement$_{16}$[1]						
TMS 9901 No.1 (P2)	TMS 9901 No.2 (P3)	TMS 9901 No.3 (P4)	P2/P3/P4 Pin No.	CRU[2] Bit	CRU[3] Read	CRU[5] Write
50	D0	150	-	40	-	-
52	D2	152	-	41	-	-
54	D4	154	-	42	-	-
56	D6	156	-	43	-	-
58	D8	158	-	44	-	-
5A	DA	15A	-	45	-	-
5C	DC	15C	-	46	-	-
5E	DE	15E	-	47	-	-
60	E0	160	20	48	Echo OUT0	-
62	E2	162	22	49	Echo OUT1	-
64	E4	164	14	50	Echo OUT2	-
66	E6	166	16	51	Echo OUT3	-
68	E8	168	18	52	Echo OUT4	-
6A	EA	16A	10	53	Echo OUT5	-
6C	EC	16C	12	54	Echo OUT6	-
6E	EE	16E	24	55	Echo OUT7	-
70	F0	170	26	56	Echo OUT8	-
72	F2	172	28	57	Echo OUT9	-
74	F4	174	30	58	Echo OUT10	-
76	F6	176	32	59	Echo OUT11	-
78	F8	178	34	60	Echo OUT12	-
7A	FA	17A	36	61	Echo OUT13	-
7C	FC	17C	38	62	Echo OUT14	-
7E	FE	17E	40	63	Echo OUT15	-

[1]This column represents the value to be added to the software base address, as determined by switch S1, to access a given block of bits (e.g., add 20$_{16}$ to the software base address to place values on OUT0 through OUT15 with a LDCR instruction loading 16 bits).

[2]This column represents the displacement to be used with a CRU single bit instruction (e.g., SBO, SBZ, TB) with no displacement added to the base address.

[3]When Control Bit = 1, the top 16 bits of this column represent the CLK Read register or the INTREQ bit. When Control Bit = 0, the top 16 bits of this column represents the incoming interrupts (if enabled).

[4]The following 9 bits represent I/O bits unless the interrupt mask is set (enable= 1) for the corresponding INTX.

[5]When Control bit = 1, writing to the CLK bits sets the clock and writing to RST2- causes a reset. When Control Bit = 0, writing a 1 to a MASK bit enables the corresponding INTX.

5.3.1 Input/Output Example Program

This program demonstrates using the I/O and Echo bits. A cable as shown in Figure 5-1 will be needed for this program. The cable connects P2 (TMS 9901 no. 1) and P3 (TMS 9901 no. 2) so that the output bits of no. 1 TMS 9901 connect to the input bits of no. 2 TMS 9901.

- Reset the TMS 9901's.
- Set TMS 9901 no. 1 as output; output a test pattern.
- Read TMS 9901 no. 1 Echo bits and compare with test pattern; output error message if not the same.
- Read TMS 9901 no. 2 input bits and compare with test pattern; output error message if not the same.
- If both tests pass, print message and branch to monitor.

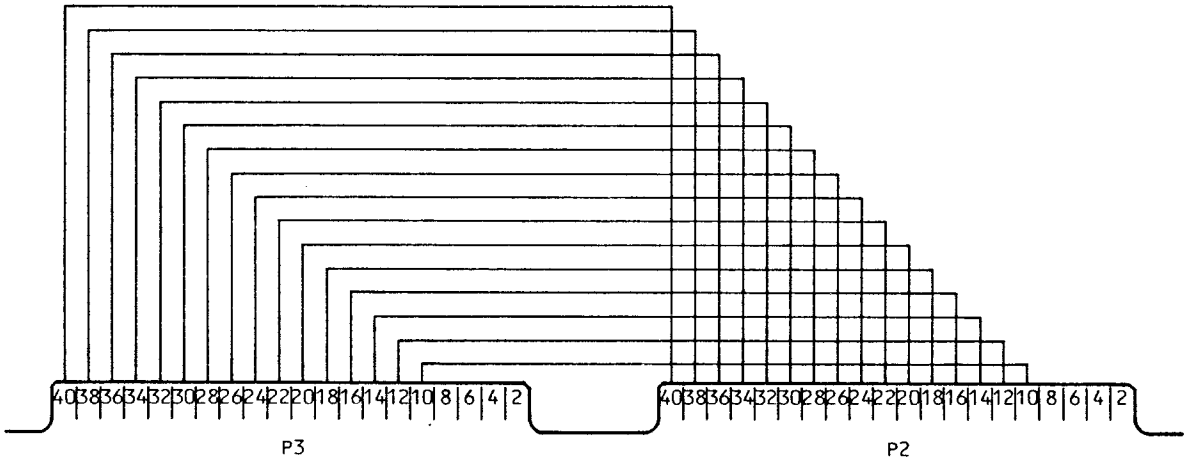


FIGURE 5-1. CABLE FOR EXAMPLE PROGRAMS

```
                ********************************************************************
                *                                                                  *
                *       INPUT/OUTPUT EXAMPLE PROGRAM                               *
                *                                                                  *
                ********************************************************************
                *       MAIN PROGRAM                                               *
                *                                                                  *
                ********************************************************************
F000                    AORG >F000
                *
                *       DEFINITIONS
                *
     0500       INT1    EQU  >0500          CRU ADDRESS OF 9901 NO.1 - INTERRUPT SECT.
     0520       PORT1   EQU  >0520          CRU ADDRESS OF 9901 NO.1 - PORT SECTION
     0540       INT2    EQU  >0580          CRU ADDRESS OF 9901 NO.2 - INTERRUPT SECT.
     0560       PORT2   EQU  >05A0          CRU ADDRESS OF 9901 NO.2 - PORT SECTION
F000            WSP     BSS  32             WORKSPACE
                *
                *       INITIALIZATION
                *
                *       RESET 9901 NO.1
                *
F020 02E0               LWPI WSP
F022 F000
F024 020C       INIT    LI   R12,INT1       LOAD CRU ADDRESS OF 9901 NO.1
F026 0500
F028 1D00               SBO  0              SET TO CLOCK MODE
F02A 1E0F               SBZ  15             RESET
                *
                *       RESET 9901 NO.2
                *
F02C 020C               LI   R12,INT2       LOAD CRU ADDRESS OF 9901 NO.2
F02E 0580
F030 1D00               SBO  0              SET TO CLOCK MODE
F032 1E0F               SBZ  15             RESET
                *
                *       SET PORT 1 (9901 NO.1) AS OUTPUT; OUTPUT PATTERN
                *
F034 020C               LI   R12,PORT1      LOAD CRU ADDRESS OF PORT 1
F036 0520
F038 0202               LI   R2,>AAAA       LOAD BIT PATTERN '1010101010101010'
F03A AAAA
F03C 3002               LDCR R2,0           SETS PORT 1 = OUTPUT, OUTPUTS PATTERN
                *
                *       ECHO PATTERN AT TMS 9901 NO. 1; COMPARE WITH TEST PATTERN
                *       AI   R12,>40          SET CRU ADDRESS TO ECHO CHARACTERS
F03E 3403               STCR R3,0           ECHOS PORT 1 OUTPUT BACK TO R3
F040 80C2               C    2,3            IS OUTPUT AND ECHO THE SAME?
F042 1606               JNE  ERR1           IF NOT, OUTPUT ERROR MESSAGE
                *
                *       READ PATTERN AT TMS 9901 NO.2; COMPARE WITH TEST PATTERN
                *
F044 020C               LI   R12,PORT2      SET CRU BASE ADDRESS TO PORT 2 (9901 No.2)
F046 0580
F048 3404               STCR R4,0           READ PORT 2 INPUTS
F04A 8102               C    2,4            PORT 2 INPUTS EQUAL PORT 1 OUTPUTS
F04C 160F               JNE  ERR2           IF NOT, OUTPUT ERROR MESSAGE
```

```
                *       IF BOTH TESTS PASS, GO TO FINISH
                *
F04E 101D               JMP  FIN            TESTS PASSED, GO TO FINISH
                ********************************************************************
                *  ERROR MESSAGES                                                  *
                *                                                                  *
                ********************************************************************
                *
                *       ERROR MESSAGE 1 - ERROR- NO ECHO
                *
F050 2FA0       ERR1    XOP  @MESS1,14      OUTPUT ERROR MESSAGE 1
F052 F058
F054 0460               B    @>80           BRANCH TO MONITOR
F056 0080
F058 0D0A       MESS1   DATA >0D0A          CARRAGE RETURN/LINE FEED
F05A   45               TEXT 'ERROR- NO ECHO'
F05B   52
F05C   52
F05D   4F
F05E   52
F05F   2D
F060   20
F061   4E
F062   4F
F063   20
F064   45
F065   43
F066   48
F067   4F
F068 0D0A               DATA >0D0A          CARRAGE RETURN/LINE FEED
F06A 0000               DATA >0000          END OF MESSAGE TAG
                *
                *       ERROR MESSAGE 2 - ERROR- NO INPUTS
                *
F06C 2FA0       ERR2    XOP  @MESS2,14      OUTPUT ERROR MESSAGE 2
F06E F074
F070 0460               B    @>80           BRANCH TO MONITOR
F072 0080
F074 0D0A       MESS2   DATA >0D0A          CARRAGE RETURN/LINE FEED
F076   45               TEXT 'ERROR- NO INPUTS'
F077   52
F078   52
F079   4F
F07A   52
F07B   2D
F07C   20
F07D   4E
F07E   4F
F07F   20
F080   49
F081   4E
F082   50
F083   55
F084   54
F085   53
F086 0D0A               DATA >0D0A          CARRAGE RETURN/LINE FEED
F088 0000               DATA >0000          END OF MESSAGE TAG
```

```
                *
                *       MESSAGE 3 - TESTS PASSED
                *
F08A 2FA0   FIN     XOP  @MESS3,14
F08C F092
F08E 0460           B    @>80           BRANCH TO MONITOR
F090 0080
F092 0D0A   MESS3   DATA >0D0A          CARRAGE RETURN/LINE FEED
F094   54          TEXT 'TESTS PASSED'
F095   45
F096   53
F097   54
F098   53
F099   20
F09A   50
F09B   41
F09C   53
F09D   53
F09E   45
F09F   44
F0A0 0D0A           DATA >0D0A          CARRAGE RETURN/LINE FEED
F0A2 0000           DATA >0000          END OF MESSAGE TAG
```

5.3.2 Clock Example Program (Polling)

This program demonstrates how to set and use the clock on no. 1 TMS 9901 on the TM 990/310 module. After a period of five seconds, a message is written. This example requires no TM 990/310 cable or connectors. The steps of this program are as follows:

1. Reset the TMS 9901.

2. Go to the interrupt mode and enable INT3 (the clock issues INT3, and INTREQ goes high when finished counting down).

3. Go to the clock mode and set the clock to a 250 ms count (for 3 MHz system clock).

4. Poll the INTREQ bit (see Table 5-1) until the clock is finished (do not poll INT3 for a clock countdown).

5. Repeat countdown 20 times for a 5-second delay.

6. Output message after 5-second countdown.

NOTE

After the TMS 9901 clock register is decremented down to zero, it is reinitialized with the original count value automatically, and the countdown begins again. The clock is disabled by writing all zeroes to the 14 clock bits or by a hardware (external) reset (not a software reset to bit 15 in the clock mode). Writing a one or a zero to the INT3 interrupt mask (bit 3) clears the interrupt; however, writing a one to this bit re-enables the clock interrupt.

```
                ************************************************************
                *
                *       POLLING CLOCK EXAMPLE
                *
                ************************************************************
                *
                *       INITIALIZATION AND DEFINITIONS
                *
F000                    AORG >F000
F000            WSP     BSS  32
F020 02E0               LWPI WSP            SET WORKSPACE POINTER
F022 F000
F024 0201               LI   R1,20          LOOP COUNTS OF 20 250-MS PERIODS (5S)
F026 0014
F028 0202               LI   R2,>0800       CODE TO GO TO INT MODE AND SET INT3
F02A 0800
F02C 0203               LI   R3,>2DFC       COUNT FOR CLOCK REGISTER (250 MS)
F02E 2DFC
F030 020C               LI   R12,>500       CRU BASE ADDRESS OF NO. 1 TMS 9901
F032 0500
                *
                *       RESET 9901'S
                *
F034 0360               RSET
                *
                *       ENABLE INTERRUPTS
                *
F036 3102       START   LDCR R2,4           GO TO INTERRUPT MODE, ENABLE INT3
                *
                *       ENABLE CLOCK
                *
F038 1D00               SBO  0              GO TO CLOCK MODE
F03A 05CC               INCT R12            SET CRU BASE UP TO FIRST CLOCK BIT
F03C 3383               LDCR R3,14          SET 250 MS COUNT, START COUNTDOWN
                *
                *       POLL INTREQ (BIT 15) WAITING FOR CLOCK TO FINISH
                *
F03E 064C               DECT R12            SET CRU BASE BACK TO CONTROL BIT
F040 1D00       LOOP    SBO  0              GO TO CLOCK MODE
F042 1F0F               TB   15             HAS THE CLOCK FINISHED?
F044 16FD               JNE  LOOP           IF NOT, WAIT FOR COUNT = 0
                *       COUNTER TO COUNT 5 SECONDS
F046 1E00               SBZ  0              GO TO INTERRUPT MODE
F048 1D03               SBO  3              RE-ENABLE CLK INTRRPT, CLEAR INTRRPT
F04A 0601               DEC  R1             DECREMENT COUNTER OF 250-MS PERIODS
F04C 16F9               JNE  LOOP           IF NOT ZERO, RUN DELAY AGAIN
                *
                *       OUTPUT MESSAGE
                *
F04E 2FA0               XOP  @MESS,14       OUTPUT 5-SECOND DELAY MESSAGE
F050 F056
F052 0460               B    @>80           BRANCH TO MONITOR
F054 0080
```

```
F056 0D0A  MESS   DATA >0D0A        CARRIAGE RETURN, LINE FEED
F058   46        TEXT 'FIVE SECONDS DELAY'
F059   49
F05A   56
F05B   45
F05C   20
F05D   53
F05E   45
F05F   43
F060   4F
F061   4E
F062   44
F063   53
F064   20
F065   44
F066   45
F067   4C
F068   41
F069   59
F06A 0D0A        DATA >0D0A        CARRIAGE RETURN, LINE FEED
F06C 0000        DATA >0000        END OF MESSAGE TAG
                 END
```

5.3.3 Example Using Interrupts

This example demonstrates how to enable and handle interrupts. Figure 5-2 shows the interrupt path from an external source through the TM 990/310 to the CPU. The numbered steps described below are keyed in Figure 5-2. For this example, the connector shown in Figure 5-1 can be used, or a single wire connecting P2-40 to P3-40 can be substituted. This example performs the following steps:

1. Load the interrupt linking areas with the starting address of the interrupt service routine (see your TM 990/1XX Users Manual).

2. Reset all 9901's. This places the I/O bits to the input mode and resets the interrupts on all four 9901s (three on the TM 990/310 and one on on the CPU module).

3. Enable interrupt 4 on the TMS 9901 on the CPU module.

4. Enable interrupt 7 on the TMS 9901 no. 1 (P2) on the TM 990/310.

5. Enable interrupt levels 0 through 4 of interrupt mask on the TMS 9900.

6. Set I/O bit 15 of TMS 9901 no. 2 on the TM 990/310 as an output with a logic 0 level.

7. The interrupt service routine disables the interrupt, prints a message indicating that the interrupt has happened, and returns to the main program.

8. The main program prints a message that all steps have been successfully completed and returns control to the monitor.

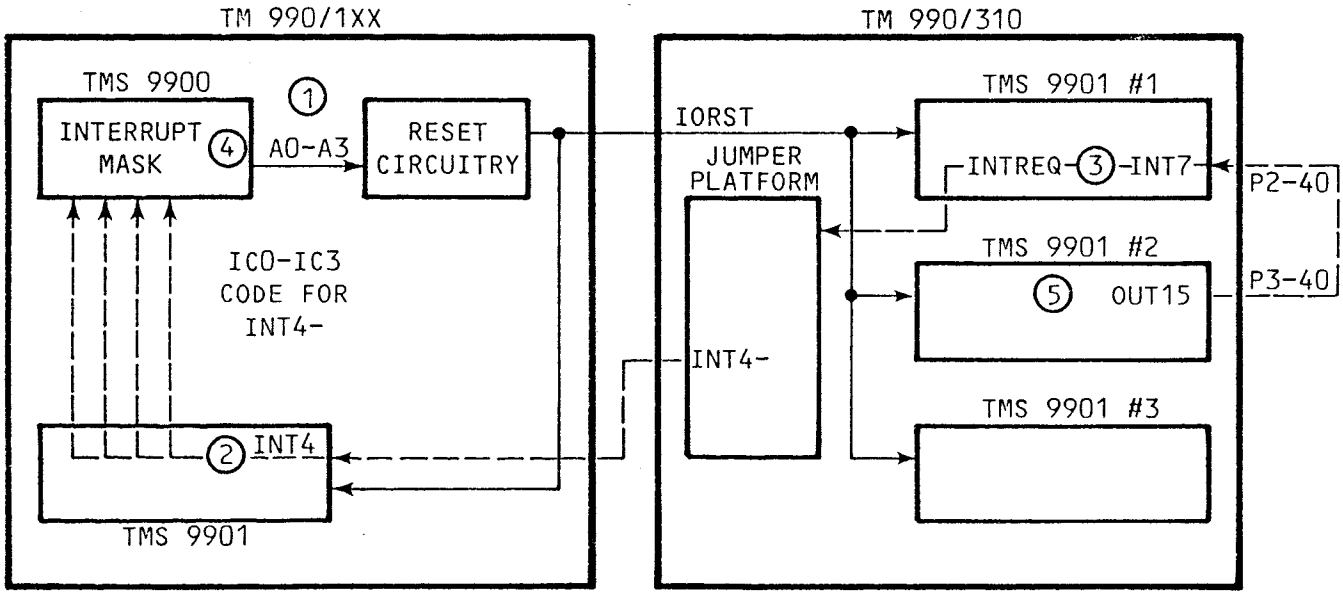


FIGURE 5-2. INTERRUPT PATH FOR EXAMPLE 5.3.3

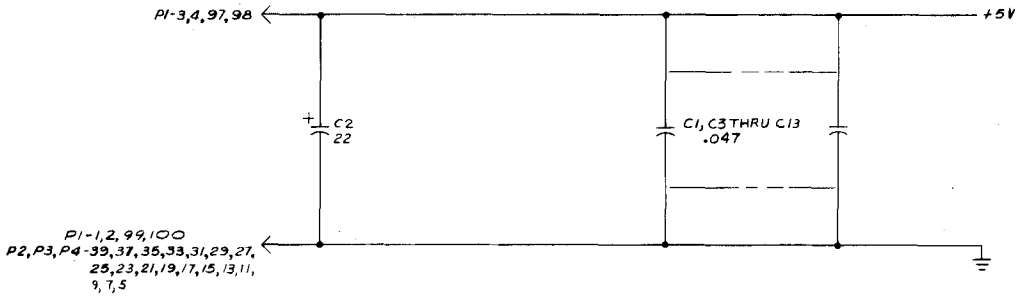
```
                ********************************************************************
                *                                                                  *
                *       INTERRUPT EXAMPLE PROGRAM                                  *
                *                                                                  *
                ********************************************************************
                *       INITIALIZATION                                             *
                *                                                                  *
                ********************************************************************
F000                    AORG >F000
F000            WSP     BSS  32             RESERVE WORKSPACE AREA
F020 02E0               LWPI WSP            LOAD WORKSPACE POINTER
F022 F000
F024 0360               RSET                RESET ALL 9901'S
                *
                *       ENABLE THE INTERRUPTS ON THE CPU 9901, THE /310 9901
                *       AND THE INTERRUPT MASK ON THE 9900
                *
F026 020C               LI   R12,>100       CRU ADDR OF 9901 ON CPU MODULE
F028 0100
F02A 1E00               SBZ  0              SET TO INTERRUPT MODE
F02C 1D04               SBO  4              ENABLE INT 4 ON CPU 9901
                *
F02E 020C               LI   R12,>500       CRU ADDR OF 9901 #1 ON /310
F030 0500
F032 1E00               SBZ  0              SET TO INTERRUPT MODE
F034 1D07               SBO  7              ENABLE INTERRUPT 7
                *
F036 0300               LIMI 4              ENABLE INTERRUPT 4 - 0 ON 9900
F038 0004
F03A 04C0               CLR  R0             CLEAR R0
                *
                *       SIMULATE AN EXTERNAL INTERRUPT
                *
F03C 020C               LI   R12,>5A0       CRU ADDR OF I/O ON 9901 #2 - /310
F03E 05A0
F040 1E0F               SBZ  15             ACTIVATE INT7-
F042 1000               NOP                 TO ALLOW TIME FOR THE INTERRUPT
F044 1000               NOP                 TO OCCUR
F046 C000               MOV  R0,R0          DID INTERRUPT OCCUR
F048 1603               JNE  OK             IF YES JUMP
F04A 2FA0               XOP  @FAIL,14       PRINT FAIL MESSAGE
F04C F0B4
F04E 1002               JMP  END            GO TO EXIT
F050 2FA0       OK      XOP  @MESS1,14      OUTPUT INTERRUPT MESSAGE
F052 F082
F054 2FA0       END     XOP  @MESS2,14      PRINT 'PROGRAM FINISHED'
F056 F09E
F058 0460               B    @>80           RETURN TO MONITOR
F05A 0080
                *
                *       LOAD INTERRUPT VECTOR VALUES
                *
FF9E                    AORG >FF9E          START AT INT4 VECTOR
FF9E 0420               BLWP @>F070         BRANCH TO INTERRUPT SERVICE ROUTIN
FFA0 F070
FFA2 0380               RTWP                RETURN TO PROGRAM
```

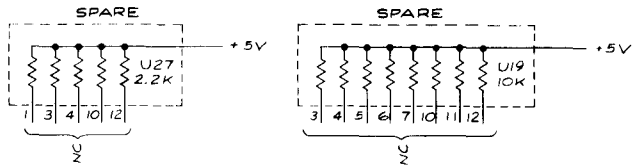
```
                ********************************************************************
                *       INTERRUPT SERVICE ROUTINE                                  *
                ********************************************************************
F070                    AORG >F070          START AT INTERRUPT SERVICE ROUTINE
F070 F000               DATA >F000          WORKSPACE POINTER FOR INT SERV ROUTINE
F072 F074               DATA >F074            PROGRAM COUNTER FOR INT SERV ROUTINE
F074 0200               LI   R0,>FFFF       SET INTERRUPT 'FLAG'
F076 FFFF
F078 020C               LI   R12,>100       CRU BASE ADDR OF 9901 ON CPU MODULE
F07A 0100
F07C 1E00               SBZ  0              SET TO INTERRUPT MODE
F07E 1E04               SBZ  4              DISABLE INTERRUPT AT 9901 ON CPU
F080 0380               RTWP                RETURN
                ********************************************************************
                *       MESSAGE TEXTS                                              *
                ********************************************************************
F082 0D0A  MESS1        DATA >0D0A          CARRIAGE RETURN, LINE FEED
F084   49               TEXT 'INTERRUPT HAS OCCURRED'
F085   4E
F086   54
F087   45
F088   52
F089   52
F08A   55
F08B   50
F08C   54
F08D   20
F08E   48
F08F   41
F090   53
F091   20
F092   4F
F093   43
F094   43
F095   55
F096   52
F097   52
F098   45
F099   44
F09A 0D0A               DATA >0D0A          CARRIAGE RETURN, LINE FEED
F09C 0000               DATA >0000          END OF MESSAGE TAG
```

```
F09E 0D0A  MESS2  DATA >0D0A        CARRIAGE RETURN, LINE FEED
F0A0   50         TEXT 'PROGRAM FINISHED'
F0A1   52
F0A2   4F
F0A3   47
F0A4   52
F0A5   41
F0A6   4D
F0A7   20
F0A8   46
F0A9   49
F0AA   4E
F0AB   49
F0AC   53
F0AD   48
F0AE   45
F0AF   44
F0B0 0D0A         DATA >0D0A        CARRIAGE RETURN, LINE FEED
F0B2 0000         DATA >0000        END OF MESSAGE TAG
                  *
F0B4 0D0A  FAIL   DATA >0D0A        CARRIAGE RETURN, LINE FEED
F0B6   49         TEXT 'INTERRUPT FAILED TO OCCUR'
F0B7   4E
F0B8   54
F0B9   45
F0BA   52
F0BB   52
F0BC   55
F0BD   50
F0BE   54
F0BF   20
F0C0   46
F0C1   41
F0C2   49
F0C3   4C
F0C4   45
F0C5   44
F0C6   20
F0C7   54
F0C8   4F
F0C9   20
F0CA   4F
F0CB   43
F0CC   43
F0CD   55
F0CE   52
F0D0 0D0A         DATA >0D0A        CARRIAGE RETURN, LINE FEED
F0D2 0000         DATA >0000        END OF MESSAGE TAG
```

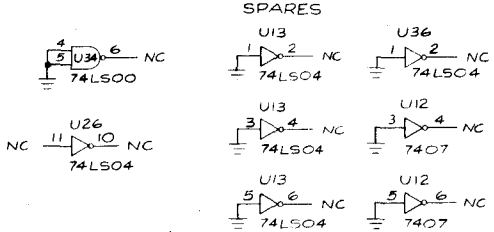
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN448634	12-21-78	
	SEE CN FOR DWG CORRECTION		

NOTES: UNLESS OTHERWISE SPECIFIED:
1. CAPACITANCE VALUES ARE IN MICROFARADS
2. RESISTANCE VALUES ARE IN OHMS
3. ALL RESISTORS ARE 1/4 W, ±5%
4. CUSTOMER'S USE - NOT INSTALLED
5. ALL 16 PIN CIRCUITS UTILIZE PIN 16 AS VCC(+5V) AND PIN 8 AS GND
6. ALL 14 PIN CIRCUITS UTILIZE PIN 14 AS VCC(+5V) AND PIN 7 AS GND
7. ALL 20 PIN CIRCUITS UTILIZE PIN 20 AS VCC (+5V) AND PIN 10 AS GND
8. NC DENOTES NO CONNECTION





SPARES



REV STATUS OF SHEETS	REV	A	A	A		A
	SH	1	2	3	4	5

SEQ NO	IDENT	P.SPEC	NO	ADDITIONAL	NOTES
	PROCESS			CLASSIFICATION	

PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS, SEE TI DRAWING 729467

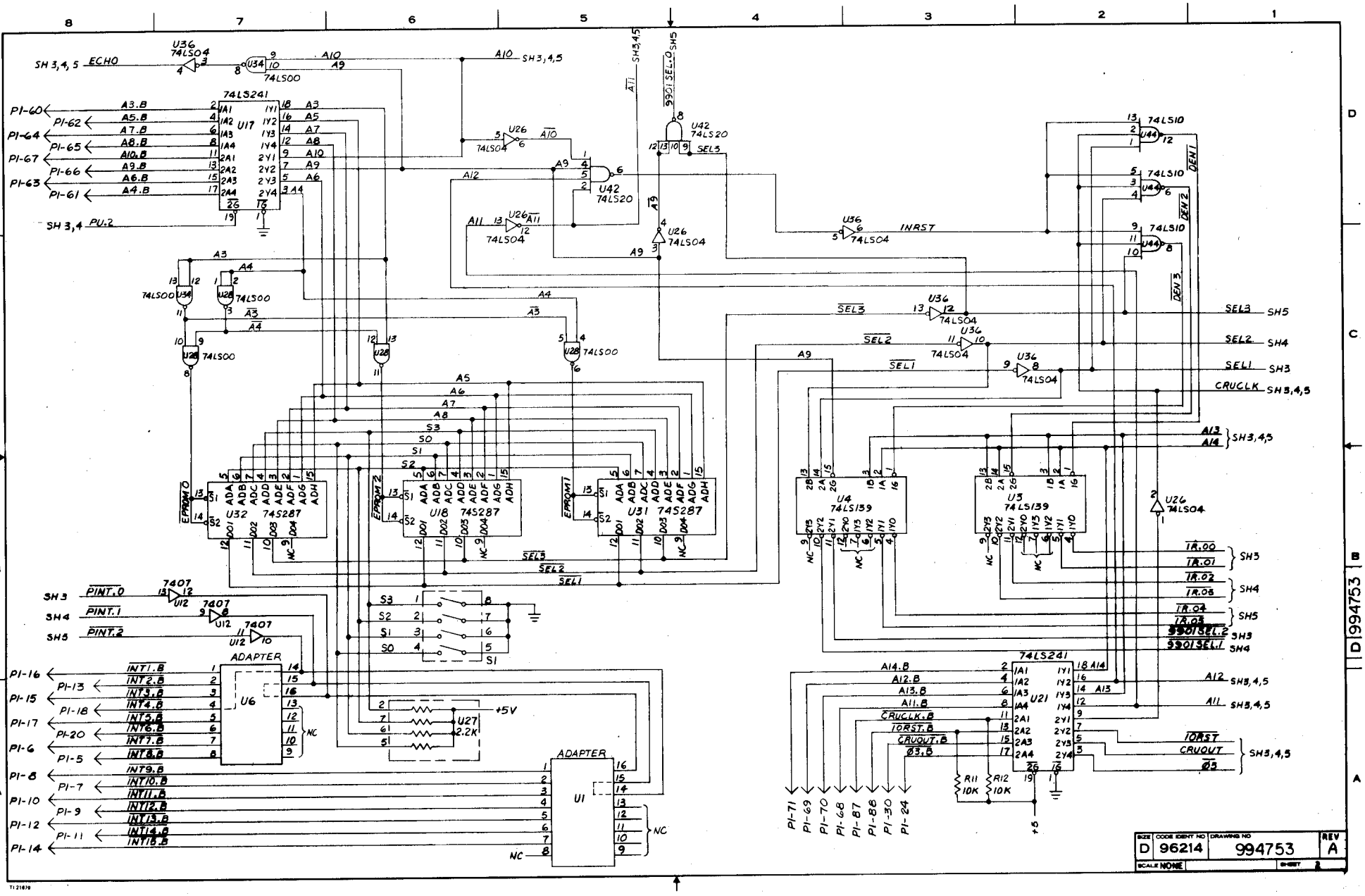
QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES
		PARTS LIST			
		UNLESS OTHERWISE SPECIFIED • DIMENSIONS ARE IN INCHES • TOLERANCES ANGLES ±1° 3 PLACE DECIMALS ± .010 2 PLACE DECIMALS ± .02 • INTERPRET DRAWING PER MIL D 1000 • REMOVE ALL BURRS AND SHARP EDGES • CONCENTRICITY MACHINED DIAMETERS .010 FIM • DIMENSIONAL LIMITS APPLY BEFORE PROCESSES • PARENTHETICAL INFO FOR REF ONLY HOLE TOLERANCE .013 THRU .124 ± .004 (.125 THRU .249 ± .005) (.251 THRU .500 ± .008) .501 THRU .750 ± .008 (.751 THRU 1.000 ± .010) (1.001 THRU 2.000 ± .012)			
	994752	8117			
	994751	8117			
	NEXT ASSY	USED ON			
	APPLICATION				

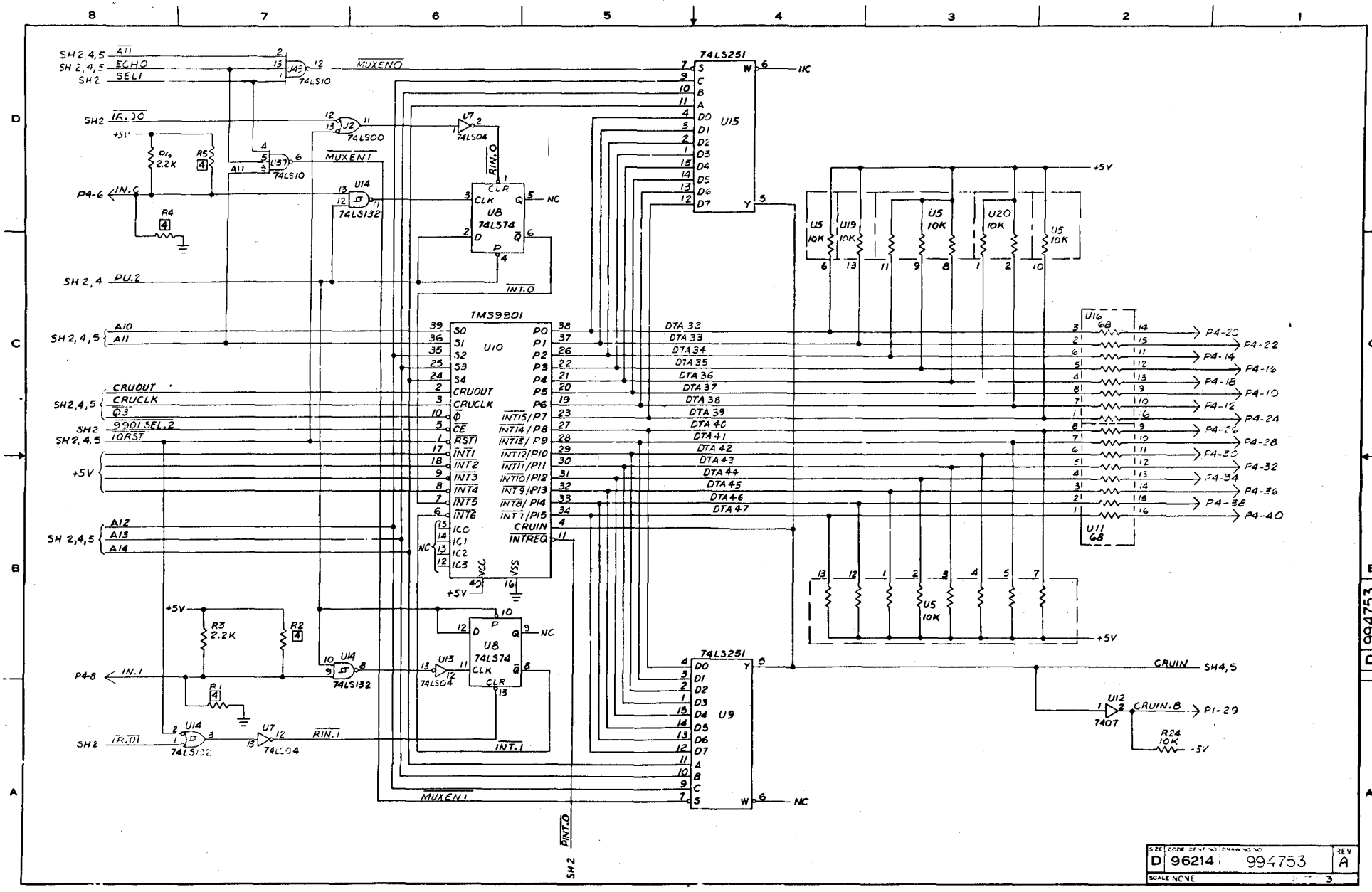
DWN Thomas Brumley 8/22/77
CHK [illegible] 12/9/77
ENGR [illegible]
APPD [illegible]
QA [illegible] 12-28-77
CONFIG [illegible] 1/9/78
PROJ [illegible] 1/9/78

TEXAS INSTRUMENTS INCORPORATED
Dallas, Texas

DIAGRAM, LOGIC, DETAILED
TM990/310

SIZE D | FSCM NO 96214 | DRAWING NO 994753
SCALE NONE | SHEET 1 OF 5


SH 3,4,5 ECHO
U36 74LS04
U34 74LS00
A10
A9
SH3,4,5
74LS241
U17
PI-60
PI-62
PI-64
PI-65
PI-67
PI-66
PI-63
PI-61
A3.B
A5.B
A7.B
A8.B
A10.B
A9.B
A6.B
A4.B
SH 3,4 PU-2
U26 74LS04
U42 74LS20
SEL3
SEL2
SEL1
INRST
DEN1
DEN2
DEN3
SEL3 SH5
SEL2 SH4
SEL1 SH3
CRUCLK SH3,4,5
U28 74LS00
EPROM0
EPROM1
EPROM2
U32 74S287
U18 74S287
U31 74S287
U4 74LS139
U3 74LS139
A13 SH3,4,5
A14 SH3,4,5
TA.00 SH3
TA.01
TA.02 SH4
TA.03
TA.04 SH5
TA.05
9901SEL.2 SH3
9901SEL.1 SH4
7407 U12
PINT.0 SH3
PINT.1 SH4
PINT.2 SH5
S3
S2
S1
S0
ADAPTER U6
INT1.B
INT2.B
INT3.B
INT4.B
INT5.B
INT6.B
INT7.B
INT8.B
INT9.B
INT10.B
INT11.B
INT12.B
INT13.B
INT14.B
INT15.B
PI-16
PI-13
PI-15
PI-18
PI-17
PI-20
PI-6
PI-5
PI-8
PI-7
PI-10
PI-9
PI-12
PI-11
PI-14
NC
U27 2.2K
+5V
ADAPTER U1
74LS241 U21
A14.B
A12.B
A13.B
A11.B
CRUCLK.B
IORST.B
CRUOUT.B
Ø3.B
R11 10K
R12 10K
PI-71
PI-69
PI-70
PI-68
PI-87
PI-88
PI-30
PI-24
IORST
CRUOUT
Ø3
SH3,4,5
D 96214
994753
REV A
SCALE NONE
SHEET 2
D994753



SIZE	CODE IDENT NO	DWG NO	REV
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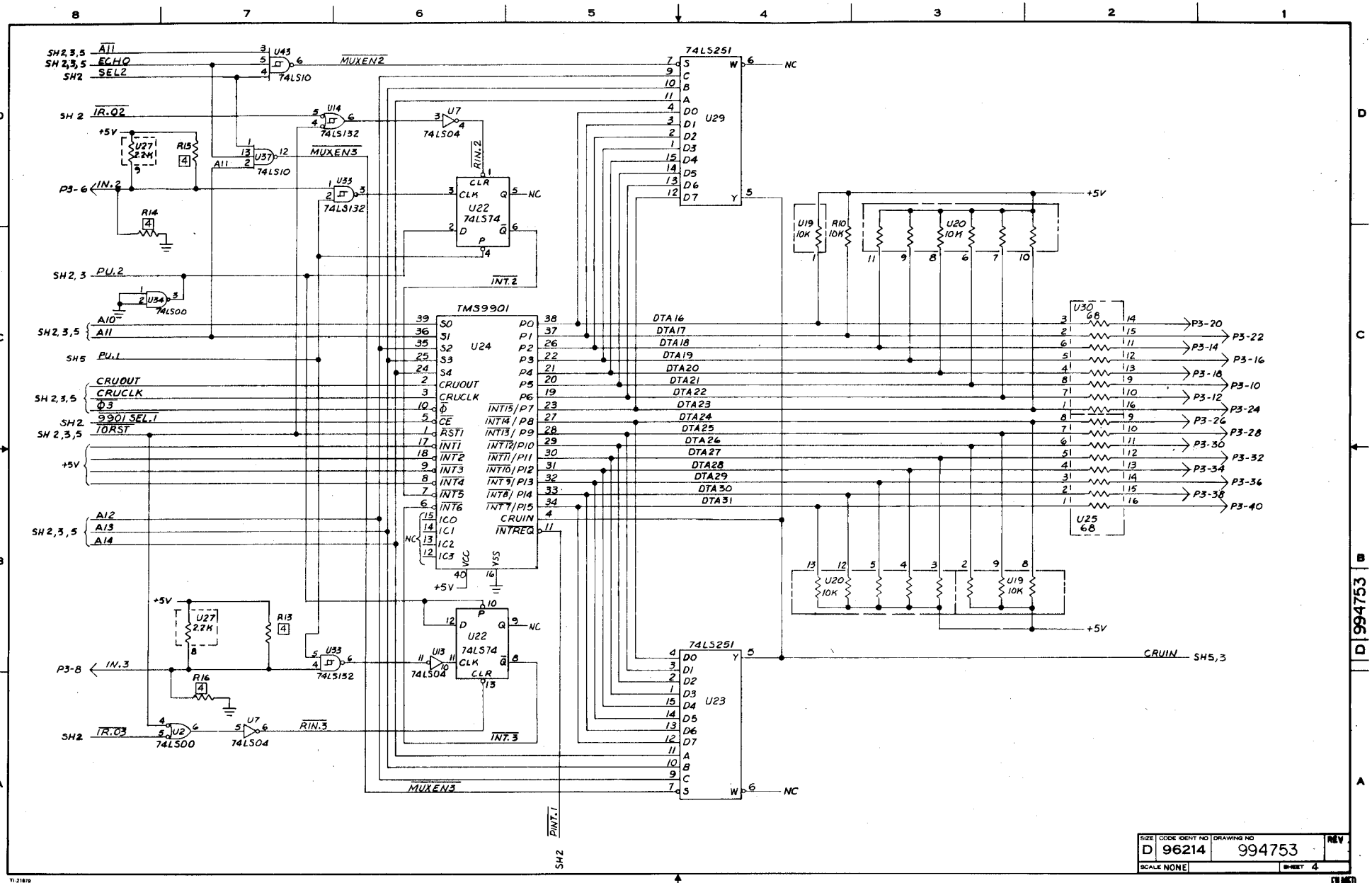
SCALE NONE SHEET 3

A-3

D 994753



SIZE	CODE IDENT NO	DRAWING NO	REV
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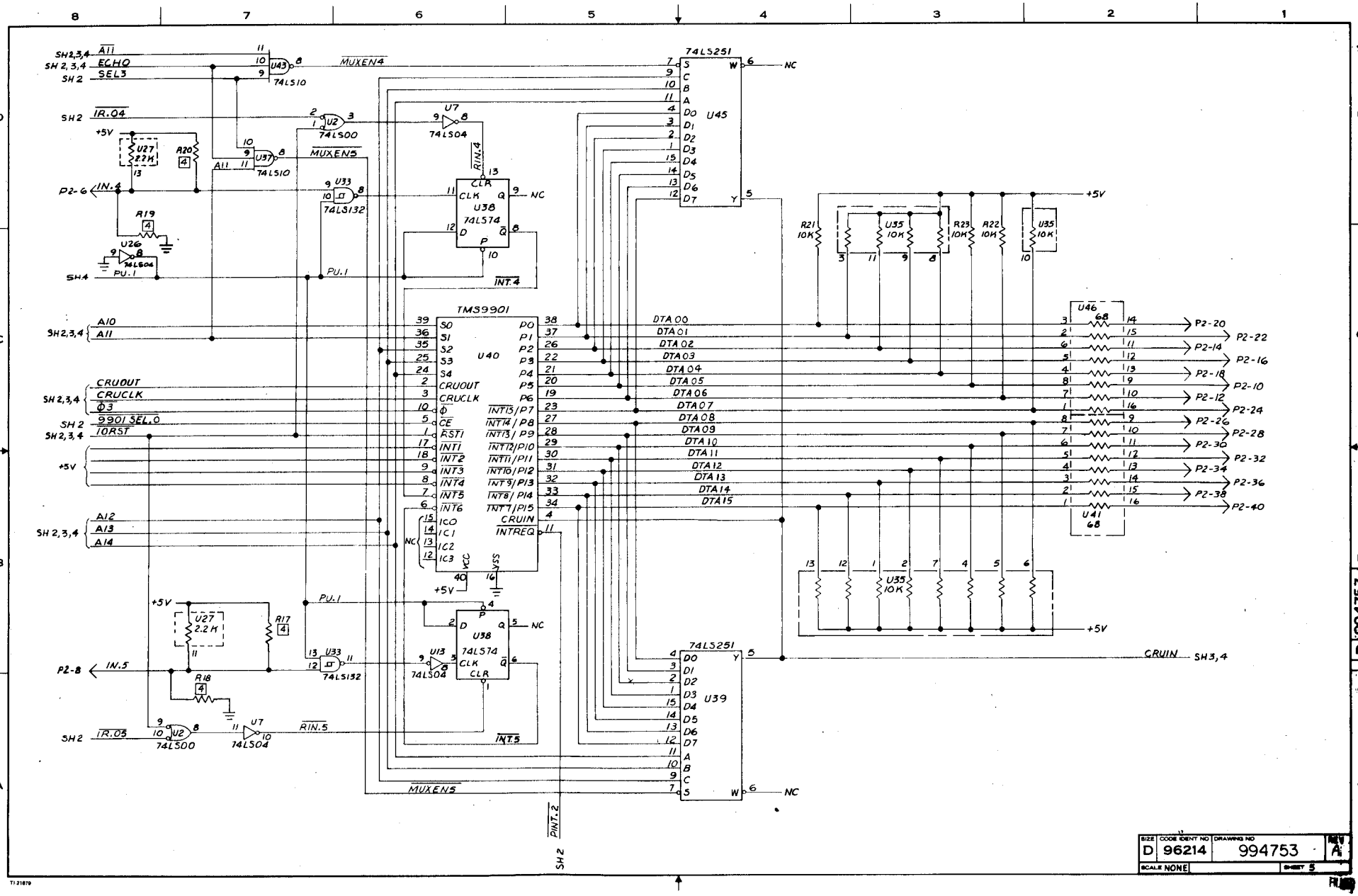
SCALE NONE		SHEET 4	

994753

A-4



SIZE	CODE IDENT NO	DRAWING NO	REV
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SCALE NONE		SHEET 5	

D 994753 A

A-5

TI 21879

APPENDIX B

PARTS LIST

SYMBOL	DESCRIPTION	QTY.
C1, C3 to C12	Capacitor, 0.047 μF	11
C2	Capacitor, 22 μF	1
R3, R6	Resistor, 2.2K, 1/4 W	2
R10,R11,R12,R21 R22,R23,R24	Resistor, 10K, 1/4 W	7
R7,R8,R9	Resistor, 2.2 ohm, 1/2 W	3
S1	Switch, 4-position	1
U1, U6	Platform, 16 pin, prewired/sockets (separate items)	2
U2,U28,U34	74LS00	3
U3, U4	74LS139	2
U5,U19,U20,U34	10K resistor pack	4
U7,U13,U26,U36	74LS04	5
U8,U22,U38	74LS74	3
U9,U15,U23, U29,U39,U45	74LS251	6
U10,U24,U40	TMS 9901/40-pin sockets (separate items)	3
U11,U16,U25,U30,U41,U46	68 ohm resistor pack	6
U12	7407	1
U14,U33	74LS132	2
U17,U21	74LS241	2
U18,U31,U32	74S287/16-pin sockets (separate items)	3
U37,U43,U44	74LS10	3
U42	74LS20	1

APPENDIX C

TMS 9901 PROGRAMMABLE SYSTEMS INTERFACE DATA MANUAL

The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

TMS 9901 PROGRAMMABLE SYSTEMS INTERFACE

JULY 1978

TEXAS INSTRUMENTS
INCORPORATED

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PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. INTRODUCTION

1.1 DESCRIPTION

The TMS 9901 Programmable Systems Interface (PSI) is a multifunctional component designed to provide low cost interrupt and I/O ports and an interval timer for TMS 9900-family microprocessor systems. The TMS 9901 is fabricated using N-channel silicon-gate MOS technology. The TMS 9901 is TTL-compatible on all inputs and outputs, including the power supply (+5 V) and single-phase clock.

1.2 KEY FEATURES

- Low Cost
- 9900-Family Peripheral
- Performs Interrupt and I/O Interface functions:
  - — Six Dedicated Interrupt Lines
  - — Seven Dedicated I/O Lines
  - — Nine Programmable Lines as I/O or Interrupt
  - — Up to 15 Interrupt Lines
  - — Up to 22 Input Lines
  - — Up to 16 Output Lines
- Easily Cascaded for Expansion
- Interval or Event Timer
- Single 5 V Power Supply
- All Inputs and Outputs TTL-Compatible
- Standard 40-Pin Plastic or Ceramic Package
- N-Channel Silicon-Gate MOS Technology.

1.3 APPLICATION OVERVIEW

The following example of a typical application may help introduce the user to the TMS 9901 PSI. Figure 1 is a block diagram of a typical application. Each of the ideas presented below is described in more detail in later sections of this manual.

The TMS 9901 PSI interfaces to the CPU through the Communications Register Unit (CRU) and the interrupt control lines as shown in Figure 1. The TMS 9901 occupies 32 bits of CRU input and output space. The five least significant bits of address bus are connected to the S lines of the PSI to address one of the 32 CRU bits of the TMS 9901. The most significant bits of the address bus are decoded on CRU cycles to select the PSI by taking its chip enable ($\overline{CE}$) line active (LOW).

Interrupt inputs to the TMS 9901 PSI are synchronized with $\bar{\phi}$, inverted, and then ANDed with the appropriate mask bit. Once every $\bar{\phi}$ clock time, the prioritizer looks at the 15 interrupt input AND gates and generates the interrupt control code. The interrupt control code and the interrupt request line constitute the interrupt interface to the CPU.

After reset all I/O ports are programmed as inputs. By writing to any I/O port, that port will be programmed as an output port until another reset occurs, either software or hardware. Data at the input pins is buffered on to the TMS 9901. Data to the output ports is latched and then buffered off-chip by the PSI's MOS-to-TTL buffers.

The interval timer on the TMS 9901 is accessed by writing a ONE to select bit zero (control bit), which puts the PSI CRU interface in the clock mode. Once in the clock mode the 14-bit clock contents can be read or written. Writing to the clock register will reinitialize the clock and cause it to start decrementing.. When the clock counts to zero, it will cause an interrupt and reload to its initial value. Reading the clock contents permits the user to see the decrementer contents at that point in time just before entering the clock mode. The clock read register is not updated when the PSI is in the clock mode.

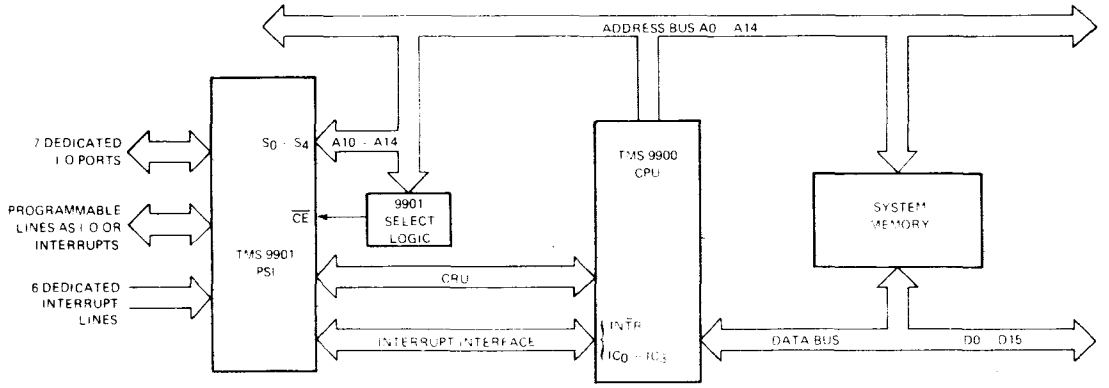


FIGURE 1– TYPICAL TMS 9901 PROGRAMMABLE SYSTEM INTERFACE (PSI) APPLICATION

2. ARCHITECTURE

The architecture of the TMS 9901 Programmable Systems Interface (PSI) is designed to provide the user maximum flexibility when designating system I/O ports and interrupts. The TMS 9901 can be divided into four subsystems: CRU interface, interrupt interface, input/output interface, and interval timer. Figure 2 is a general block diagram of the TMS 9901 internal architecture. Each of the subsystems of the PSI is discussed in detail in subsequent paragraphs.

2.1 CRU Interface

The CPU communicates with the TMS 9901 PSI via the CRU. The TMS 9901 occupies 32 bits in CRU read space and 32 bits in CRU write space. Table 1 shows the mapping for CRU bit addresses to TMS 9901 functions.

The CRU interface consists of five address select lines (S0-S4), chip enable ($\overline{CE}$), and the three CRU lines (CRUIN, CRUOUT, CRUCLK). The select lines (S0-S4) are connected to the five least significant bits of the address bus; for a TMS 9900 system S0-S4 are connected to A10-A14, respectively. Chip enable ($\overline{CE}$) is generated by decoding the most significant bits of the address bus on CRU cycles; for a 9900 based system address bits 0-9 would be decoded. When $\overline{CE}$ goes active (LOW), the five select lines point to the CRU bit being accessed. When $\overline{CE}$ is inactive (HIGH), the PSI's CRU interface is disabled.

NOTE

When $\overline{CE}$ is inactive (HIGH) the 9901 sets its CRUIN pin to high impedance and disables CRUCLK from coming on chip. This means that CRUIN can be used as an OR tied bus. When $\overline{CE}$ is high the 9901 will still see the select lines, but no command action is taken.

In the case of a write operation, the TMS 9901 strobes data off the CRUOUT line with CRUCLK. For a read operation, the data is sent to the CPU on the CRUIN line.

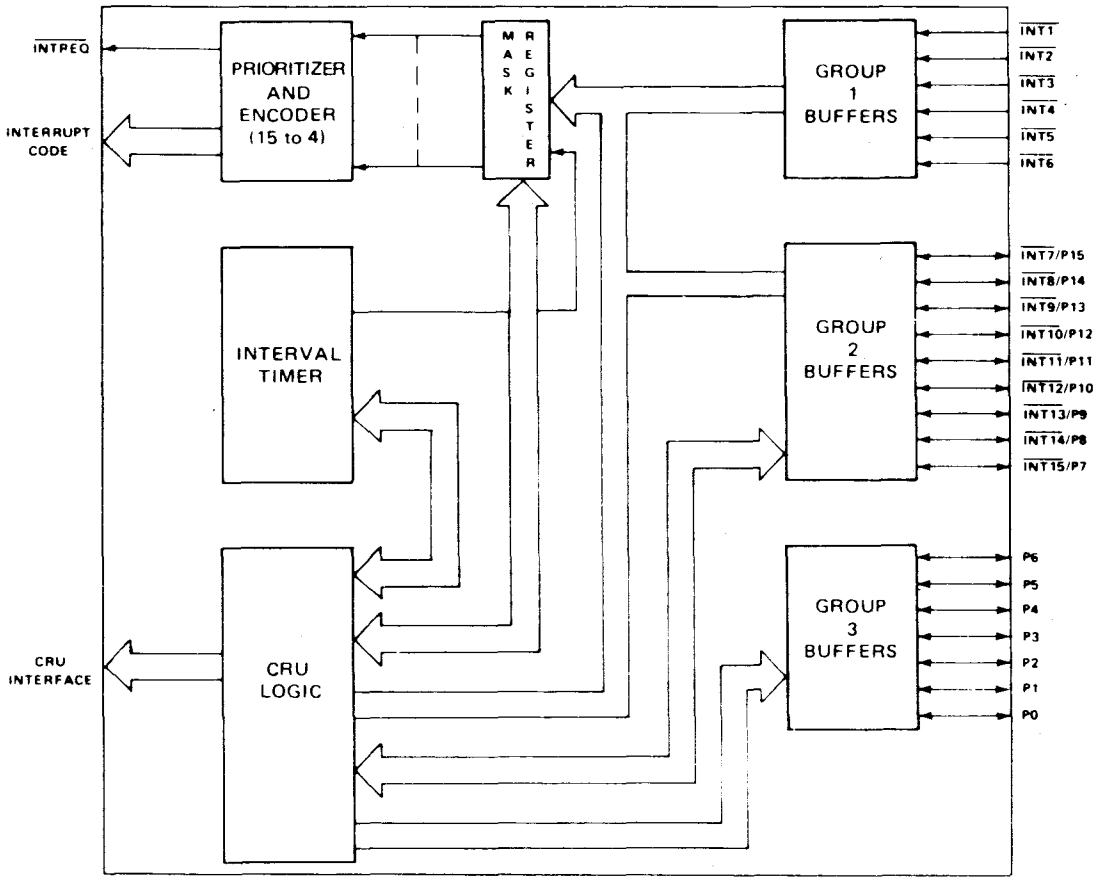


FIGURE 2–TMS 9901 PSI BLOCK DIAGRAM

Several TMS 9901 devices may be cascaded to expand I/O and interrupt handling capability simply by connecting all CRU and address select lines in parallel and providing each device with a unique chip enable signal: the chip enable ($\overline{CE}$) is generated by decoding the high-order address bits (A0-A9) on CRU cycles.

For those unfamiliar with the CRU concept, the following is a discussion of how to build a CRU interface. The CRU is a bit addressable (4096 bits), synchronous, serial interface over which a single instruction can transfer between one and 16 bits serially. Each one of the 4096 bits of the CRU space has a unique address and can be read and written to. During multi-bit CRU transfers, the CRU address is incremented at the beginning of each CRU cycle to point to the next consecutive CRU bit.

TABLE 1
CRU SELECT BIT ASSIGNMENTS

CRU Bit	S_0 S_1 S_2 S_3 S_4	CRU Read Data	CRU Write Data
0	0 0 0 0 0	CONTROL BIT(1)	CONTROL BIT(1)
1	0 0 0 0 1	$\overline{INT}$1/CLK1(2)	Mask 1/CLK1(3)
2	0 0 0 1 0	$\overline{INT}$2/CLK2	Mask 2/CLK2
3	0 0 0 1 1	$\overline{INT}$3/CLK3	Mask 3/CLK3
4	0 0 1 0 0	$\overline{INT}$4/CLK4	Mask 4/CLK4
5	0 0 1 0 1	$\overline{INT}$5/CLK5	Mask 5/CLK5
6	0 0 1 1 0	$\overline{INT}$6/CLK6	Mask 6/CLK6
7	0 0 1 1 1	$\overline{INT}$7/CLK7	Mask 7/CLK7
8	0 1 0 0 0	$\overline{INT}$8/CLK8	Mask 8/CLK8
9	0 1 0 0 1	$\overline{INT}$9/CLK9	Mask 9/CLK9
10	0 1 0 1 0	$\overline{INT}$10/CLK10	Mask 10/CLK10
11	0 1 0 1 1	$\overline{INT}$11/CLK11	Mask 11/CLK11
12	0 1 1 0 0	$\overline{INT}$12/CLK12	Mask 12/CLK12
13	0 1 1 0 1	$\overline{INT}$13/CLK13	Mask 13/CLK13
14	0 1 1 1 0	$\overline{INT}$14/CLK14	Mask 14/CLK14
15	0 1 1 1 1	$\overline{INT}$15/INTREQ(7)	Mask 15/$\overline{RST2}$(4)
16	1 0 0 0 0	PO Input(5)	PO Output(6)
17	1 0 0 0 1	P1 Input	P1 Output
18	1 0 0 1 0	P2 Input	P2 Output
19	1 0 0 1 1	P3 Input	P3 Output
20	1 0 1 0 0	P4 Input	P4 Output
21	1 0 1 0 1	P5 Input	P5 Output
22	1 0 1 1 0	P6 Input	P6 Output
23	1 0 1 1 1	P7 Input	P7 Output
24	1 1 0 0 0	P8 Input	P8 Output
25	1 1 0 0 1	P9 Input	P9 Output
26	1 1 0 1 0	P10 Input	P10 Output
27	1 1 0 1 1	P11 Input	P11 Output
28	1 1 1 0 0	P12 Input	P12 Output
29	1 1 1 0 1	P13 Input	P13 Output
30	1 1 1 1 0	P14 Input	P14 Output
31	1 1 1 1 1	P15 Input	P15 Output

NOTES:
(1) 0 = Interrupt Mode 1 = Clock Mode
(2) Data present on $\overline{INT}$ input pin (or clock value) will be read regardless of mask value.
(3) While in the Interrupt Mode (Control Bit = 0) writing a "1" into mask will enable interrupt; a "0" will disable.
(4) Writing a zero to bit 15 while in the clock mode (Control Bit = 1) executes a software reset of the I/O pins.
(5) Data present on the pin will be read. Output data can be read without affecting the data.
(6) Writing data to the port will program the port to the output mode and output the data.
(7) INTREQ is the inverted status of the $\overline{INTREQ}$ pin.

When a 99XX CPU executes a CRU Instruction, the processor uses the contents of workspace register 12 as a base address. (Refer to the *9900 Microprocessor Data Manual* for a complete discussion on how CRU addresses are derived.) The CRU address is brought out on the 15-bit address bus; this means that the least significant bit of R12 is not brought out of the CPU. During CRU cycles, the memory control lines ($\overline{\text{MEMEN}}$, $\overline{\text{WE}}$, and DBIN) are all inactive; $\overline{\text{MEMEN}}$ being inactive (HIGH) indicates the address is not a memory address and therefore is a CRU address or external instruction code. Also, when $\overline{\text{MEMEN}}$ is inactive (HIGH) and a valid address is present, address bits A0-A2 must all be zero to constitute a valid CRU address; if address bits A0-A2 are other than all zeros, they are indicating an external instruction code. In summary, address bits A3-A14 contain the CRU address to be decoded, address bits A0-A2 must be zero and $\overline{\text{MEMEN}}$ must be inactive (HIGH) to indicate a CRU cycle.

2.2 Interrupt Interface

A block diagram of the interrupt control section is shown in Figure 3. The interrupt inputs (six dedicated, $\overline{\text{INT1}}$-$\overline{\text{INT6}}$, and nine programmable) are sampled on the falling edge of $\overline{\phi}$ and latched onto the chip for one $\overline{\phi}$ time by the SYNC LATCH, each $\overline{\phi}$ time. The output of the sync latch is inverted (interrupts are LOW active) and ANDed with its respective mask bit (MASK = 1, INTERRUPT ENABLED). On the rising edge of $\overline{\phi}$, the prioritizer and encoder senses the masked interrupts and produces a four-bit encoding of the highest priority interrupt present (see Tables 2 and 3). The four-bit prioritized code and $\overline{\text{INTREQ}}$ are latched off-chip with a sync latch on the falling edge of the next $\overline{\phi}$, which ensures proper synchronization to the processor.

Once an interrupt goes active (LOW), it should stay active until the appropriate interrupt service routine explicitly turns off the interrupt. If an interrupt is allowed to go inactive before the interrupt service routine is entered, an erroneous interrupt code could be sent to the processor. A total of five clock cycles occur between the time the CPU samples the $\overline{\text{INTREQ}}$ line and the time it samples the IC0-IC3 lines. For example, if an interrupt is active and the CPU recognizes that an interrupt is pending, *but before the CPU can sample the interrupt control lines the interrupt goes inactive,* the interrupt control lines will contain an incorrect code.

The interrupt mask bits on the TMS 9901 PSI are individually set or reset under software control. Any unused interrupt line should have its associated mask disabled to avoid false interrupts: To do this, the control bit (CRU bit zero), is first set to a zero for interrupt mode operation. Writing to TMS 9901 CRU bits 1-15 will enable or disable interrupts 1-15, respectively. Writing a one to an interrupt mask will *enable* that interrupt; writing a zero will *disable* that interrupt. Upon application of $\overline{\text{RST1}}$ (power-up reset), all mask bits are reset (LOW), the interrupt code is forced to all zeros, and $\overline{\text{INTREQ}}$ is held HIGH. Reading TMS 9901 CRU bits 1-15 indicates the status of the respective interrupt inputs; thus, the designer can employ the unused (disabled) interrupt input lines as data inputs (true data in).

2.3 Input/Output Interface

A block diagram of the TMS 9901 I/O interface is shown in Figure 4. Up to 16 individually controlled, I/O ports are available (seven dedicated, P0-P6, and nine programmable) and, as discussed above, the unused dedicated interrupt lines also can be used as input lines (true data in). Thus the 9901 can be configured to have more than 16 inputs. $\overline{\text{RST1}}$ (power-up reset) will program all I/O ports to input mode. Writing data to a port will automatically switch that port to the output mode. Once programmed as an output, a port will remain in output mode until $\overline{\text{RST1}}$ or $\overline{\text{RST2}}$ (command bit) is executed. An output port can be read and indicates the present state of the pin. A pin programmed to the output mode *cannot* be used as an input pin: *Applying an input current to an output pin may cause damage to the TMS 9901.* The TMS 9901 outputs are latched and buffered off-chip, and inputs are buffered onto the chip. The output buffers are MOS-to-TTL buffers and can drive two standard TTL loads.

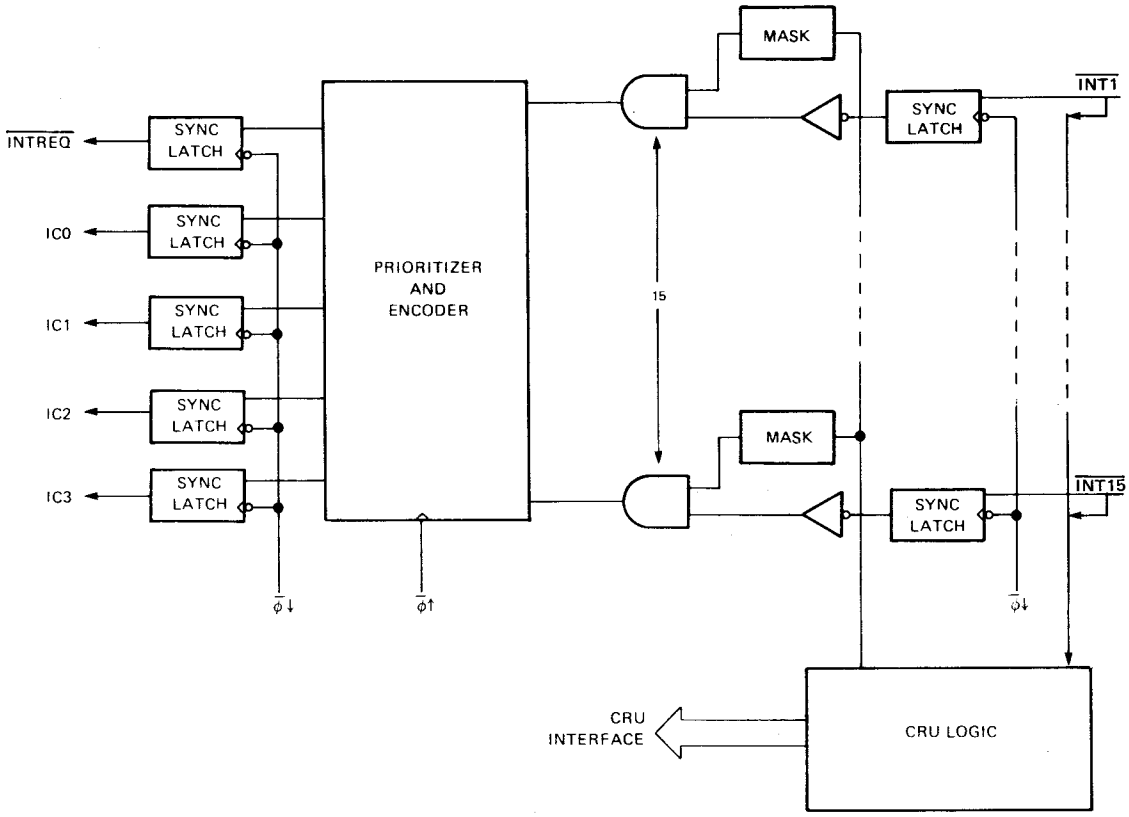


FIGURE 3– TMS 9901 PSI INTERRUPT CONTROL SECTION BLOCK DIAGRAM

TABLE 2
INTERRUPT CODE GENERATION

INTERRUPT/STATE	PRIORITY	I_{C0}	I_{C1}	I_{C2}	I_{C3}	$\overline{INTREQ}$
$\overline{RST}$ 1	–	0	0	0	0	1
$\overline{INT}$ 1	1 (HIGHEST)	0	0	0	1	0
$\overline{INT}$ 2	2	0	0	1	0	0
$\overline{INT}$ 3/CLOCK	3	0	0	1	1	0
$\overline{INT}$ 4	4	0	1	0	0	0
$\overline{INT}$ 5	5	0	1	0	1	0
$\overline{INT}$ 6	6	0	1	1	0	0
$\overline{INT}$ 7	7	0	1	1	1	0
$\overline{INT}$ 8	8	1	0	0	0	0
$\overline{INT}$ 9	9	1	0	0	1	0
$\overline{INT}$ 10	10	1	0	1	0	0
$\overline{INT}$ 11	11	1	0	1	1	0
$\overline{INT}$ 12	12	1	1	0	0	0
$\overline{INT}$ 13	13	1	1	0	1	0
$\overline{INT}$ 14	14	1	1	1	0	0
$\overline{INT}$ 15	15 (LOWEST)	1	1	1	1	0
NO INTERRUPT	–	1	1	1	1	1

TABLE 3
TMS 9980A OR TMS 9981 INTERRUPT LEVEL DATA

INTERRUPT CODE (IC0–IC2)	FUNCTION	VECTOR LOCATION (MEMORY ADDRESS IN HEX)	DEVICE ASSIGNMENT	INTERRUPT MASK VALUES TO ENABLE (ST12 THROUGH ST15)
1 1 0	Level 4	0 0 1 0	External Device	4 Through F
1 0 1	Level 3	0 0 0 C	External Device	3 Through F
1 0 0	Level 2	0 0 0 8	External Device	2 Through F
0 1 1	Level 1	0 0 0 4	External Device	1 Through F
0 0 1	Reset	0 0 0 0	Reset Stimulus	Don't Care
0 1 0	Load	3 F F C	Load Stimulus	Don't Care
0 0 0	Reset	0 0 0 0	Reset Stimulus	Don't Care
1 1 1	No-Op	.....	.....	

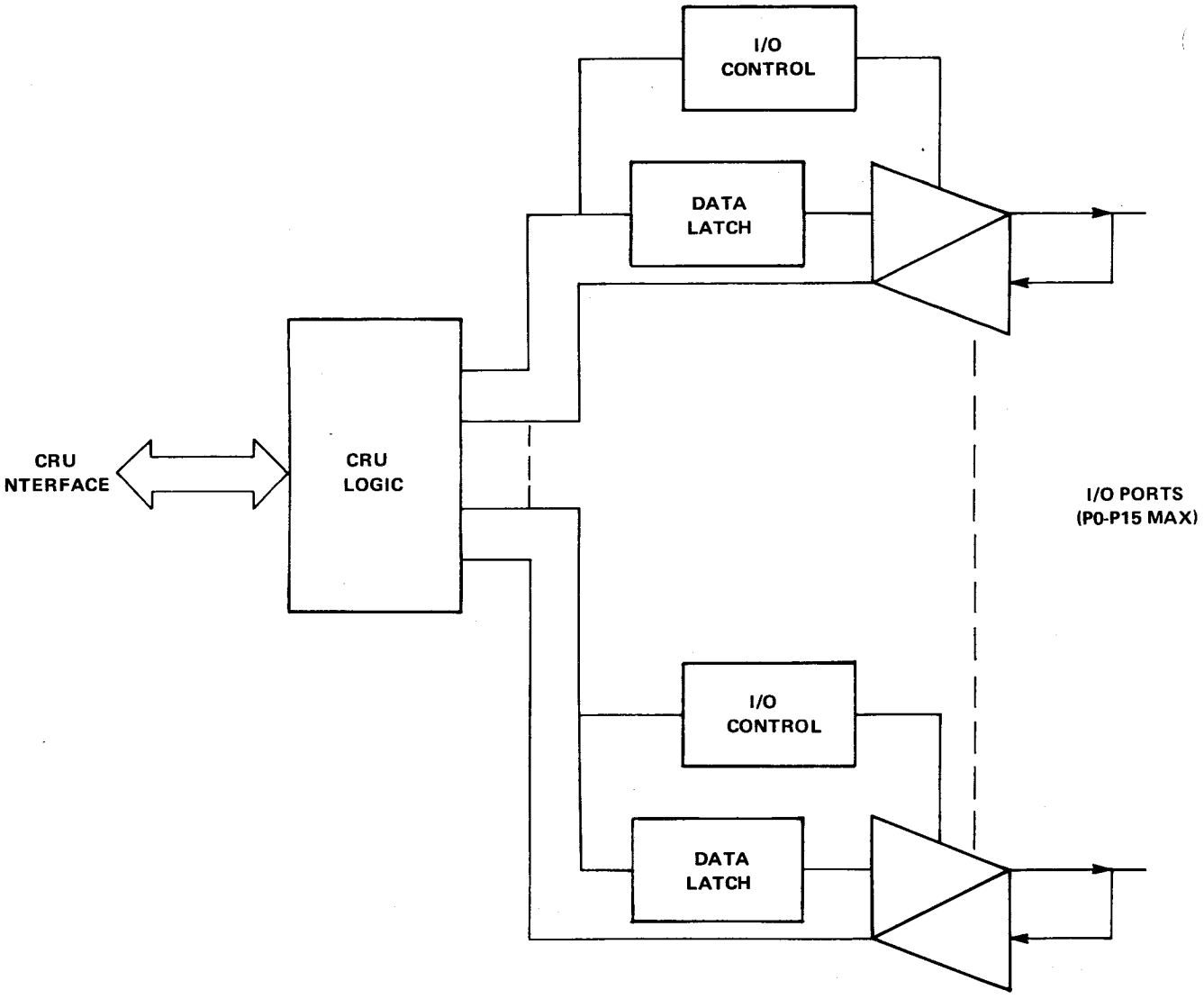


FIGURE 4–TMS 9901 I/O INTERFACE SECTION

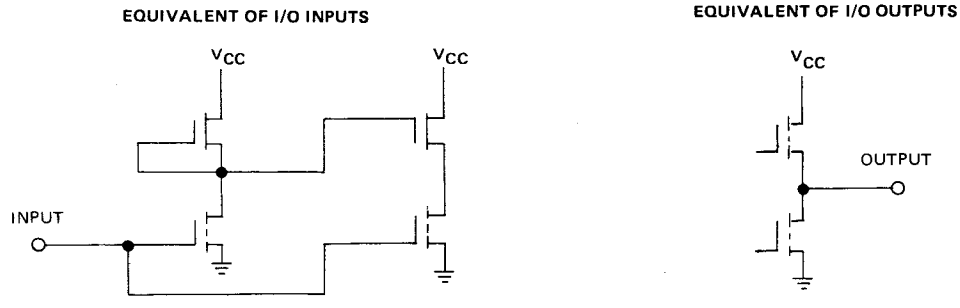


FIGURE 5 – INPUT AND OUTPUT EQUIVALENTS

2.4 Programmable Ports

A total of nine pins ($\overline{INT}$7/P15-$\overline{INT}$15/P7) on the TMS 9901 are user-programmable as either I/O ports or interrupts. These pins will assume all characteristics of the type pin they are programmed to be (as described in Sections 2.2 and 2.3). Any pin which is not being used for interrupt should have the appropriate interrupt mask disabled (mask = 0) to avoid erroneous interrupts to the CPU. To program one of the pins as an interrupt, its interrupt mask simply is enabled and the line may be used as if it were one of the dedicated interrupt lines. To program a pin as an I/O port, disable the interrupt mask and use that pin as if it were one of the dedicated I/O ports.

2.5 Interval Timer

Figure 6 is a block diagram of the TMS 9901 interval timer section. The clock consists of a 14-bit counter that decrements at a rate of $f(\overline{\phi})/64$ (at 3 MHz this results in a maximum interval of 349 milliseconds with a resolution of 21.3 microseconds). The clock can be used as either an interval timer or an event timer. To access the clock, select bit zero (control bit) must be set to a one. The clock is enabled to cause interrupts by writing a nonzero value to it and is then disabled from interrupting by writing zero to it or by a $\overline{RST}$1. The clock starts operating at no more than two ϕ times after it is loaded. When the clock decrementer is running, it will decrement down to zero and issue a level-3 interrupt. The decrementer, when it becomes zero, will also be reloaded from the clock register and decrementing will start again. (The zero state is counted as any other decrementer state.) The decrementer always runs, but it will not issue interrupts unless enabled; of course, the contents of the unenabled clock read register are meaningless.

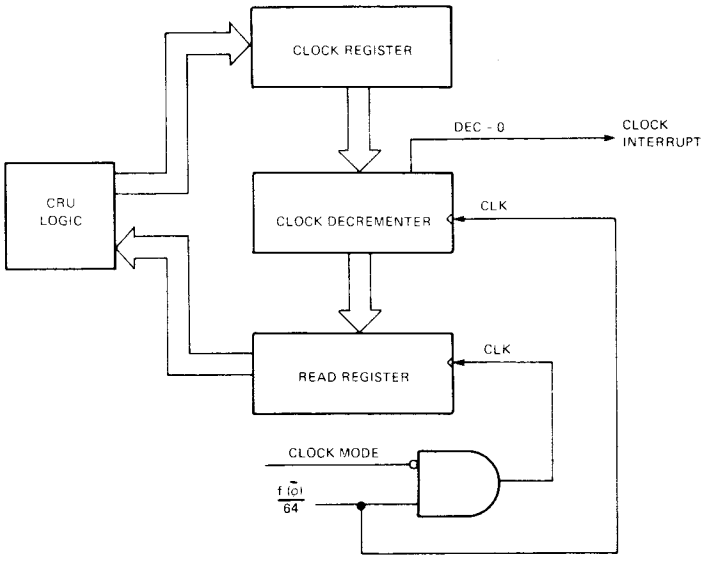


FIGURE 6–TMS 9901 INTERVAL TIMER SECTION

The clock is accessed by writing a one into the control bit (TMS 9901 CRU bit zero) to force CRU bits 1-15 to clock mode. Writing a nonzero value into the clock register then enables the clock and sets its time period. When the clock is enabled, it interrupts on level 3 and external level-3 interrupts are disabled. The mask for level 3 in the PSI must be set to a one so that the processor will see the clock interrupt. When the clock interrupt is active, the clock mask (mask bit 3) must be written into with either a one or zero to clear the interrupt; writing a zero also disables further interrupts.

If a new clock value is required, a new 14-bit clock start value can be programmed by executing a CRU write operation to the clock register. During programming, the decrementer is restarted with the current start value after each start value bit is written. A timer restart is easily implemented by writing a single bit to any of the clock bits. The clock is disabled by $\overline{RST1}$ (power up reset) or by writing a zero value into the clock register; $\overline{RST2}$ does not affect the clock.

The clock read register is updated every time the decrementer decrements when the TMS 9901 is not in clock mode. There are two methods to leave the clock mode : first, a zero is written to the control bit; or second, a TMS 9901 select bit greater than15 is accessed. Note that when $\overline{CE}$ is inactive(HIGH),the PSI is not disabled from seeing the select lines. As the CPU is addressing memory, A10-A14 could very easily have a value of 15 or greater — A10-A14 are connected to the select lines; therefore, the TMS 9901 interval timer section can "think" it is out of clock mode and update the clock read register. Very simply, this means that a value cannot be locked into the clock read register by writing a one to CRU select bit zero (the control bit). The 9901 must be out of clock mode for at least one timer period to ensure that the contents of the clock read register has been updated. This means that to read the most recent contents of the decrementer, just before reading, the TMS 9901 *must* not be in the clock mode. The only sure way to manipulate clock mode is to use the control bit (select bit zero). When clock mode is reentered to access the clock read register, updating of the read register will cease. This is done so that the contents of the clock read register will not change while it is being accessed.

2.6 Power-Up Considerations

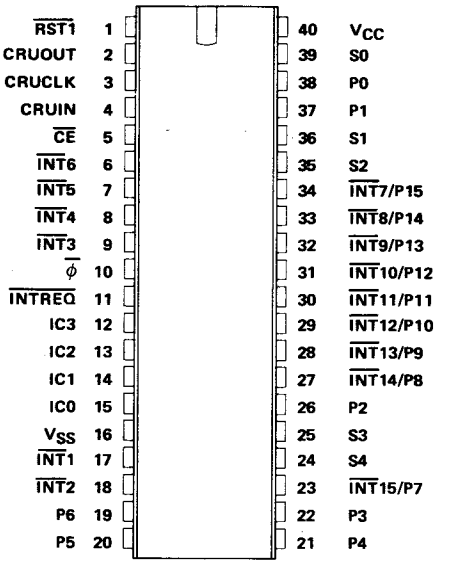
During hardware reset, $\overline{RST1}$ must be active (LOW) for a minimum of two clock cycles to force the TMS 9901 into a known state. $\overline{RST1}$ will disable all interrupts, disable the clock, program all I/O ports to the input mode, and force IC0-IC3 to all zeros with $\overline{INTREQ}$ held HIGH. The system software must enable the appropriate interrupts, program the clock, and configure the I/O ports as required. After initial power-up the TMS 9901 is accessed only as needed to service the clock, enable (disable) interrupts, or read (write) data to the I/O ports. The I/O ports can be reconfigured by use of the $\overline{RST2}$ software reset command bit.

2.7 Pin Descriptions

Table 4 defines the TMS 9901 pin assignments and describes the function of each pin.

TABLE 4
TMS 9901 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{INTREQ}$	11	OUT	INTERRUPT Request. When active (low) $\overline{INTREQ}$ indicates that an enabled interrupt has been received. $\overline{INTREQ}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0-IC3 output the binary code corresponding to the highest priority enabled interrupt. If no enabled interrupts are active IC0–IC3 = (1,1,1,1).
IC1	14	OUT	
IC2	13	OUT	
IC3 (LSB)	12	OUT	
$\overline{CE}$	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. $\overline{CE}$ has no effect on the interrupt control section.
S0	39	IN	Address select lines. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0-S4.
S1	36	IN	
S2	35	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{CE}$ is not active CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{CE}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0-S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{RST1}$	1	IN	Power Up Reset. When active (low) $\overline{RST1}$ resets all interrupt masks to "0", resets IC0 – IC3 = (0, 0, 0, 0), $\overline{INTERQ}$ = 1, disables the clock, and programs all I/O ports to inputs. $\overline{RST1}$ has a Schmitt-triger input to allow implementation with an RC circuit as shown in Figure 7.
V_{CC}	40		Supply Voltage. +5 V nominal.
V_{SS}	16		Ground Reference
$\overline{\phi}$	10	IN	System clock ($\overline{\phi}3$ in TMS 9900 system, $\overline{CKOUT}$ in TMS 9980 system).
$\overline{INT1}$	17	IN	Group 1, interrupt inputs. When active (Low) the signal is ANDed with its corresponding mask bit and if enabled sent to the interrupt control section. $\overline{INT1}$ has highest priority.
$\overline{INT2}$	18	IN	
$\overline{INT3}$	9	IN	
$\overline{INT4}$	8	IN	
$\overline{INT5}$	7	IN	
$\overline{INT6}$	6	IN	
$\overline{INT7}$/ P15	34	I/O	Group 2, programmable interrupt (active low) or I/O pins (true logic). Each pin is individually programmable as an interrupt, an input port, or an output port.
$\overline{INT8}$/ P14	33	I/O	
$\overline{INT9}$/ P13	32	I/O	
$\overline{INT10}$/P12	31	I/O	
$\overline{INT11}$/P11	30	I/O	
$\overline{INT12}$/P10	29	I/O	
$\overline{INT13}$/P9	28	I/O	
$\overline{INT14}$/P8	27	I/O	
$\overline{INT15}$/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as an input port or an output port.
P1	37	I/O	
P2	26	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	



3. APPLICATIONS

3.1 Hardware Interface

Figure 7 illustrates the use of a TMS 9901 PSI in a TMS 9900 system. The TIM 9904 clock generator/driver syncs the $\overline{\text{RESET}}$ for both the TMS 9901 and the CPU. The RC circuit on the TIM 9904 provides the power-up and pushbutton $\overline{\text{RESET}}$ input to the clock chip. Address lines A0-A9 are decoded on CRU cycles to select the TMS 9901. Address lines A10-A14 are sent directly to PSI select lines S0-S4, respectively, to select which TMS 9901 CRU bit is to be accessed.

Figure 8 illustrates the use of a TMS 9901 with a TMS 9981 CPU. No TIM 9904 is needed with the TMS 9981, so the reset circuitry is connected directly to the system reset line. The clock ($\overline{\phi}$) then comes from the TMS 9981. All other circuitry is identical to the TMS 9900 system.

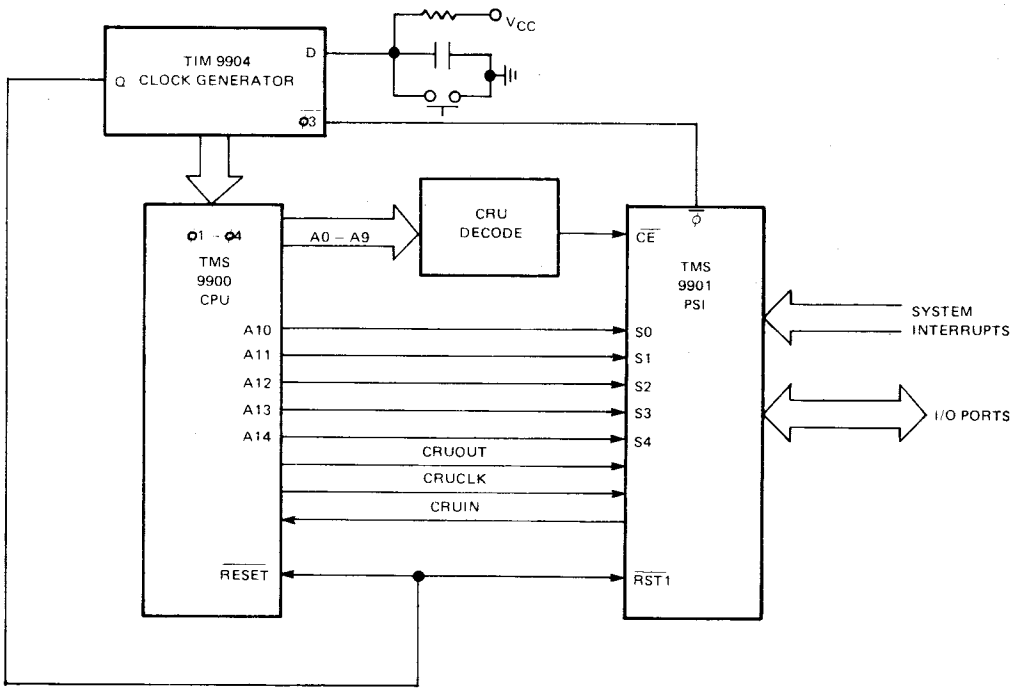


FIGURE 7–TMS 9900/TMS 9901 INTERFACE

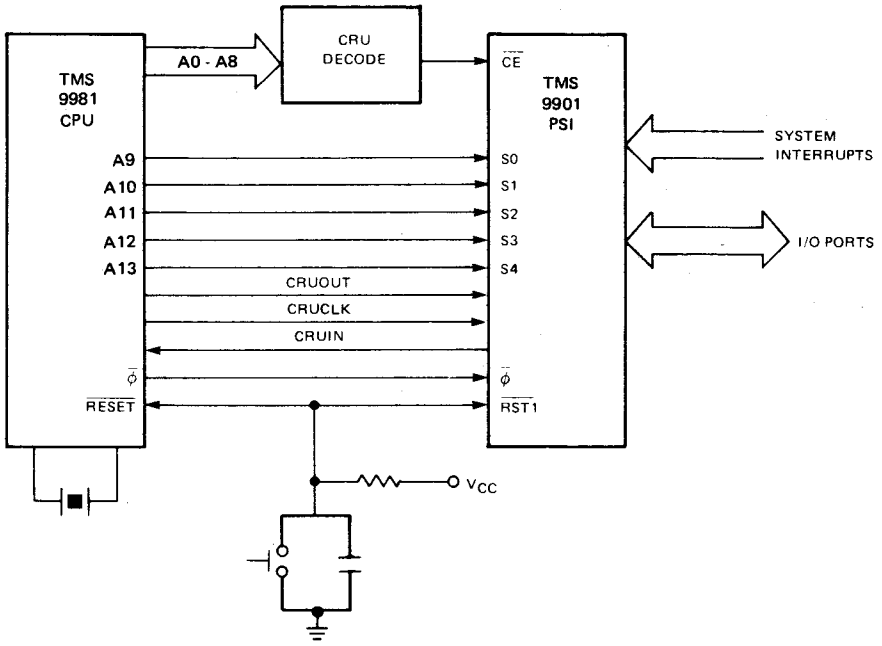


FIGURE 8—TMS 9981/TMS 9901 INTERFACE

3.2 Software Interface

Figure 9 lists the TMS 9900 code needed to control the TMS 9901 PSI. The code initializes the PSI to an eight-bit input port, an eight-bit output port, and enables interrupt levels 1-6. The six dedicated interrupt pins are all used for interrupts; their mask bits are set ON. The nine programmable pins are all used as I/O ports; mask bits 7-15 remain reset. P0-P7 are programmed as an eight-bit output port, and P8-P15 are programmed as an eight-bit input port.

Some code is added to read the contents of the clock read-register. The SBZ instruction takes the TMS 9901 out of clock mode long enough for the clock read register to be updated with the most recent decrementer value. When clock mode is reentered, the decrementer will cease updating the clock read-register so that the contents of the register will not be changing during a read operation.

The second section of code is typical code found in a clock interrupt service routine. All interrupts initially are disabled by the routine. These functions are not necessary, but are usually done to ensure system integrity. The interrupt mask should be restored as soon as the sensitive processing is complete. The interrupt is counted in the variable COUNT and is then cleared by writing a one to mask bit 3. If a zero is written to mask bit 3 to clear the interrupt, clock interrupt will be disabled from that point onward, but the clock will continue to run.

ASSUMPTION:

- System uses clock at maximum interval (349 msec @ 3MHz)
- Interrupts 1-6 are used
- Eight bits are used as an output port , P0 –P7
- Eight bits are used as an input port , P8 – P15
- $\overline{\text{RST}}$1 (power-up reset) has been applied
- The most significant byte of R1 contains data to be output.

```
        LI      R12, PSIBAS     Set up CRU base to point to 9901
        LDCR    @CLKSET, 0      16-bit transfer, set clock to max interval

        LDCR    @INTSET, 7      Enter interrupt mode and enable interrupts 1 – 6

        LI      R12, PSIBAS+32  Set CRU base to I/O ports – output
        LDCR    R1, 8           Output byte from R1, program ports 0 – 7 as output

        LI      R12, PSIBAS+48  Set CRU base to I/O ports – input
        STCR    R2, 8           Store a byte from input port into MSBT of R2

        LI      R12, PSIBAS     Set CRU base to 9901
        SBZ     0               Leave clock mode so decremented contents can be latched
        INCT    R12             Set CRU base to clock read register
        SBO     -1              Enter clock mode
        STCR    R3, 14          Read 14-bit clock read register contents into R3

CLKSET  DATA    >FFFF
INTSET  BYTE    >7E

CLKINT  S                       Clock interrupt service routine – level 3
        LIMI    0               Disable interrupts at CPU
        INC     @COUNT          Count the clock interrupt
        LI      R12, PSIBAS     Set CRU base to point to 9901
        SBZ     0               Enter interrupt mode
        SBO     3               Clear clock interrupt
```

FIGURE 9 – TMS 9900 SAMPLE SOFTWARE TO CONTROL THE TMS 9901

3.3 Interval Timer Application

A TM 990/100M microcomputer board application in which every 10 seconds a specific task must be performed is described below. The TMS 9901 clock is set to interrupt every 333.33 milliseconds. This is accomplished by programming the 14-bit clock register to $3D09_{16}$ ($15{,}625_{10}$). The TM 990/100M microcomputer board system clock runs at 3 MHz, giving a clock resolution of 21.33 microseconds. A decrementer period of 21.33 microseconds multiplied by 15,625 periods until interrupt gives 333.33 milliseconds between interrupts. The interrupt service routine must count 30 interrupts before 10 seconds elapses:

$$f_{(DEC)} = \frac{f_{(O)}}{64}, \qquad T_{(DEC)} = \frac{1}{f_{(DEC)}} = \frac{64}{3{,}000{,}000} = 21.3333\ \mu s$$

Figure 10 is a flowchart of the software required to perform the above application, and Figure 11 is a listing of the code. Following the flowchart, the main routine sets up all initial conditions for the 9901 and clock service routine. The interrupt service routine decrements a counter in R2 which was initialized to 30. When the counter in R2 decrements to zero, 10 seconds have elapsed, and the work portion of the service routine is entered. Note carefully that the work portion of the service routine takes longer than 333.33 ms which is the time between clock interrupts from the 9901. Therefore, recursive interrupts are going to occur and some facility must be provided to handle them. Loading a new workspace pointer and transferring the saved WP, PC, and ST (R13-R15) from the interrupt workspace to the new workspace allows one level of recursion.

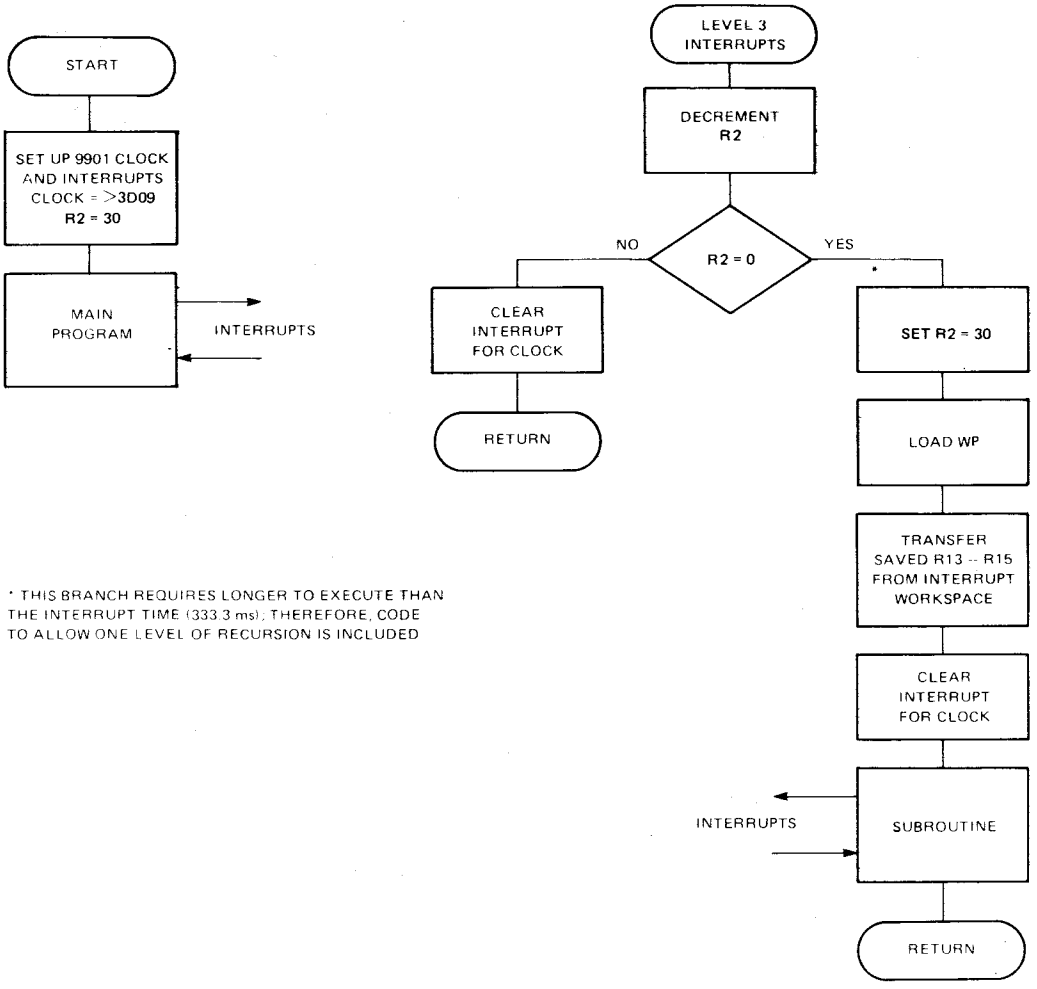


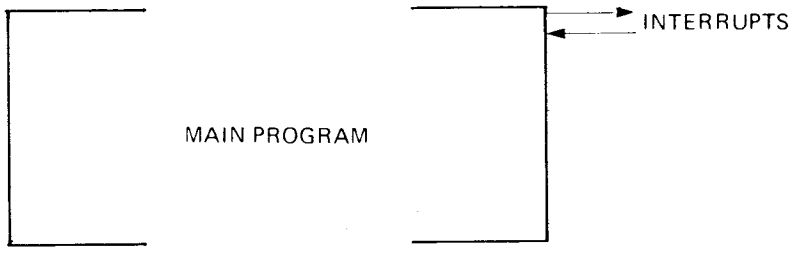
FIGURE 10–TMS 9901 INTERVAL TIMER APPLICATION FLOWCHART

DEVICE INITIALIZATION

```
FE00 02E0 LWPI >FF20
FE02 FF20
FE04 020C LI R12,>100    9901 CRU BASE ADDRESS
FE06 0100
FE08 02E0 LWPI >FF68     INTERRUPT 3 WORKSPACE
FE0A FF68
FE0C 0201 LI R1,>7A13    DATA FOR 333.33MS CLOCK
FE0E 7A13
FE10 0202 LI R2,30       30 X 333.33MS = 10SEC
FE12 001E
FE14 020C LI R12,>100    9901 CRU BASE ADDRESS
FE16 0100
FE18 3301 LDCR R1,15     LOAD 9901 CLOCK
FE1A 1E00 SBZ 0          SET 9901 TO INTERRUPT MODE
FE1C 1D03 SBO 3          UNMASK INTERRUPT 3
```

MAIN PROGRAM

```
FD00 02E0 LWPI >FF00     MAIN PROGRAM WORKSPACE
FD02 FF00
FD04 0300 LIMI 3         ENABLE INT 0-3
FD06 0003
```



NOTE: This code was assembled using the TM 990/402 line-by-line assembler.

FIGURE 11–INTERVAL TIMER

INTERRUPT 3 SERVICE ROUTINE
(WP = FF68)

```
FD80 0602 DEC R2          COUNT DOWN 30 IN R2
FD82 1302 JEQ >FD88       IF ZERO THEN JUMP
FD84 1D03 SBO 3           CLEAR 9901 CLOCK INTERRUPT
FD86 0380 RTWP            RETURN TO INTERRUPTED ROUTINE
FD88 0202 LI R2,30        RELOAD R2 FOR 10 SEC COUNT DOWN
FD8A 001E
FD8C 0460 B @>FC80        BRANCH TO SUBROUTINE
FD8E FC80
```

ROUTINE TO BE PERFORMED EVERY 10 SECONDS, IT TAKES
LONGER THAN 333.33 MS WHICH IS 9901 CLOCK PERIOD'

```
FC80 02E0 LWPI >FF20      WORKSPACE FOR SUBROUTINE
FC82 FF20
FC84 C360 MOV @>FF82,R13 TRANSFER SAVED WP,PC,ST FROM
FC86 FF82
FC88 C3A0 MOV @>FF84,R14 INT 3 WORKSPACE
FC8A FF84
FC8C C3E0 MOV @>FF86,R15
FC8E FF86
FC90 1D03 SBO 3           CLEAR 9901 CLOCK INTERRUPT
FC92 0300 LIMI 3          ENABLE INT 0-3
FC94 0003
```


```
FEC0        RTWP
```

FIGURE 11–(CONCLUDED)

4. TMS 9901 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply voltage, V_{CC} ..... −0.3 V to 10 V
All inputs and output voltages ..... −0.3 V to 10 V
Continuous power dissipation ..... 0.85 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions*

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5.0	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.0		V_{CC}	V
Low-level input voltage, V_{IL}	V_{SS}−.3		0.8	V
Operating free-air temperature, T_A	0		70	°C

4.3 Electrical Characteristics Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = −100 μA	2.4		V_{CC}	V
		I_{OH} = −200 μA	2.2		V_{CC}	V
V_{OL}	Low level output voltage	I_{OL} = 3.2 mA	V_{SS}		0.4	V
I_I	Input current (any input)	V_I = 0 V to V_{CC}			±100	μA
$I_{CC(av)}$	Average supply current from V_{CC}	$t_{c(\phi)}$ = 330 ns, T_A = 70°C			150	mA
C_I	Small signal input capacitance, any input	f = 1 MHz			15	pF

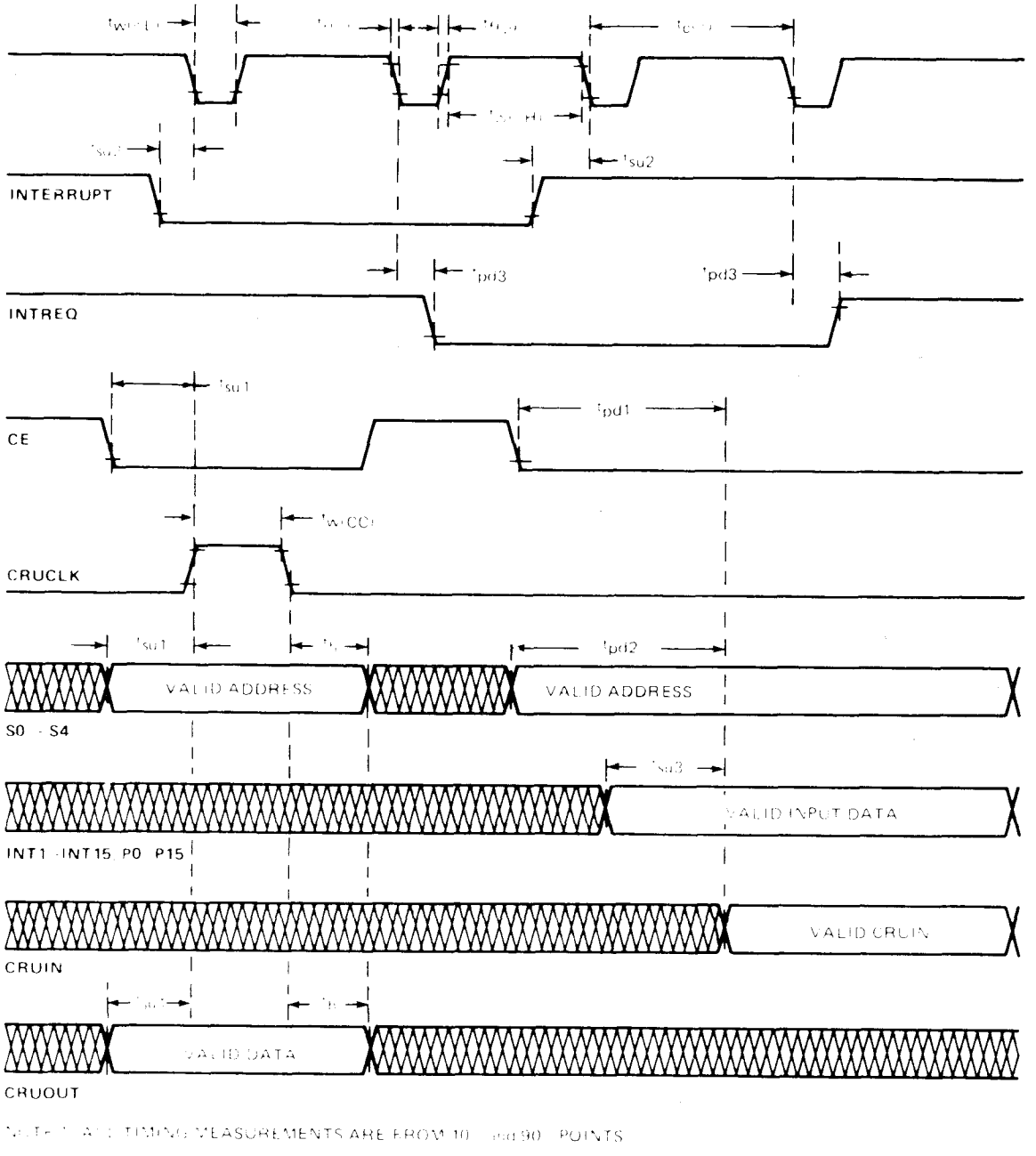
4.4 Timing Requirements Over Full Range of Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time	300	333	2000	ns
$t_{r(\phi)}$	Clock rise time	5		40	ns
$t_{f(\phi)}$	Clock fall time	10		40	ns
$t_{w(\phi H)}$	Clock pulse width (high level)	225			ns
$t_{w(\phi L)}$	Clock pulse width (low level)	45		300	ns
$t_{w(CC)}$	CRUCLK pulse width	100	185		ns
t_{su1}	Setup time for $\overline{CE}$, S0-S4, or CRUOUT before CRUCLK	100			ns
t_{su2}	Setup time for interrupt before $\overline{\phi}$ low	60			ns
t_{su3}	Setup time for inputs before valid CRUIN	200			ns
t_h	Hold time for $\overline{CE}$, S0-S4, or CRUOUT after CRUCLK	60			ns

*NOTE: All voltage values are referenced to V_{SS}.

4.5 Switching Characteristics Over Full Range of Recommended Operating Conditions

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay, $\overline{CE}$ to valid CRUIN	C_L = 100 pF			300	ns
t_{pd2}	Propagation delay, S0-S4 to valid CRUIN	C_L = 100 pF			320	ns
t_{pd3}	Propagation delay, $\overline{\phi}$ low to valid $\overline{INTREQ}$, IC0-IC3	C_L = 100 pF			110	ns
t_{pd}	Propagation delay, $\overline{CRUCLK}$ to valid data out (P0-P15)	C_L = 100 pF			300	ns



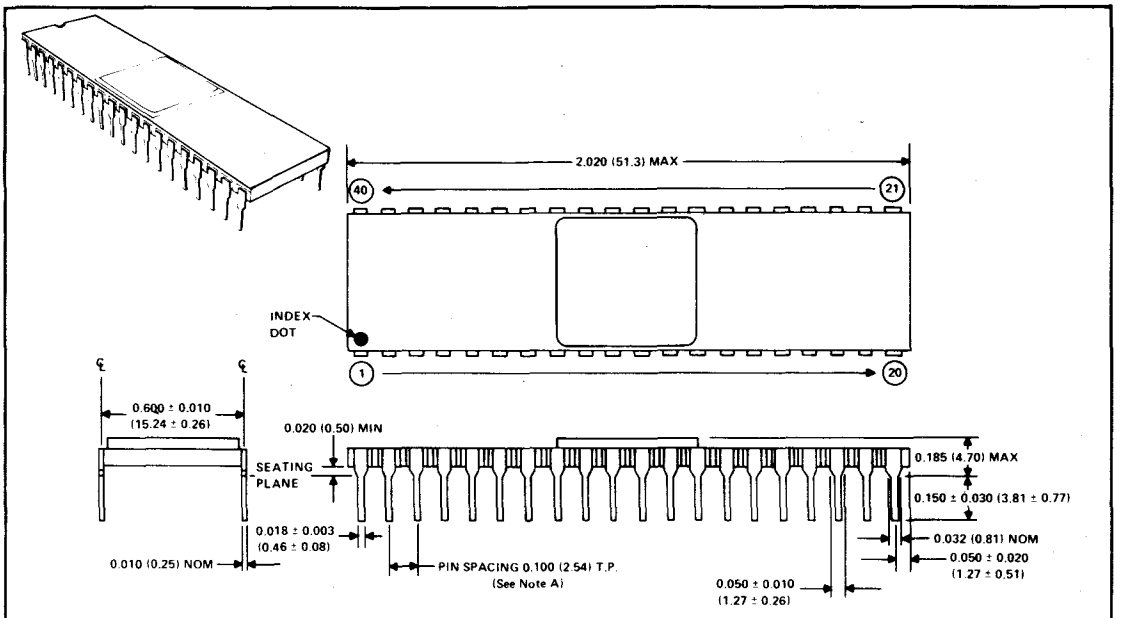
NOTE: A.C. TIMING MEASUREMENTS ARE FROM 10% TO 90% POINTS

FIGURE 12–SWITCHING CHARACTERISTICS

5. MECHANICAL DATA

5.1 TMS 9901 JL — 40 Pin Ceramic Package

ceramic packages with side-brazed leads and metal or epoxy or glass lid seal



NOTES: a. Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.
b. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
c. The index is placed in this area to identify pin 1 and to provide other information as follows:

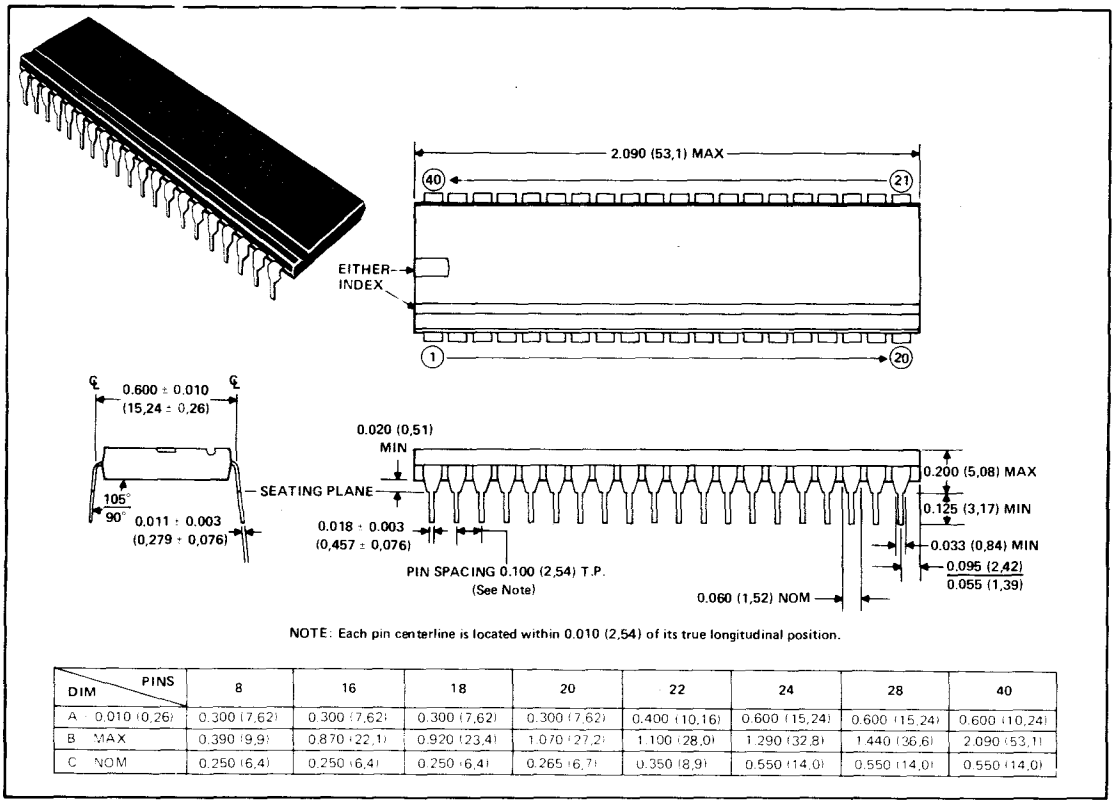
1 Pin 1 connected to chip-mounting pad.
ΔXX Pin XX connected to chip-mounting pad.
• No connection to chip-mounting pad.

Other symbols may indicate any combination of up to 4 pins connected to the chip-mounting pad.

DIM \ PINS	16	18	20	22	24	28	40
A ± 0.010 (0.26)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.400 (10,16)	0.600 (15,24)	0.600 (15,24)	0.600 (15,24)
B MAX	0.840 (21,4)	0.910 (23,1)	1.020 (25,9)	1.100 (28,0)	1.290 (32,8)	1.415 (36,0)	2.020 (51,3)
C NOM	0.290 (7,4)	0.290 (7,4)	0.290 (7,4)	0.390 (9,9)	0.590 (15,0)	0.590 (15,0)	0.590 (15,0)

5.2 TMS 9901 NL – 40 Pin Plastic Package

plastic packages



NOTE: Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.

DIM \ PINS	8	16	18	20	22	24	28	40
A ± 0.010 (0,26)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.400 (10,16)	0.600 (15,24)	0.600 (15,24)	0.600 (10,24)
B MAX	0.390 (9,9)	0.870 (22,1)	0.920 (23,4)	1.070 (27,2)	1.100 (28,0)	1.290 (32,8)	1.440 (36,6)	2.090 (53,1)
C NOM	0.250 (6,4)	0.250 (6,4)	0.250 (6,4)	0.265 (6,7)	0.350 (8,9)	0.550 (14,0)	0.550 (14,0)	0.550 (14,0)

INDEX

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