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The Engineering Staff of
TEXAS INSTRUMENTS LIMITED
Semiconductor Group

TMS5110A VOICE SYNTHESIS PROCESSOR DATA MANUAL

May 1982
DM-11

TEXAS INSTRUMENTS

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1. INTRODUCTION

The TMS5110A is a PMOS Voice Synthesis Processor (VSP). Speech is synthesized by processing an externally provided variable data-rate bit stream of encoded speech data and converting the result to an audible output with an on-chip eight-bit D/A converter and push-pull amplifier. The TMS5110A is designed to work with up to sixteen TMS6100 128K-bit (ROM) or up to four TMS6125 32K-bit (ROM) Voice Synthesis Memories (VSM). The TMS5110A outputs all control signals necessary for direct control of the VSP which is provided by an external device (e.g. TMS1000) through four control pins and a command clock.

2. THEORY OF OPERATION

2.1 LINEAR PREDICTIVE CODING

LPC synthesizes human speech by recovering from the original speech enough data to construct a time-varying digital filter model of the vocal tract. This filter is excited with a digital representation of either glottal air impulses (voiced sound) or the rush of air, which produces unvoiced sounds. The output of this filter model is passed through an 8-bit digital-to-analog (D/A) converter to produce a synthetic speech waveform. The TMS5110A performs all of these operations.

The TMS5110A design is based on a 40 hertz input frame rate (the rate at which new speech data — a maximum of 49 bits/frame — is obtained from the vocabulary memories). The output speech waveform from the D/A converter changes at an 8 kHz rate, which corresponds to a maximum speech output frequency of 4 kHz. Each 49-bit frame defines excitation and filter characteristics that are linearly interpolated (every 3.125 milliseconds) to be smoothly time-varying throughout the 25-millisecond interval between frames. This allows a 1960 bit/second maximum data rate to produce high-quality speech. The data rate is actually slower than this since certain parameters are not necessary in some instances, as described in the next section. Each 49-bit frame is composed of 13 parameters:

(1) Energy (amplitude — four bits)
(2) Repeat bit
(3) Pitch (fundamental frequency — five bits)
(4) Ten reflection coefficients (K-parameters-K1 and K2, five bits each; K3-K7, four bits each; K8-K10, three bits each)

The K parameters define the vocal transfer function.

A full set of parameters for each frame would require a data rate of 40 Hz × 49 bits = 1960 bit/second. Three special cases, in which a full frame is not necessary, allow the data rate to be considerably reduced:

(1) Since the vocal tract changes shape relatively slowly, it is often possible to repeat previous reflection coefficient data. If the repeat bit is set to a 1, the K parameters from the previous frame are used and no more data is accessed from memory. This makes repeated frames only 10 bits in length (4 energy, 1 repeat, 5 pitch.)

(2) Unvoiced sounds (such as s, f, t, sh) require fewer reflection coefficients. When pitch = 00000, only K1-K4 are used. K5-K10 are internally zeroed, making an unvoiced frame of 28 bits (4 energy, 1 repeat, 5 pitch, K1 and K2 — five bits each, K3 and K4 — four bits each).

(3) When energy = 0000, no other data is required. Energy is zero during interword or intersyllable pauses. When energy = 1111, it is detected as an end-of-phrase and the TMS5110A stops talking. Both of these cases yield a four-bit frame.

The combination of these three cases has reduced the average data rate to nominally 1200 bits/sec.

EXAMPLE PHRASE — "TEN"

Table 1 shows the word "TEN" bit by bit, frame by frame.

TABLE 1 — "TEN"

The following 16 frames is a display of coded analyzed speech:

Frame	Erms	Ec	Pitch	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
1.	821.	8	0	24	2	7	5						
2.	1011.	8	0	18	6	3	5						
3.	1357.	12	16	20	10	4	10	8	9	5	1	2	3
4.	3523.	14	15	21	14	5	7	7	11	10	3	2	3
5.	3559.	14	16	20	14	5	10	8	12	11	4	2	3
6.	2734.	14	17	21	13	6	7	7	10	10	6	1	4
7.	2460.	14	18	23	14	7	7	5	6	9	6	2	3
8.	1831.	14	21	23	14	7	7	5	5	8	6	2	3
9.	2164.	14	25	23	11	11	7	4	8	8	6	3	3
10.	1553.	13	26	21	13	11	5	4	8	10	6	2	4
11.	625.	11	27	19	18	6	3	5	9	10	4	3	3
12.	190.	8	28	19	6	4	6	12	5	8	4	2	5
13.	197.	7	29	19	6	4	6	12	5	8	4	2	5
15.	134.	7	30	19	7	5	5	12	7	8	4	2	5
16.	110.	6	30	21	6	4	3	12	9	7	5	2	5

The following 16 frames is a binary pattern equiv. to the above:

Frame	Ec	R	Pitch	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
1.	1000	0	00000	11000	00010	0111	0101						
2.	1000	0	00000	10010	00110	0011	0101						
3.	1100	0	10000	10100	01010	0100	1010	1000	1001	0101	001	010	011
4.	1110	0	01111	10101	01110	0101	0111	0111	1011	1010	011	010	011
5.	1110	0	10000	10100	01110	0101	1010	1000	1100	1011	100	010	011
6.	1110	0	10001	10101	01101	0110	0111	0111	1010	1010	110	001	100
7.	1110	0	10010	10111	01110	0111	0111	0101	0110	1001	110	010	011
8.	1110	1	10101										
9.	1110	0	11001	10111	01011	1011	0111	0100	1000	1000	110	011	011
10.	1101	0	11010	10101	01101	1011	0101	0100	1000	1010	110	010	100
11.	1011	0	11011	10011	10010	0110	0011	0101	1001	1010	100	011	011
12.	1000	0	11100	10011	00110	0100	0110	1100	0101	1000	100	010	101
13.	0111	1	11101										
14.	0111	0	11110	10011	00111	0101	0101	1100	0111	1000	100	010	101
15.	0110	0	11110	10101	00110	0100	0011	1100	1001	0111	101	010	101
16.	1111												

2.2 TMS5110A

The TMS5110A is controlled by commands on five pins: the Control Bus (CTL 1,2,4,8) and the processor data clock (PDC) (see Table 2). A command is first set up on the Control Bus (with the PDC low), then strobed into the device by toggling the PDC (low - high - low). Multi-nibble commands, such as Load Address, are executed by strobing in the command first, then setting up the data on the Control Bus and toggling the PDC. The beginning of each command description gives the binary form of each command.

TABLE 2 — TMS5110A COMMAND LIST

NAME	CONTROL BUS CONTENTS CTL8 (MSB)	CTL4	CTL2	CTL1 (LSB)	PDC'S REQUIRED
RESET	0	0	0	X	1
LOAD ADDRESS	0	0	1	X	2
OUTPUT	0	1	0	X	3
READ BIT	1	0	0	X	1
SPEAK	1	0	1	X	1
READ & BRANCH	1	1	0	X	1
TEST TALK	1	1	1	X	3

X — don't care

RESET

The Reset command (000X) is used to synchronize a command sequence. Since there are some multi-nibble commands (such as Load Address, which requires a Load Address command followed by address data), the TMS5110A may not be ready to accept a command, for example, when the device is expecting data in a load address sequence. The Reset command must be executed three times to ensure that the next toggling of the PDC will strobe in a command, not data.

The Reset command can also be used to halt speech. The execution of the Reset command while the TMS5110A is talking completely halts the device, but does not clear any internal registers. This allows the rest of the phrase to be spoken upon subsequent execution of the Speak command.

LOAD ADDRESS

This command (001X) loads the address of a phrase contained in the VSM. This is a two-nibble command, the first nibble is the Load Address command (001X). Once this has been toggled in, the TMS5110A expects the data on the Control Bus to be four address bits. Upon toggling the PDC, the chip gates this address (along with the proper control signals) to the VSM. This two-nibble sequence is repeated as many times as necessary to complete loading of the VSM address register. For example, the TMS6100 requires five Load Address sequences, i.e., it takes exactly ten toggles of the PDC to load an address.

READ & BRANCH

This instruction (110X) is an indirect load address command for a single ROM system. The first step is to load an address. This is the address of a word in the VSM that contains the address of data that the user desires. The Read and Branch command is now executed and the VSM address register is loaded with the contents of the ROM byte (specified in the Load Address sequence) and the next consecutive byte. In this manner a look-up table of phrase addresses can be stored in the VSM and easily accessed. The execution of this command also performs a dummy read so that a Read Bit or Speak command can be immediately executed to access data or begin speech (Note: the addressed byte holds the MSB's of the VSM address. The next sequential byte holds the eight LSB's of the VSM address.) The VSM uses only the 14 LSB's of these two bytes, and therefore the Read and Branch command is local to only one VSM, i.e., a lookup table for data must be on the same chip as the data itself.

SPEAK

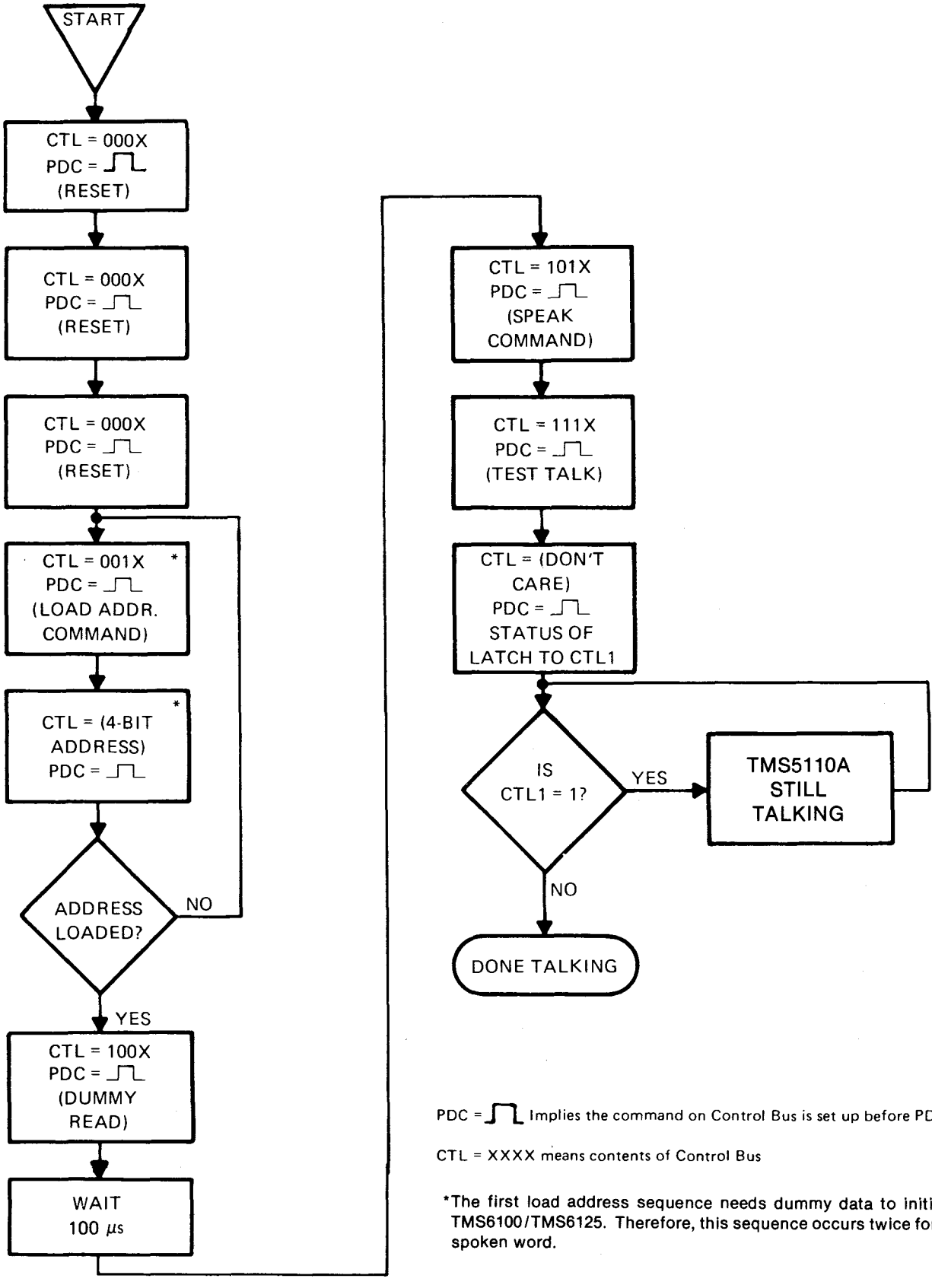
This command (101X) is used to start the TMS5110A talking. After an address has been loaded and a dummy read performed (see Figure 1), this command is toggled into the TMS5110A and it immediately begins transferring data from the VSM and talking. The speech can now be interrupted by the Reset command, if desired, and restarted later by simply toggling the Speak command into the device again. If no Reset command is issued during the speech, the device continues talking until it detects an end of phrase datum (energy = 1111).

TEST TALK

The Test Talk command (111X) was created so that the controlling device would know when the TMS5110A is finished talking. This is a three PDC command: the first PDC clocks in the command; the second gates the status of the talk latch in the device to CTL1 and enables the CTL output buffers; the third returns the CTL pins to inputs. After the falling edge of the second PDC, CTL1 will be high if the TMS5110A is talking. As soon as the device detects an end of phrase datum, it will go low indicating the end of speech. Note that no commands will be understood by the device until the third PDC is used, since the CTL output buffers are enabled. (See Figure 1). Also note that the method of issuing three Reset commands (see Reset command section) would also guarantee the next toggle of the PDC to mean a command exists on CTL.

READ BIT/OUTPUT

The Read Bit command (100X) is used for two reasons: (1) reading data out of the VSM in conjuction with the Output command (010X), and (2) changing the direction of the ADD8/Data line from VSP output to VSP input (a "dummy read" option prior to using a "Speak" command).



PDC = ⎍ Implies the command on Control Bus is set up before PDC high.

CTL = XXXX means contents of Control Bus

*The first load address sequence needs dummy data to initialize the TMS6100/TMS6125. Therefore, this sequence occurs twice for the first spoken word.

FIGURE 1 – OPERATION FLOW – TALK COMMAND SEQUENCE

Data can be read out of the VSM by:

(1) Loading a 20-bit address,
(2) Performing a dummy read,
(3) Performing four Read Bit commands sequentially to load the 4-bit data buffer in the TMS5110A
(4) Toggling the PDC with an Output command on CTL,
(5) Toggling the PDC again to reverse the CTL pins to outputs,
(6) Toggling the PDC again to return the CTL pins to inputs,
(7) Going to step 3 and repeating until all needed data is obtained

Data is transferred between the VSM and the speech synthesizer over the ADD8 pin. Since this pin is usually an input on the VSM and an output on the TMS5110A, a dummy read is required to reverse the data flow so that data is now transferred in the other direction. This need only be performed when a new address is loaded. The correct direction of the data flow will still be set in cases such as interrupted speech or in between sequential data reads (see M0-Transfer bit section).

3. OPERATION OF TMS5110A VSP WITH TMS6100 VSM / TMS6125 VSM.

This section is intended as an aid for those who may desire to interface the TMS6100 ROM / TMS6125 ROM to the TMS5110A. The following sections describe the timing of the control signals (ADD1, ADD2, ADD4, ADD8, ROMCLK, M0, and M1) that the TMS5110A provides to the ROM. It is suggested that the reader obtain a copy of the TMS6100/TMS6125 specification to further clarify this discussion.

DESCRIPTION OF THE TMS6100

The TMS6100 contains an auto-incrementing address register. No further load address sequences are needed if the data is sequentially positioned in the ROM. See Figure 2 for operation flow.

The TMS6100 is a mask-programmable PMOS 128K-bit Read-Only Memory internally organized as 16K words of 8 bits. Externally it appears as 128K × 1. Once the 20-bit address (14 bits to select a byte within the device, 4 chip select banks, 2 bits ignored) is loaded through ADD1, ADD2, ADD4, and ADD8 in five Load Address sequences, data is read out bit-wise by toggling a control pin M0. The ROM contains an on-chip address counter that is incremented every eight bits (eight toggles of M0). The four internal chip select banks are a mask-programmable option, and allow parallel connection of up to 16 ROMs (about 30 minutes of speech) without the need of external select circuitry.

DESCRIPTION OF THE TMS6125

The TMS6125 is a PMOS 32K ROM internally organized as 4K × 8. Externally it appears as a 1-bit serial output. Once the 16-bit address (12 bits to select a byte within the device, 2 chip select banks, 2 bits ignored) is loaded through ADD1, ADD2, ADD4, and ADD8 in four Load Address sequences, data is read out bit-wise by toggling a control pin M0. The address is internally incremented after 8 bits have been read. There is a mask programmable internal bank select option allowing parallel connection of up to 4 ROMs (16K bytes).

M1 — LOAD ADDRESS

The TMS5110A loads an address into the TMS6100/TMS6125 using the ADD bus and M1 control pin. As the PDC is brought high during the address portion of a load address sequence, the TMS5110A brings M1 high and gates the CTL bus to the ADD bus. When the PDC is brought low, M1 goes low and the VSM stores the nibble in its address register. This 18-bit register is filled after five toggles of M1 in the TMS6100 and 4 toggles in the TMS6125. (M1 stays low when the Load Address command (001 ×) is clocked in).

M0 — TRANSFER BIT

Data is transferred from the ROM to the TMS5110A over the ADD8 pin. Toggling M0 instructs the ROM to transfer the next required bit. As the PDC is brought high during a Read Bit command, the TMS5110A toggles M0 and accepts the new bit into its four-bit buffer over the ADD8 pin. The first M0 after a load address sequence changes the direction of the ADD8/Data line.

ROM CLOCK

The TMS5110A system oscillator clock is divided by four to generate ROMCLK, which is used as the input clock to the TMS6100 / TMS6125. To achieve maximum speech quality ROMCLK must be adjusted to match the data rate at which the particular TMS6100 / TMS6125 vocabulary was processed. A 40 hertz frame rate requires ROMCLK to be 160 ± 5% kHz.

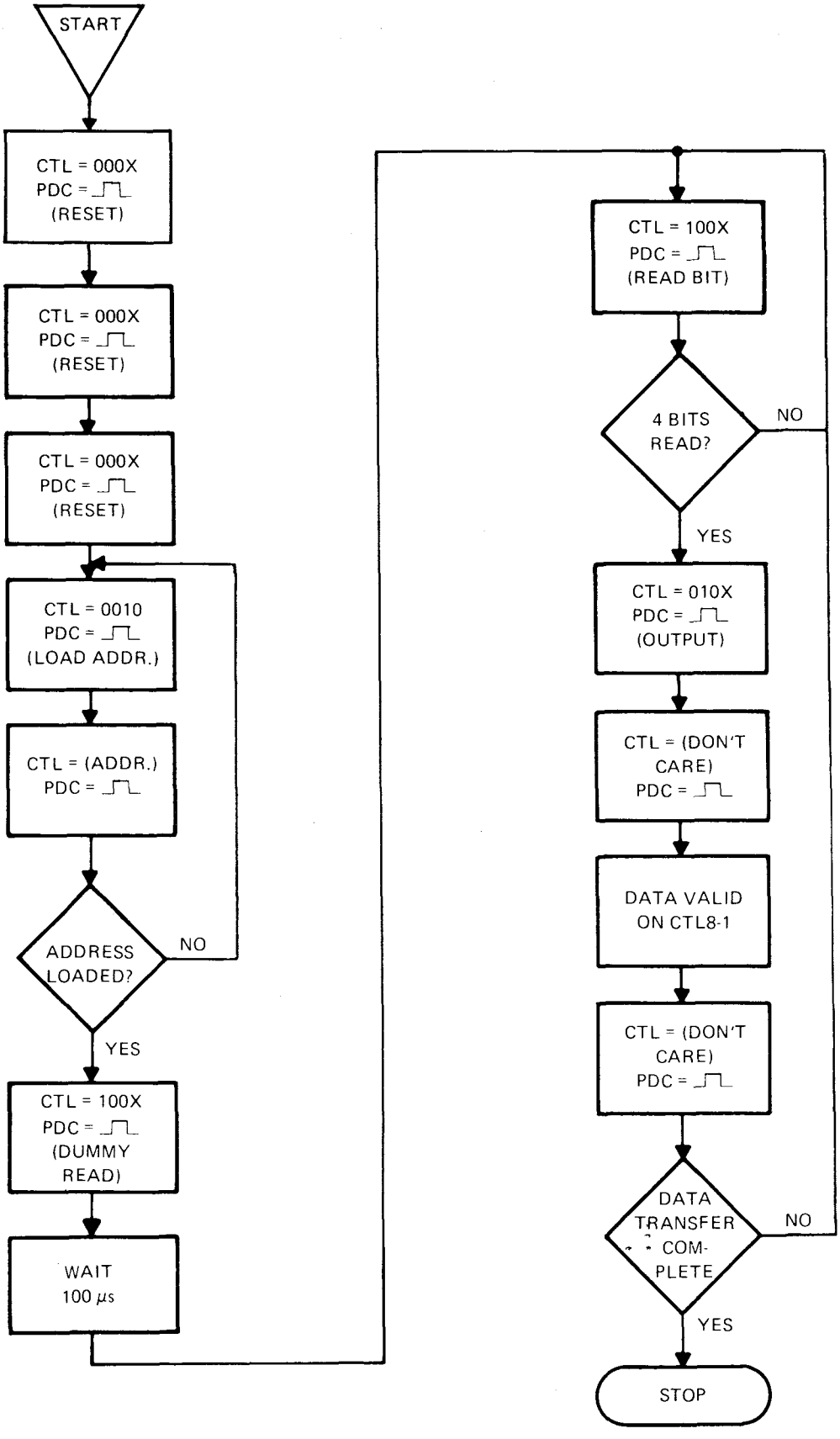


FIGURE 2 – OPERATION FLOW – READ/OUTPUT COMMAND SEQUENCE

4. TMS5110A SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS* OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply Voltage, V_{DD} (see Note 1) . . . . . −20 V to +0.3 V
Voltage applied to any device pin . . . . . −24 V to +0.3 V
Storage temperature . . . . . −30°C to +125°C
Operating temperature . . . . . 0°C to +70°C
Continuous power dissipation . . . . . 600 mW

NOTE 1: All voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or beyond those listed under the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

4.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	−8.3	−9	−9.7	V
High-level input voltage (see Note 2)	−0.7		0	V
Low-level input voltage (see Note 2)	V_{DD}		−4	V
Oscillator frequency (external RC)	608	640	674	kHz
Operating free-air temperature, T_A	0	25	70	°C

4.3 ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE, V_{DD} = −9 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX (See Note 2)	UNIT
V_{IH}	High-level input voltage	ADD8		−0.7		0	V
		CTL1, CTL2, CTL4, CTL8, PDC, CS		−0.95		0	
V_{IL}	Low-level input voltage, all inputs			−12		−4	V
V_{OH}	High-level output voltage	ROM CLK, CPU CLK, I0, I1, ADD1, ADD2, ADD4, ADD8	I_{OH} = −100 μA	−0.5		0	V
		CTL1, CTL2, CTL4, CTL8	I_{OH} = −400 μA	−0.7		0	
V_{OL}	Low-level output voltage, all outputs		I_{OL} = 100 μA	V_{DD}		−5	V
I_{IH}	High-level input current		V_I = 0 V			100	μA
I_{IL}	Low-level input current		V_I = −12V			−50	μA
I_{DD}	Supply current		All inputs and outputs open		−20	−35	mA
	Power output to speaker		100-Ω speaker load, 50-Ω each output	30			mW

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4.4 TIMING REQUIREMENTS, DATA OUTPUT AND I/O MODE SWITCHING (TEST TALK, OUTPUT) SEE FIGURE 3

PARAMETER		MIN	MAX	UNIT
t_{su}	CS setup time	0		μs
t_{wH}	Pulse width, PDC high	1		cycle
t_{wH}	Pulse width, PDC high, f_{osc} = 640 kHz	6.25		μs
t_{wL}	Pulse width, PDC low	1		cycle‡
t_{wL}	Pulse width, PDC low, f_{osc} = 640 kHz	6.25		μs

† Typical values are at T_A = 25°C.

‡ Cycle refers to the equivalent time in CPU clock cycles.

4.5 TIMING REQUIREMENTS, COMMAND AND DATA TRANSFER (LOAD ADDRESS, RESET, READ BIT, READY BRANCH, SPEAK) SEE FIGURE 4

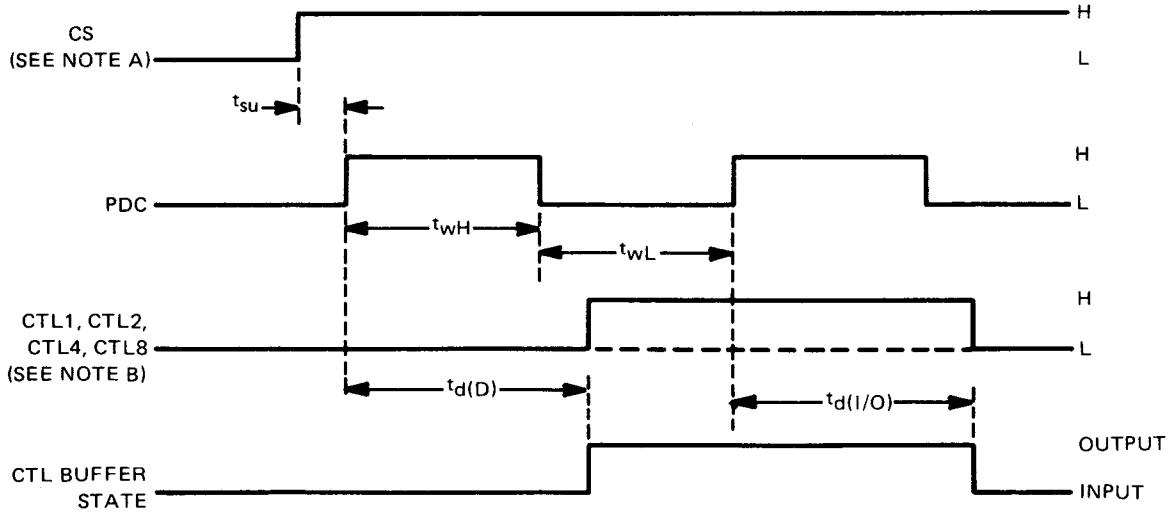
PARAMETER		MIN	MAX	UNIT
t_{su}	Data and CS setup time	0		μs
t_h	Data hold time	1.75		cycle‡
t_h	Data hold time, f_{osc} = 640 kHz*	10.9		μs
t_{wH}	Pulse width, PDC high	1		cycle‡
t_{wH}	Pulse width, PDC high, f_{osc} = 640 kHz	6.25		μs
t_{wL}	Pulse width, PDC low	1		cycle‡
t_{wL}	Pulse width, PDC low, f_{osc} = 640 kHz	6.25		μs

* The system clock is set by using the ROM clock (160 kHz).

4.6 SWITCHING CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE, V_{DD} = −9

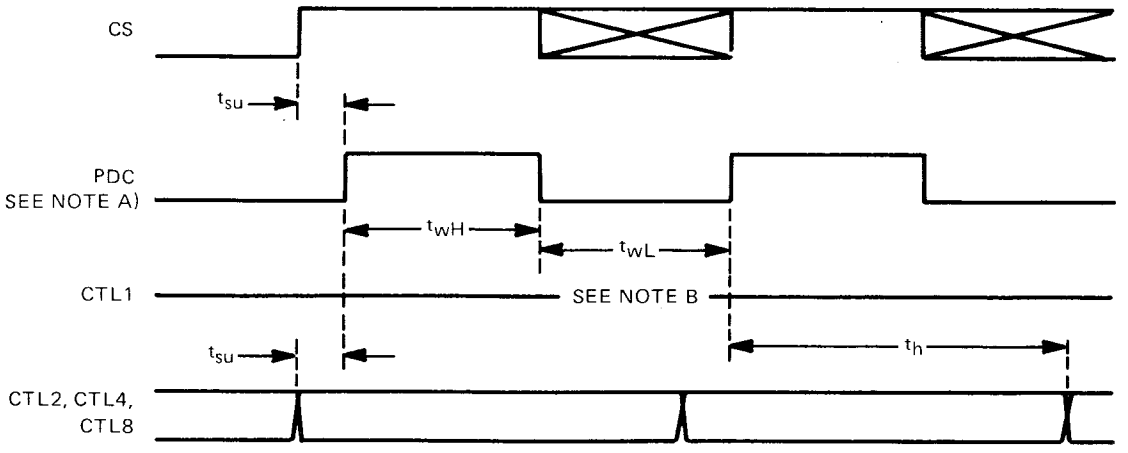
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{osc}	Oscillator frequency		608	640	674	kHz
$t_{d(D)}$	Data output time		1.25			cycle‡
$t_{d(D)}$	Data output time	f_{osc} = 640 kHz	7.8		8.1	μs
$t_{d(I/O)}$	Output buffer switching time		1.25			cycle‡
$t_{d(I/O)}$	Output buffer switching time	f_{osc} = 640 kHz	7.8		8.1	μs

† Typical values are at T_A = 25°C.
‡ Cycle refers to the equivalent time in CPU clock cycles.



NOTES: A. Output buffers are enabled only while CS is high. Turn-on and turn-off delays are equivalent to 0.75 instruction cycle.
B. For TEST TALK, only CTL1 is active.

FIGURE 3 – TIMING DIAGRAM, DATA OUTPUT AND I/O MODE SWITCHING

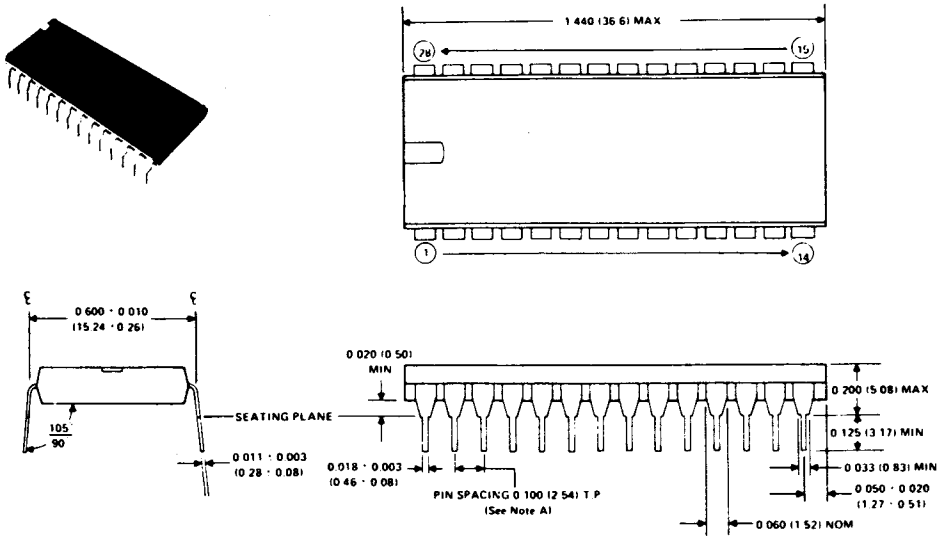


NOTES: A. Refer to command descriptions for PDC requirements.
B. CTL1 is irrelevant (don't care) for command transfer; same as CTL2, CTL4, CTL8 for address transfer.

FIGURE 4 – TIMING DIAGRAM, COMMAND AND DATA TRANSFER

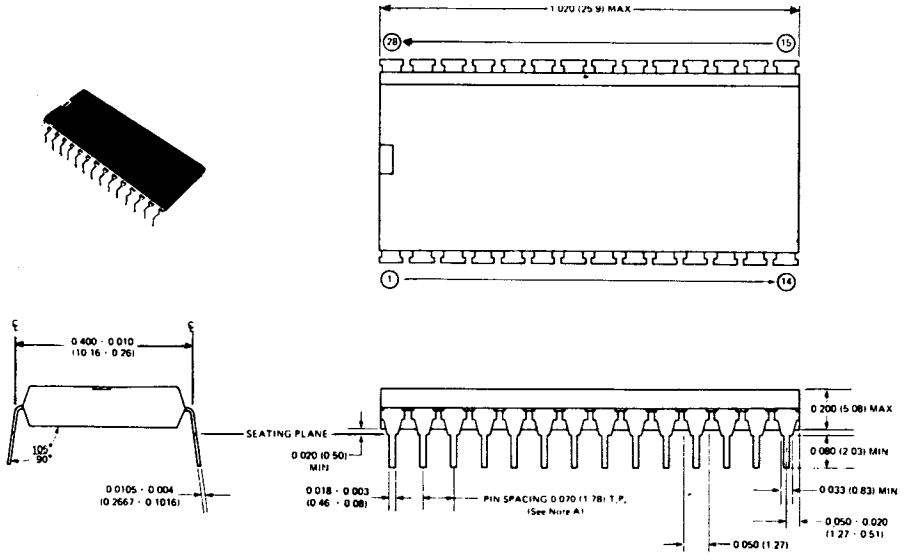
5. MECHANICAL DATA

5.1 TMS 5110A — 28-PIN PLASTIC PACKAGE, .100″ PIN CENTER SPACING, .600″ PIN ROW SPACING



NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

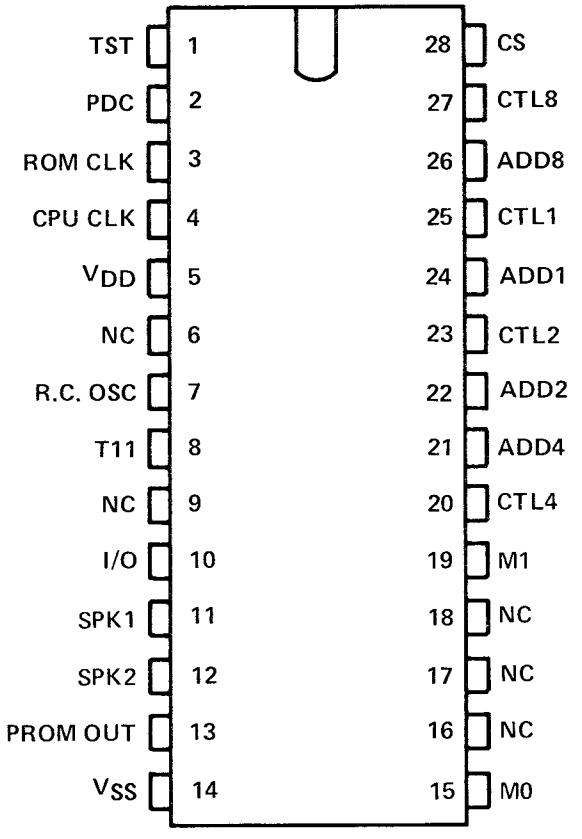
5.2 TMS 5110A — 28-PIN PLASTIC PACKAGE, .070″ PIN CENTER SPACING, .400″ PIN ROW SPACING



NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

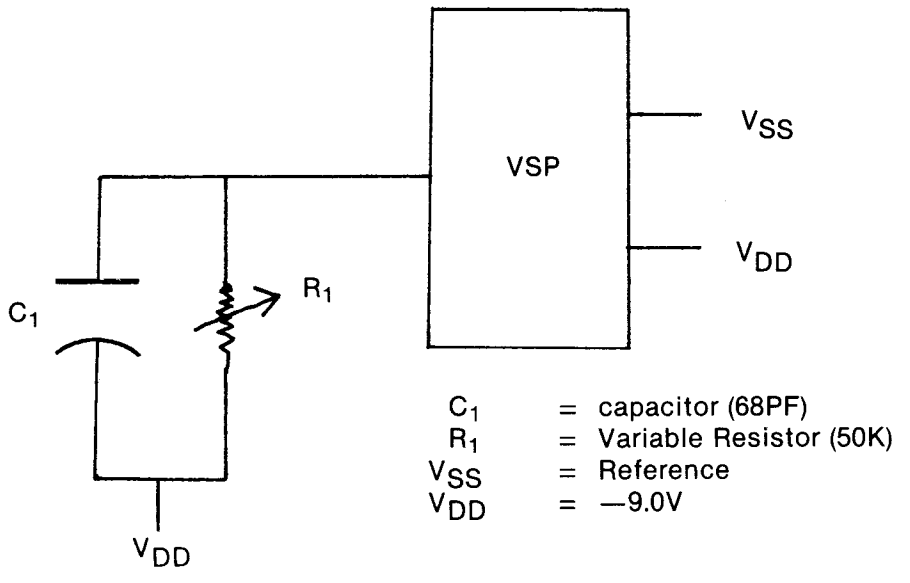
5.2 PIN ASSIGNMENTS AND FUNCTIONS

PIN	NAME	IN/OUT	FUNCTION
1	TST		For factory testing only
2	PDC	I	Processor data clock
3	ROM CLK	O	Clock to control TMS6100 ROM (160 kHz)
4	CPU CLK	O	Output clock for CPU (320 kHz)
5	V_{DD}	I	Drain supply voltage (–9V NOM)
6	NC	I	No connection
7	R.C. OSC.	I	RC option pin (640 kHz)
8	T11		Sync for serial data out
9	NC	–	No connection
10	I/O	O	Serial data out
11	SPK1	O	Analog speech out
12	SPK2	O	Analog speech out
13	PROM OUT		Test
14	V_{SS}	I	Substrate supply voltage (0 V NOM)
15	M0	O	Transfer data to VSP control
16	NC	–	No connection
17	NC	–	No connection
18	NC	–	No connection
19	M1	O	Load address to VSM control
20	CTL4	I/O	Control/read data bus
21	ADD4	O	Address to VSM
22	ADD2	O	Address to VSM
23	CTL2	I/O	Control/read data bus
24	ADD1	O	Address to VSM (LSB)
25	CTL1	I/O	Control/read data bus (LSB)
26	ADD8	I/O	Address to VSM/data to VSP (MSB)
27	CTL8	I/O	Control/read data bus (MSB)
28	CS	I	Chip select


TST 1
PDC 2
ROM CLK 3
CPU CLK 4
VDD 5
NC 6
R.C. OSC 7
T11 8
NC 9
I/O 10
SPK1 11
SPK2 12
PROM OUT 13
VSS 14
28 CS
27 CTL8
26 ADD8
25 CTL1
24 ADD1
23 CTL2
22 ADD2
21 ADD4
20 CTL4
19 M1
18 NC
17 NC
16 NC
15 M0

APPENDIX

SYSTEM CLOCKS*



- The system clock is set by using the ROM CLK (160 kHz)

Figure A-1 TMS5110A Oscillator

TABLE A-1 – A COMPARISON OF SYSTEM TIMES

SAMPLE RATE:	10 kHz	8 kHz
FRAME RATE	50 Hz	40 Hz
FRAME PERIOD	20 ms	25 ms
INTERPOLATION RATE	400 Hz	320 Hz
INTERPOLATION INTERVAL	2.5 ms	3.125 ms
SAMPLE RATE	10 kHz	8 kHz
SAMPLE PERIOD	100 μs	125 μs
ROM CLOCK RATE	200 kHz	160 kHz
ROM CLOCK PERIOD	5 μs	6.25 μs
RC OSC RATE	800 kHz	640 kHz
RC OSC PERIOD	1250 ns	1562.5 ns

NOTE: All timing references in this data manual are based on an 8-kHz sample rate.