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TEXAS INSTRUMENTS

TM 990

TM 990/307 Communication Expander

Data Manual

MICROPROCESSOR SERIES™

January 1980

IMPORTANT NOTICE

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

Information contained herein supersedes previously published data on these devices from TI.

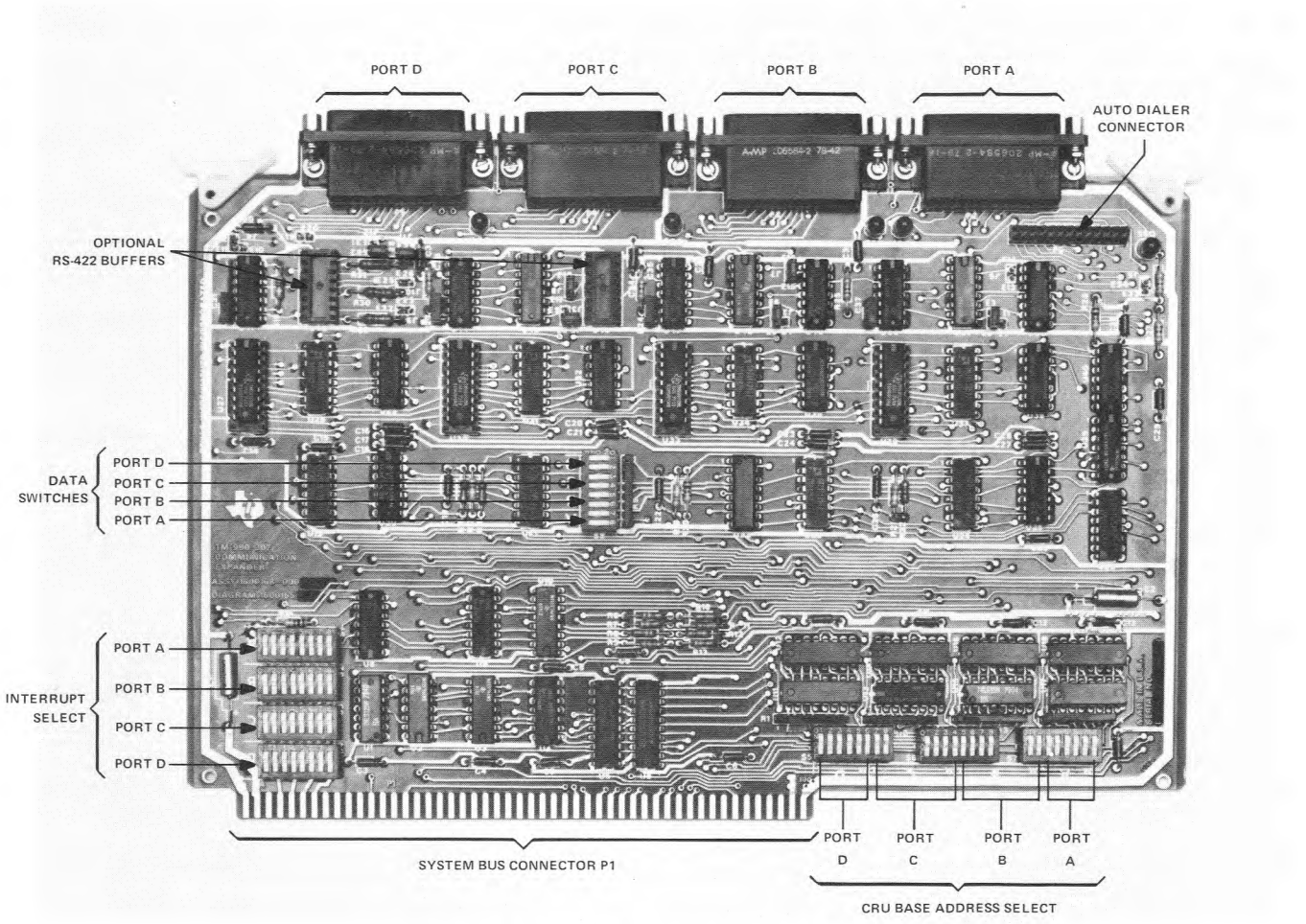

FIGURE 1 – TM 990/307 PRINCIPAL COMPONENTS

TM990/307 COMMUNICATION EXPANDER

TM990/307 Communication Expander Module, shown in Figure 1, is a bus compatible member of the TM990 product family. Figure 2 is a block diagram of the module. This module can communicate with up to four asynchronous or synchronous devices through RS232 interfaces (an optional TMS9903 is required for synchronous devices). The devices can be either modems or terminals. A parallel interface is included for interfacing to an autodialer such as Bell 801 Automatic Calling Unit.

FEATURES

- Four RS-232C EIA ports using DB-25P connectors (Port D provides both RS 232C and RS 422 interfaces).
- Bell automatic calling unit interface
- Individual channels are CRU address selectable
- CRU addressable DIP switches and status LED's provided
- Compatible with TM990/101 Port B software
- Loopback allows self testing
- Software programmable baud rates.

ADVANCE INFORMATION
This document contains information on a new product. Specifications are subject to change without notice.

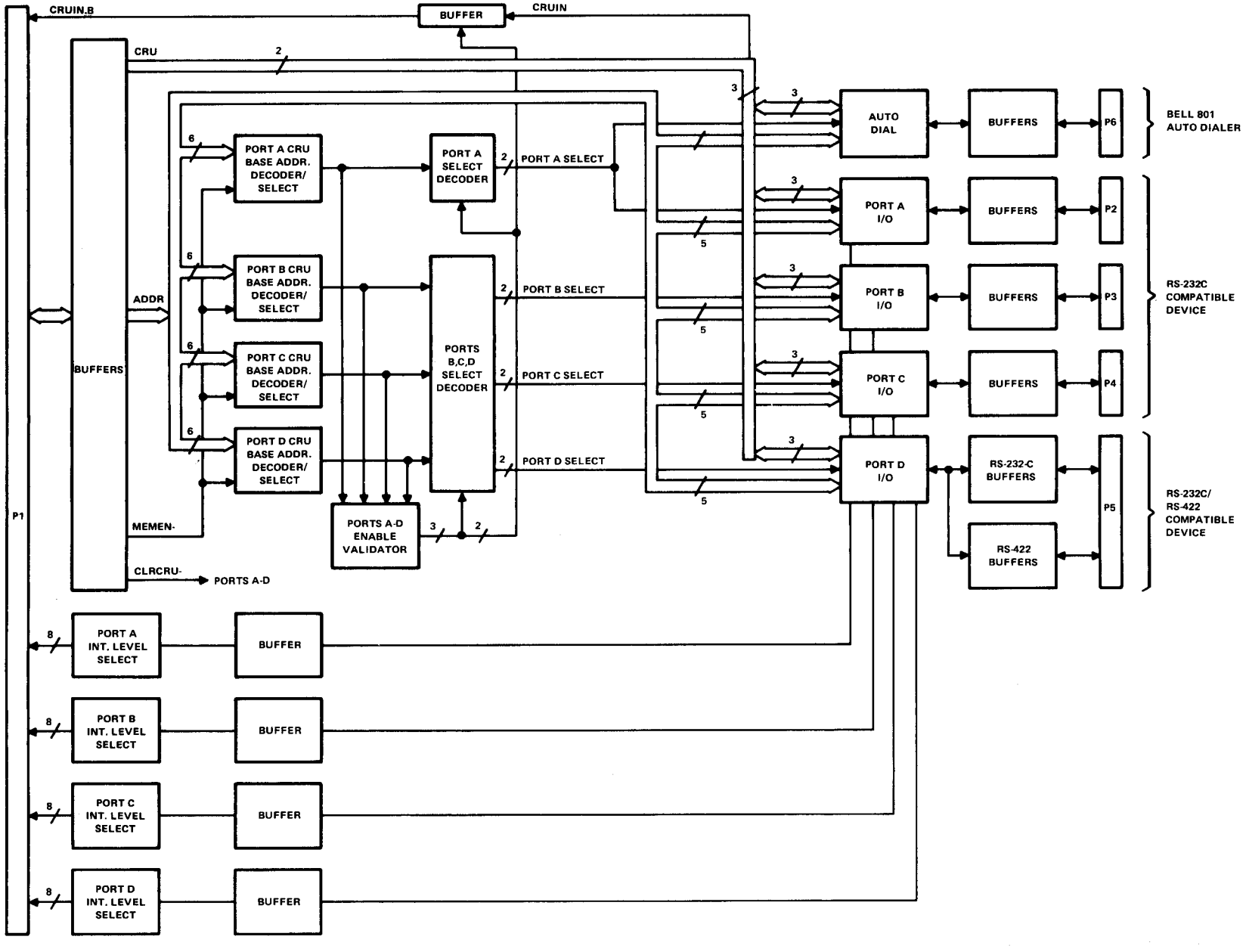

FIGURE 2 – TM 990/307 BLOCK DIAGRAM

OPERATION

The TM990/307 Communication Expander Module is implemented using the TM990 printed circuit format. The TM990/307 uses four TMS9902 asyncronous communication CONTROLLER devices for transmitting and receiving serial data. Each TMS9902 also contains an interval timer giving the user four programmable timers. By replacing the TMS9902's with TMS9903's communication to synchronous modems is possible.

ADDRESSING

Each EIA data port occupies 64 bits in the CRU map. Ports B, C, and D use identical CRU maps. The first thirty two bits are used to address the 9902 communication controller. The next 32 bits are used for modem control, CRU addressable switches, status monitoring and LED. Port A has the Auto Dialer feature in addition.

SPECIFICATIONS

Input/Output

Data Ports

TMS9902 asynchronous controller

Programmable data rate, stop bits, parity

Break characters generation

Framing, parity, and overrun errors detected

75 to 38400 baud, software programmable

EIA RS-232 signal compatible

Switch selectable CRU address, each port independent

Two CRU addressable switches per port

One CRU addressable LED per port

Auto Dialer (Port A Only)

Header connector with pinouts compatible with a BELL 801 auto dialer or equivalent. Pinouts are arranged such that an interface cable can be constructed using: 25/26-pin ribbon cable, a 26-pin header connector and a 25-pin DB-25 EIA connector.

RS-422 Port (Port D Only)

Port D can be jumper configured as an RS-422 Port.

Interval Timers

Four timers with a resolution of 64 microseconds and a maximum interval of 16.32 milliseconds.

Interrupts

Each port is capable of generating an interrupt from the data port or the interval timer. These interrupts can be jumpered to system interrupts 8 through 15.

I/O Connectors

Data ports
DB-25
25-pin EIA connector

Auto dialer
26-pin dual row header

Power Requirements

5 V ± 3% @ 1 A

+12 V ± 3% @ 0.2 A

−12 V ± 3% @ 0.2 A

Temperature Range

Operating:	0°C to 70°C
Storage:	−40°C to 100°C

Physical Characteristics

Width:	11 inches (280 mm)
Height:	7.5 inches (191 mm)
Board thickness:	0.062 inches (1,58 mm)

Interrupts: Jumper selectable-levels 8 through 15

OPTIONAL ACCESSORIES

The four ports are compatible with the following EIA RS-232C cables; 502 (RS-232 EIA terminal), 503 (743/745), 505 (733 ASR), and the 506 RS-232 modem cable. The user may construct his own cable to interface to the 801 auto-dialer or when using RS-422 on port D with standard ribbon cable components.

Demonstration Software

TM990/427 demonstration software package allows the user to verify the operation of the communication expansion module. The module is put in the loopback mode and tested under different baud rate settings. If the board passes the test the LED is extinguished. The demonstration software accepts input from the CPU EIA port and transmits it to any of the four expansion ports.

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SECTION 1

INTRODUCTION

1.1 GENERAL

The TM 990/307 is a four channel communication expander module (See Figure 1-1). This module can communicate with up to four asynchronous or synchronous devices through RS-232C interfaces (a TMS 9903 is required for synchronous devices). The devices can be either terminals or modems. A parallel interface is included for interfacing to an auto-dialer such as the Bell 801 Automatic Calling Unit. The TM 990/307 interfaces with either the TM 990/100 or TM 990/101 CPU Modules via the TM 990 system bus. Other features include:

- Four RS-232C EIA ports using DB-25P connectors (Port D provides both RS-232C and RS-422 interfaces).
- Bell Automatic Calling Unit interface
- Individual channels are CRU address selectable
- Individual channels can be assigned to interrupt levels 8-15
- CRU addressable DIP switches and LEDs
- Compatible with TM 990/101 Port B software
- Loopback allows automatic testing.

1.2 MANUAL ORGANIZATION

This manual is organized as follows:

- Section 1 covers module characteristics and specifications
- Section 2 shows how to install, power-up, and operate the TM 990/307
- Section 3 covers the programming aspects of the module
- Section 4 covers the theory of operation with circuit descriptions keyed to schematic diagrams.

1.3 GENERAL SPECIFICATIONS

- Power Requirements:

VOLTAGE	REGULATION	CURRENT	
		TYP	MAX
+5V	±3%	0.75A	1.60A
+12V	±3%	0.09A	0.36A
-12V	±3%	0.08A	0.30A

- Operating Temperature: 0°C to 65°C.

- Module Dimensions: See Figure 1-2.

1.4 TM 990/307 MODULE APPLICATIONS

Figure 1-3 shows a system that uses the TM 990/307 Communication Expander Module. This system allows communications between a TM 990/100 or TM 990/101 CPU Module and two modems, two terminals, and a Bell 801 Automatic Calling Unit (ACU). The modems allow telephone lines to be used as a communications link: this feature provides for long range communications. The CPU module can access the ACU via the auto dialer interface that is provided on the TM 990/307. The auto dialer, when selected by the CPU module, places the call that was requested.

1.5 APPLICABLE DOCUMENTS

The following is a list of documents that provide supplementary information for the TM 990/307 user.

- TMS 9902 Asynchronous Communications Controller Data Manual
- TMS 9903 Synchronous Communications Controller Data Manual
- The TTL Data Book
- Data Auxiliary Set 801C (Automatic Calling Unit) Interface Specification (American Telephone & Telegraph Company)
- Data Auxiliary Sets 801C3 and 801C4 for Automatic Calling - Theory of operation and Supplementary Information (American Telephone & Telegraph Company).

1.6 TM 990/307 BLOCK DIAGRAM

The block diagram for the TM 990/307 is given in Figure 1-4.

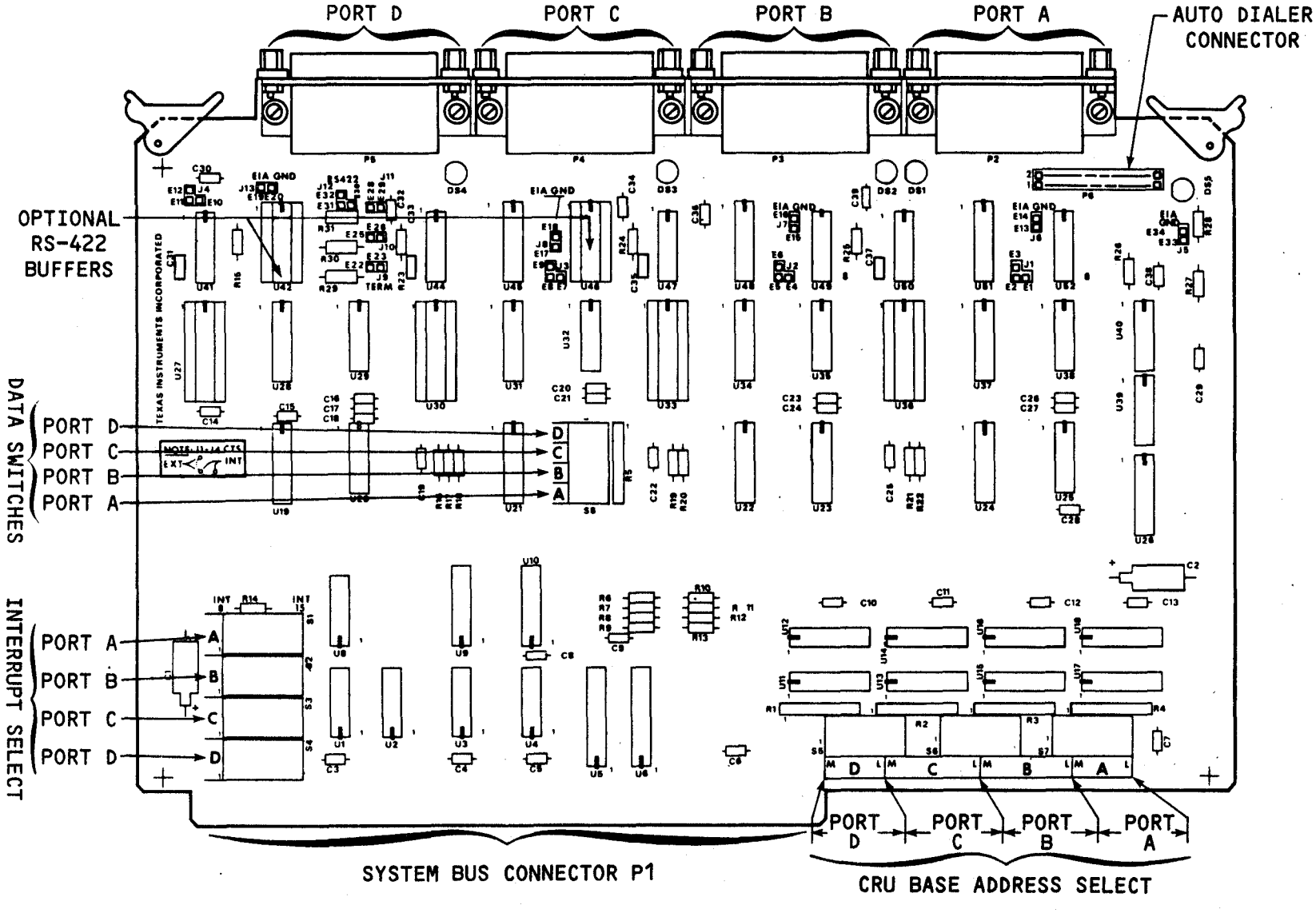


FIGURE 1-1. TM 990/307 PRINCIPAL COMPONENTS

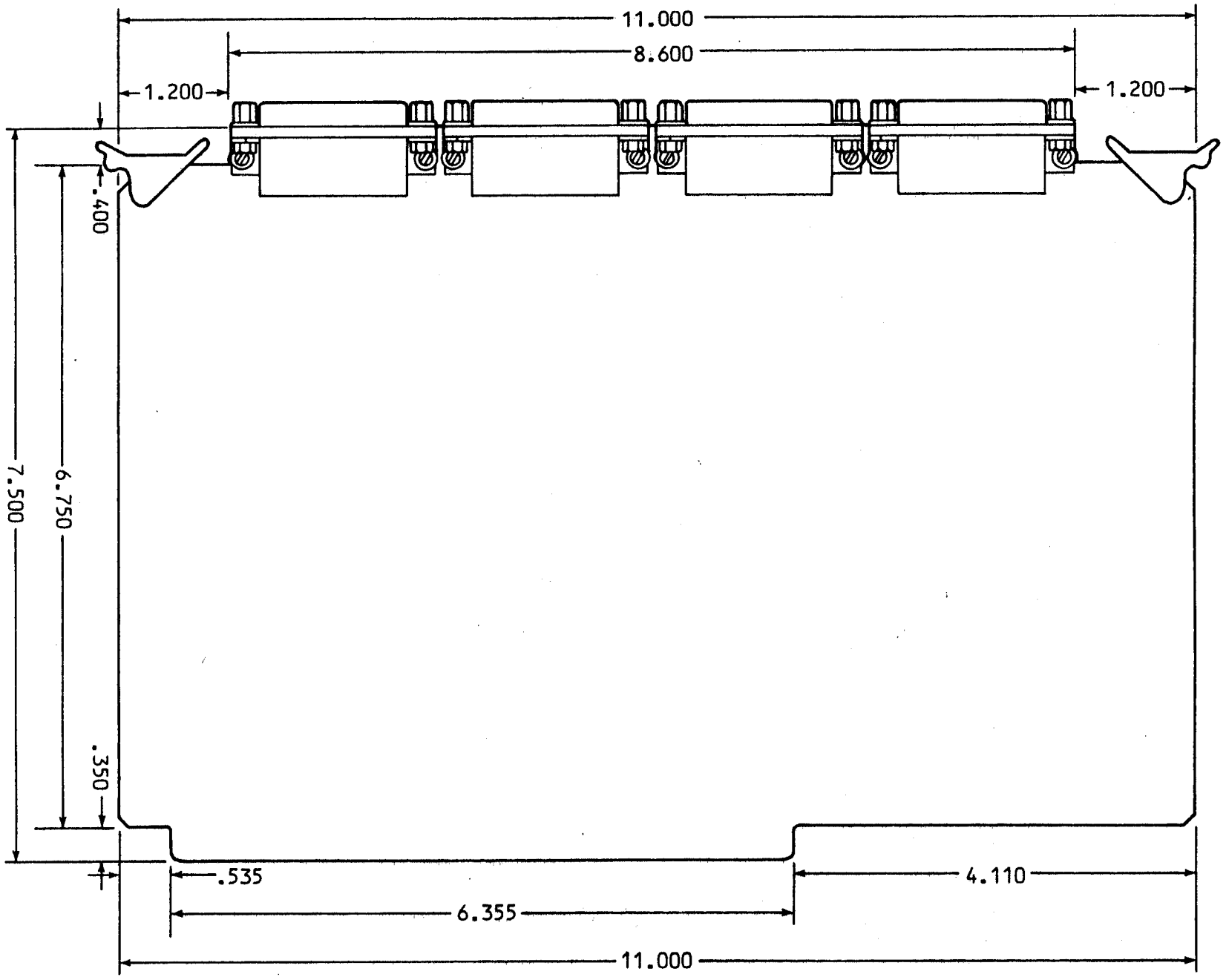


FIGURE 1-2. TM 990/307 DIMENSIONS (IN INCHES)

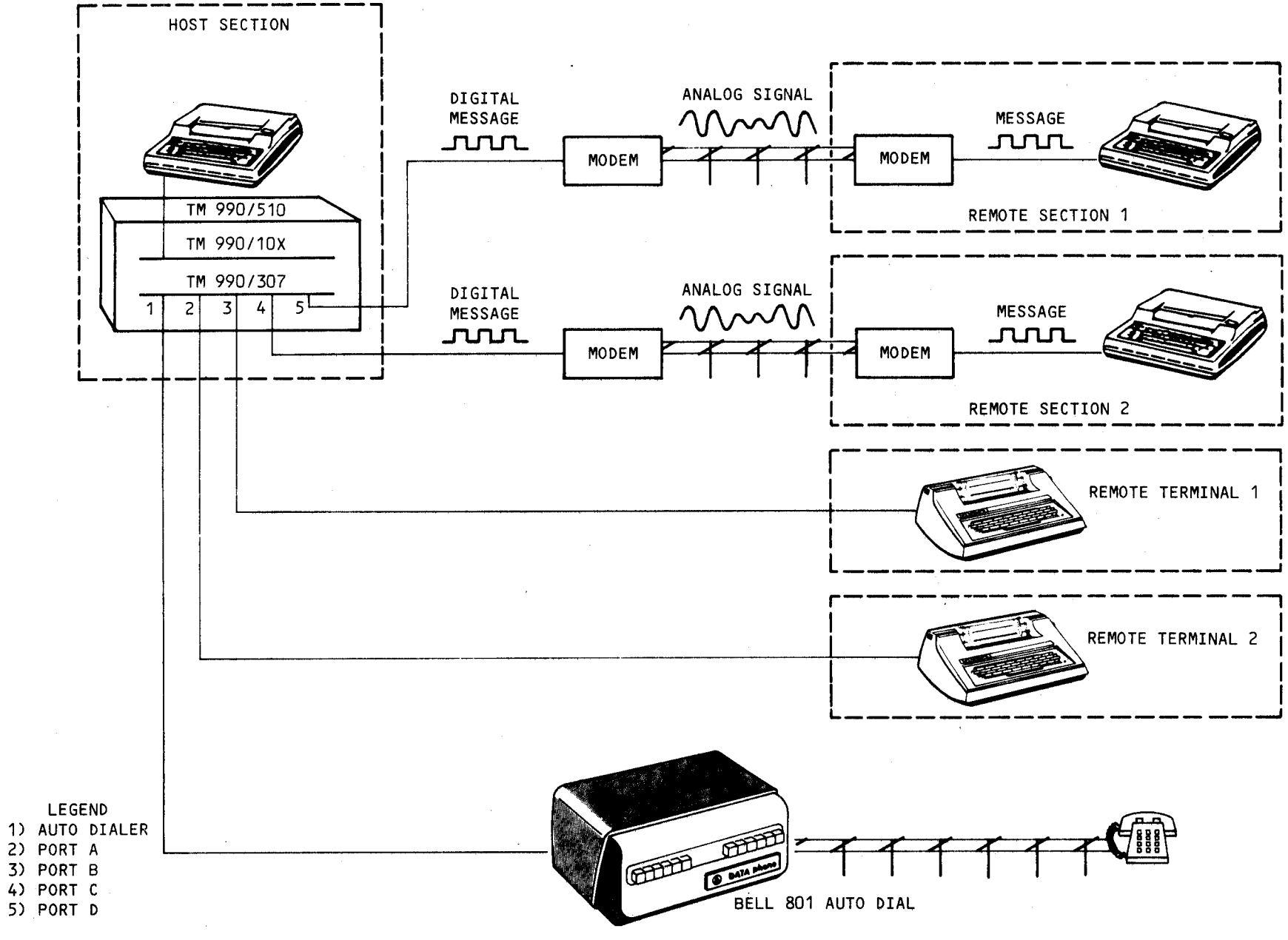


FIGURE 1-3. TM 990/307 COMMUNICATION EXPANDER MODULE APPLICATION

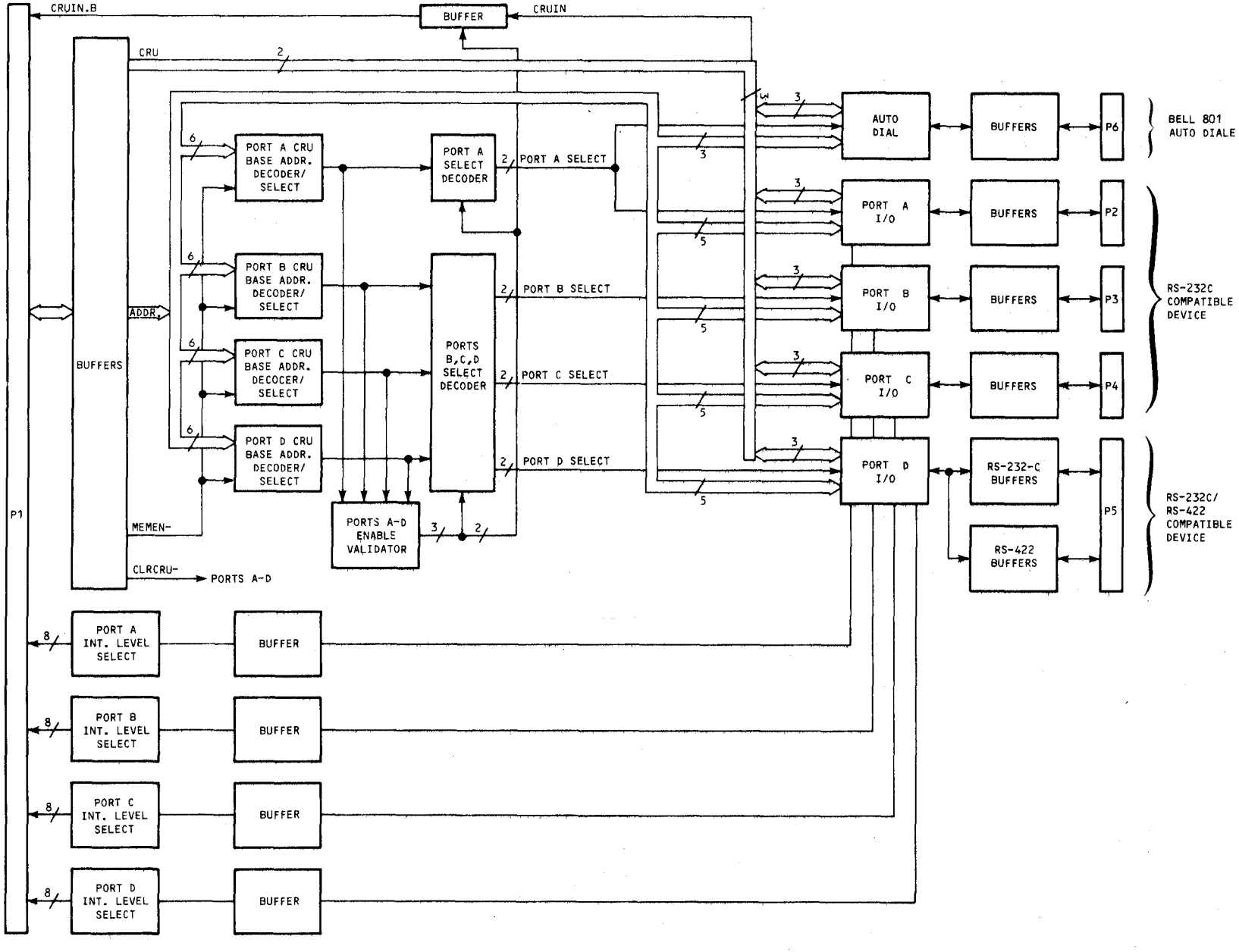


FIGURE 1-4. TM 990/307 BLOCK DIAGRAM

SECTION 2

INSTALLATION AND OPERATION

2.1 GENERAL

This section covers unpacking and inspection, jumper and switch settings, required equipment, and a test routine that can be used to checkout the module.

2.2 UNPACKING AND INSPECTION

Remove the TM 990/307 from its carton and discard any protective wrapping. Inspect the module for any damage that could have occurred in shipping. Report any damage to your supplier.

2.3 JUMPER/SWITCH DESCRIPTIONS

Jumpers and switches are used to provide the following functions:

1) Terminal/modem select (paragraph 2.3.1)

2) CRU base address select for ports A to D (2.3.2)

3) Interrupt level select for ports A to D (2.3.3)

4) Two-bit data decoder switch for each port (2.3.4)

5) Port D only: RS-232-C/RS-422 selection (2.3.5)

6) Protective ground (2.3.6)

These jumper/switch selectable functions are described in the following paragraphs.

2.3.1 Terminal/Modem Select

The TM 990/307 can be used with either an RS-232-C terminal or a modem. Table 2-1 shows the jumper postions that are required to select the desired function for the individual ports.

TABLE 2-1. TERMINAL/MODEM SELECT JUMPERS

Port	Jumper Connection	
	Modem Select	Terminal Select
A (P2)	E2 to E3	E2 to E1
B (P3)	E5 to E6	E5 to E4
C (P4)	E8 to E9	E8 to E7
D (P5)	E11 to E12	E11 to E10

2.3.2 CRU Base Address Select (Switches S5, S6, S7)

Each port can be assigned a unique CRU base address that is the beginning of a 64-bit CRU address area, Section 3 of this manual covers programming these CRU areas, and Tables 3-1 and 3-2 identify the bits in each of these 64-bit areas.

The CRU base address for each port is selected by the settng of switches S5, S6, and S7 as listed in Table 2-2. These 8-position switches are divided into four groups of six switches that are used to select I/O ports A to D. Figure 2-1 shows the switch position assignments for these switches. Each EIA port can be placed on any 64-bit boundry within the 4096-bit CRU space. Each EIA port occupies 64 bits in the CRU map. Note the address lines (A3 to A8) that are compared to the switch settings as shown in Table 2-2. Address lines A9 to A14 define which of the 64 bits is selected.

CAUTION

1. The ports should not be assigned CRU hardware base addresses below 100_{16} (software base adress 200_{16} or R12 contents) when using TM 990/100 or TM 990/101 CPU modules as this can interfere with dedicated CRU devices on these boards.
2. Do <u>not</u> assign the same CRU base address to more than one port. Ports assigned the same CRU base address will not operate.

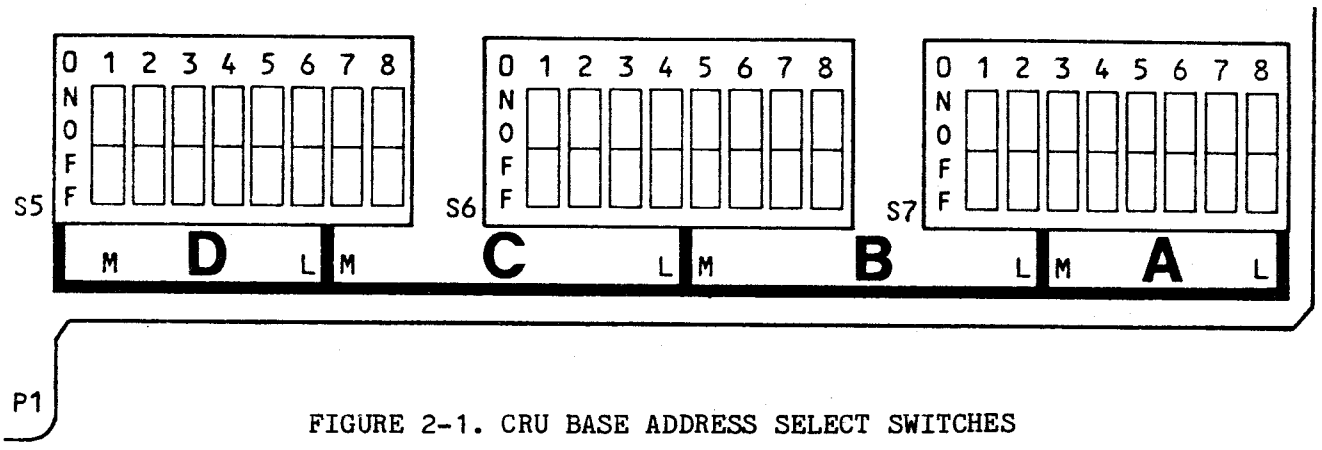


FIGURE 2-1. CRU BASE ADDRESS SELECT SWITCHES

TABLE 2-2. CRU BASE ADDRESS SELECT SWITCHES

Port	Switch Positions MSB A3	A4	A5	A6	A7	LSB A8	CRU Base Address (Dec)	Hardware Base Addr (Hex)	Software Base Addr (Hex)
A	S7-3	S7-4	S7-5	S7-6	S7-7	S7-8			
B	S6-5	S6-6	S6-7	S6-8	S7-1	S7-2			
C	S5-7	S5-8	S6-1	S6-2	S6-3	S6-4			
D	S5-1	S5-2	S5-3	S5-4	S5-5	S5-6			
	0	0	0	0	0	0	0	0000	0000
	0	0	0	0	0	1	64	0040	0080
	0	0	0	0	1	0	128	0080	0100
	0	0	0	0	1	1	192	00C0	0180
	0	0	0	1	0	0	256	0100	0200
	0	0	0	1	0	1	320	0140	0280
	0	0	0	1	1	0	384	0180	0300
			.						
			.						
			.						
	1	1	1	1	1	1	4032	0FC0	1F80

Note: 1 = ON; 0 = OFF

The following procedure can be used to determine the switch positions for selecting a CRU hardware base address that is not given in Table 2-2.

1) Convert the CRU hardware base address into its binary equivalents.
2) Strip off the first four bits; the CRU hardware base address is a 12-bit value using only the 12 LSBs applied to address lines A3 to A14; since only address lines A3 to A8 are compared on the board, use the first six bits of these remaining 12 bits.
3) Convert the first six bits of the remaining 12 bits (obtained in step 2) into ON/OFF equivalents to determine the switch settings. The following definitions apply: 1 = ON, 0 = OFF.

Example: Determine the switch settings required to select CRU hardware base address 0140_{16} for port A (NOTE: never use the same address for more than one port; otherwise, port access will be prevented).

		Comments
1)	0 1 4 0	Hardware Base Address (Hex)
	0000 0001 0100 0000	Binary equivalent of Hardware Base Address
2)	0001 01	Strip off first 4 bits; use next six bits which are compared to address lines A3 to A8

3)

	A3	A4	A5	A6	A7	A8
	0	0	0	1	0	1
	↓	↓	↓	↓	↓	↓
	OFF	OFF	OFF	ON	OFF	ON
Port A Settings =	S7-3	-4	-5	-6	-7	-8

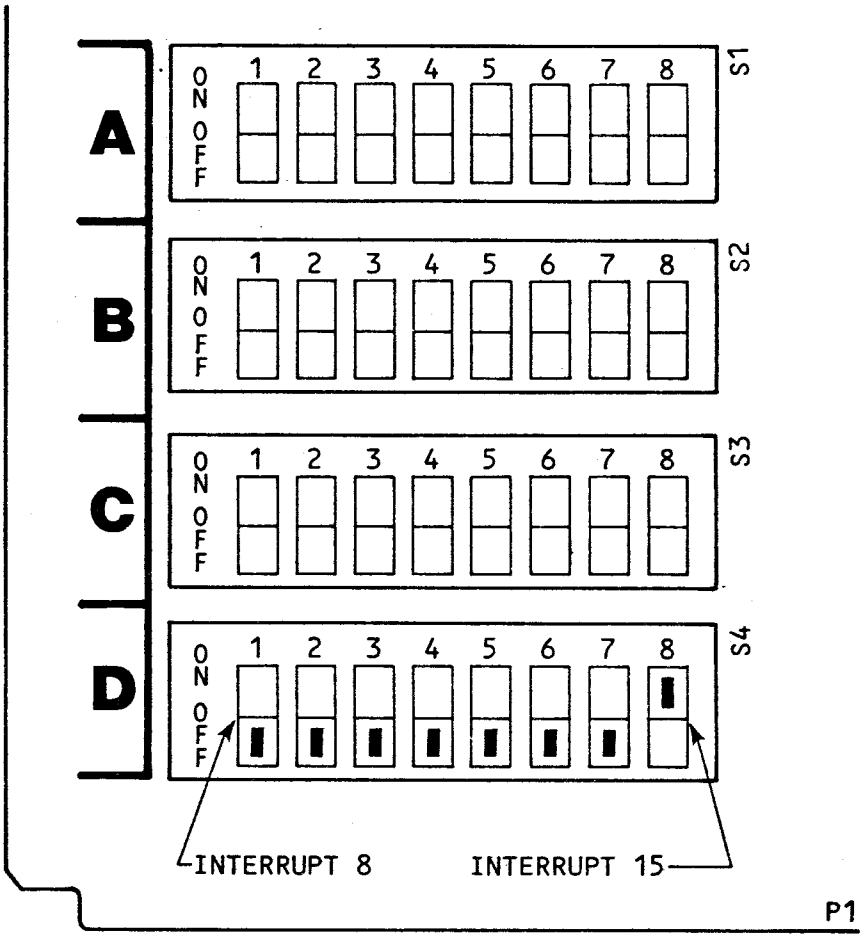
2.3.3 Interrupt Level Select (Switches S1, S2, S3, S4)

Each TMS 9902 (or TMS 9903) issues an interrupt under certain circumstances. These circumstances and interrupt operation are explained in section 3.3.8. as well as in the respective TMS 9902 or TMS 9903 data manuals.

The interrupt level to the host (INT8- through INT15-) is selected by setting the specific ports's interrupt select switch to the ON position for the desired interrupt level. All in the OFF position means no interrupt will be sent to the host. S1 is used for Port A, S2 for Port B, S3 for Port C, and S4 for Port D. Figure 2-2 shows the respective settings for these ports.

2.3.4 Two-Bit Decoder Switch (Switch S8)

Each port provides switch selection of two data bits that can be read via the CRU in order to monitor constants such as desired parameters or station ID numbers during program execution. These switches can also be used as an aid in testing and evaluating the performance of the TM 990/307. S8-1 and S8-2 are within the Port A CRU map, S8-3 and S8-4 with Port B, S8-5 and S8-6 with Port C, and S8-7 and S8-8 with Port D. Figure 2-3 shows the data level select circuitry for Port A. S8-1 and S8-2 can provide either a logic one or a logic zero as data inputs (D5 and D4) for 74LS251 data selector/multiplexer U37. Address lines A12-A14 are used to select the desired data input. A switch in the ON postion corresponds to a logic one, and a switch in the OFF postion corresponds to a logic zero.



NOTE: Darken position indicates switch setting.

FIGURE 2-2. INTERRUPT LEVEL SELECTION

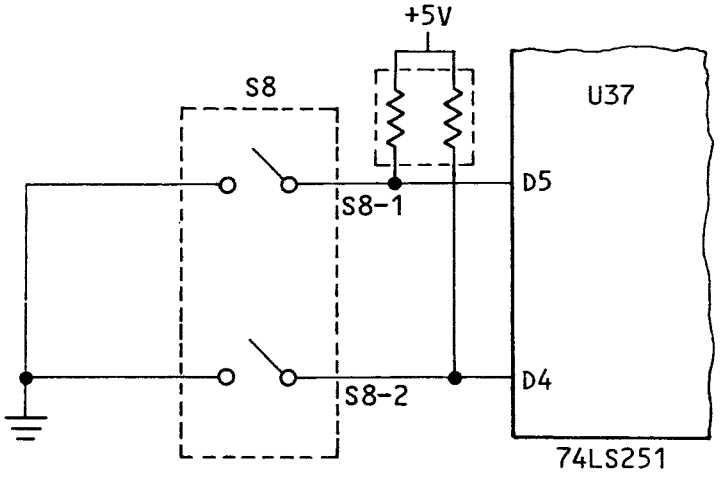


FIGURE 2-3. DATA LEVEL SELECT

2.3.5 Port D: RS-232/RS-422 Selection

Port D can be used with either RS-232-C or RS-422 compatible devices. However, if a TMS 9903 (synchronous I/O controller) is used, then only RS-422 devices can be used. Table 2-3 shows the connections required so that one or the other type can be used.

TABLE 2-3. RS-232-C/RS-422 SELECTION

Function	Jumper Postions
RS-232-C Compatible Device	E31 to E30
RS-422 Compatible Device	E31 to E32

Line termination jumpers are provided in the RS-422 interface circuitry. If it is desired to terminate the RS-422 lines, connect jumpers from E28 to E29, E25 to E26, and E22 to E23.

2.3.6 Signal/Protective Ground

A jumper is provided with each RS-232-C interface that allows tying signal and protective grounds together. The use of the signal ground (common return) is mandatory; however, the use of the protective ground depends on local electrical codes and is optional. If protective grounds are required, connect jumpers as shown in Table 2-4. A protective grounding wire should also be connected from signal ground to the point of electrical ground. A convenient place to connect this wire would be on the terminal block on the back of the card cage TB1/TB10 (signal ground points). The size and color of the protective grounding wire should conform to the applicable underwriter's regulation.

TABLE 2-4. PROTECTIVE GROUNDS

Function	Jumper Postions
Protective Ground for Port A	E14 to E13
Protective Ground for Port B	E16 to E15
Protective Ground for Port C	E18 to E17
Protective Ground for Port D	E20 to E19
Protective Ground for Auto dialer	E33 to E34

2.3.7 Jumper Survey

Thirteen jumpers are used to select the jumper-selectable functions just described. Table 2-5 lists these jumpers, a brief description of each, and the section in the manual where additional material can be found. It is recommended that the user read the detailed information on these jumpers before making a jumper setting.

TABLE 2-5. JUMPER SUMMARY

Jumper	Setting	Description	Section
J1	E2-E1	Port A Terminal select	2.3.1
J1	E2-E3	Port A modem select	2.3.1
J2	E5-E4	Port B Terminal select	2.3.1
J2	E5-E6	Port B modem select	2.3.1
J3	E8-E7	Port C Terminal select	2.3.1
J3	E8-E9	Port C modem select	2.3.1
J4	E11-E10	Port D Terminal select	2.3.1
J4	E11-E12	Port D modem select	2.3.1
J5	E33-E34	Auto dialer protective ground	2.3.6
J6	E13-E14	Port A protective ground	2.3.6
J7	E15-E16	Port B protective ground	2.3.6
J8	E17-E18	Port C protective ground	2.3.6
J9	E22-E23	RS-422 line termination	2.3.5
J10	E25-E26	RS-422 line termination	2.3.5
J11	E28-E29	RS-422 line termination	2.3.5
J12	E31-E30	RS-232 compatible device	2.3.5
J12	E31-E32	RS-422 compatible device	2.3.5
J13	E19-E20	Port D protective ground	2.3.6

2.4 REQUIRED EQUIPMENT FOR CHECKOUT

A minimal system for using the TM 990/307 requires the following:

1) TM 990/307 Communication Expander Module
2) TM 990/100 or TM 990/101 CPU module
3) TM 990/502 Cable Assembly for each RS-232-C terminal
4) TM 990/510 card cage or equivalent
5) TM 990/518A power supply or equivalent
6) RS-232-C terminal
7) Optional Bell 801 automatic calling unit.

Figure 2-4 shows a system that can be used for evaluation purposes. The setup procedure that follows assumes that the following items will be used: 1) TM 990/10X CPU module, 2) TM 990/307 Communication Expander Module (Port A), 3) TM 990/502 cable assemblies (two), 4) TM 990/510 card cage, 5) TM 990/518A dc power supply, and 6) two RS-232-C terminals.

2.4.1 Power Supply and Card Cage

Install the TM 990/10X CPU module into slot 1 of the card cage. Any other available slot may be used for the TM 990/307. Figure 2-4 shows the connections between the power supply and card cage.

2.4.2 Terminals and Cable Assemblies

TM 990/502 cable assemblies can be used as the connecting link between the terminals and the two modules. Connect one cable from terminal 1 to P2 of the CPU module. Connect the other cable assembly to P2 of the TM 990/307 to interface with Port A.

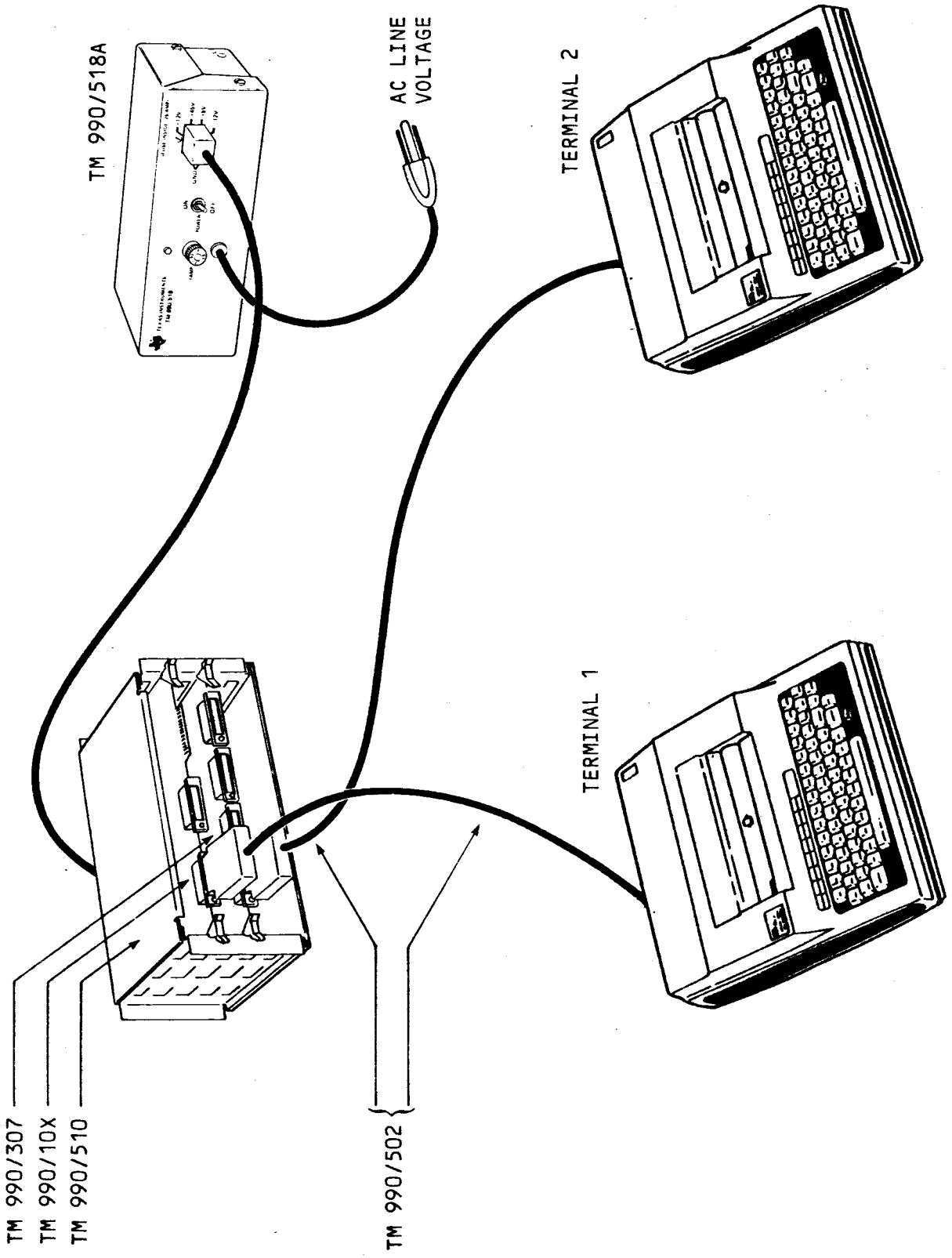


FIGURE 2-4. TM 990/307 SAMPLE SYSTEM

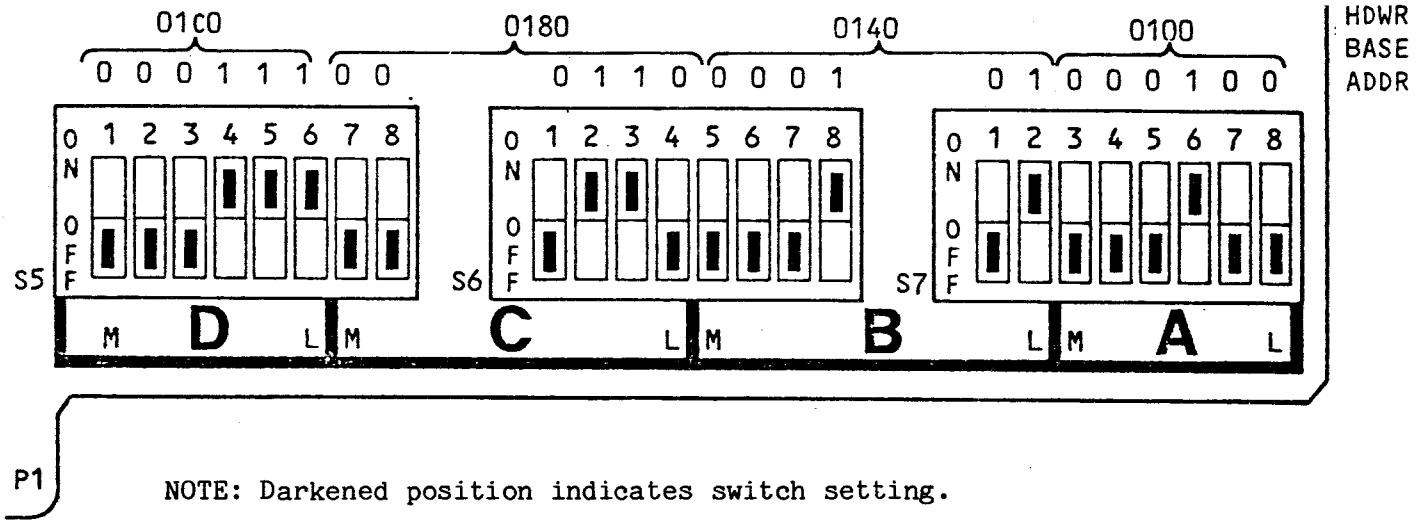
2.4.1.3 TM 990/307 Jumper/Switch Settings

The following functions must be selected by jumper positions and switch settings on the TM 990/307:

1) Terminal/modem select (Section 2.3.1)
2) CRU base address select (Section 2.3.2)
3) Interrupt level select (Section 2.3.3)
4) Data level select (Section 2.3.4).

2.5 TEST ROUTINES

After the system has been configured, the following short programs can be used to check system operation. Switches S5, S6, and S7 must be set as shown below so that Ports A to D are contiguously placed 64 CRU bits apart beginning with Port A located at CRU hardware base address 0100_{16} (CRU software base address 0200_{16}). These addresses will be used in the example programs throughout this manual.



NOTE: Darkened position indicates switch setting.

Use the TIBUG memory inspect/change command (M) to load the program object code at the memory addresses shown. The programs can be executed using the E command with $FE00_{16}$ in the Program Counter.

2.5.1. Blink All Five LEDs

The program in Figure 2-5 will cause all the LEDs on the board to blink. Note that this program uses the RSET (reset) instruction which resets the system and lights the LEDs.

```
Memory Object
 Addr   Code
 FE00 02E0          LWPI >FE20          SET WORKSPACE POINTER
 FE02 FE20
 FE04 020C          LI   R12,>0300      INITIALIZE CRU SFTWR BASE ADDR
 FE06 0300
 FE08 1DBF  LOOP    SBO  -65            EXTINGUISH AUTOCALL LED
 FE0A 1DAC          SBO  -84            EXTINGUISH PORT A LED
 FE0C 1DEC          SBO  -20            EXTINGUISH PORT B LED
 FE0E 1D24          SBO  +36            EXTINGUISH PORT C LED
 FE10 1D64          SBO  +100           EXTINGUISH PORT D LED
 FE12 0600          DEC  R0             DECREMENT COUNTER
 FE14 16FE          JNE  $-2
 FE16 0360          RSET                TURN ON LIGHTS
 FE18 0600          DEC  R0             DECREMENT COUNTER
 FE1A 16FE          JNE  $-2
 FE1C 10F5          JMP  LOOP           REPEAT
```

Execute by entering $FE00_{16}$ in the Program Counter and issuing the E command.

FIGURE 2-5. CODE TO BLINK LEDS

2.5.2 Write Character, Verify Character Sent

The program in Figure 2-6 writes a character out to each port and then reads the character back from the same port. If the operation is successful, the port LED goes off. If operation is not successful, the port LED will be lit. The autocall LED blinks after program execution. (Removing a TMS 9902 at a port will cause unsuccessful operation.)

The following jumper settings must be made:

- J1: E1-E2 CTS- to RTS- loop
- J2: E4-E5 CTS- to RTS- loop
- J3: E7-E8 CTS- to RTS- loop
- J4: E10-E11 CTS- to RTS- loop
- J12: E31-E32 RS-232 (TMS 9902)

```
Memory Object
 Addr   Code

       0200  CRUBAS  EQU   >0200              ADDRESS OF FIRST PORT
       026E  LED     EQU   CRUBAS+>6E         AUTO DIAL LED
       0080  SIZE    EQU   >0080              SIZE OF PORT ADDRESS SPACE
       0400  END     EQU   4*SIZE+CRUBAS      END OF 307 ADDRESS SPACE
       001A  BAUD    EQU   >001A              TEST BAUD RATE
             *
             *
 FE00  02E0  TEST    LWPI  >FE50              LOAD WORKSPACE POINTER
 FE02  FE50
 FE04  020C          LI    R12,CRUBAS         R12 POINTS TO LOW PORT
 FE06  0200
 FE08  1D1F  TEST1   SBO   31                 RESET 9902
 FE0A  0201          LI    R1,>6200           SET CONTROL BITS
 FE0C  6200
 FE0E  3201          LDCR  R1,8
 FE10  1E0D          SBZ   13                 PREPARE TO SET BAUD RATE
 FE12  0204          LI    R4,BAUD            GET BAUD RATE
 FE14  001A
 FE16  3304          LDCR  R4,12              OUTPUT BAUD RATE
 FE18  1D0F          SBO   15                 PUT 9902 IN SELF TEST
 FE1A  1D10          SBO   16                 ENABLE RTS
 FE1C  1E12          SBZ   18
 FE1E  3201          LDCR  R1,8               OUTPUT PATTERN
 FE20  1F15  TEST2   TB    21                 DID WE RECEIVE A CHARACTER
 FE22  16FE          JNE   TEST2              NO: KEEP LOOKING
 FE24  3602          STCR  R2,8               YES: BRING IT IN
 FE26  9042          CB    R2,R1              IS IT THE RIGHT ONE
 FE28  1601          JNE   TEST3              NO: LEAVE LED ON
 FE2A  1D24          SBO   36                 YES: TURN OFF LED
 FE2C  022C  TEST3   AI    R12,SIZE           POINT TO NEXT PORT
 FE2E  0080
 FE30  028C          CI    R12,END            ALL PORTS CHECKED?
 FE32  0400
 FE34  1AE9          JL    TEST1              NO: CONTINUE
 FE36  020C          LI    R12,LED            YES: POINT TO AUTO DIAL LED
 FE38  026E
 FE3A  0603  TEST4   DEC   R3                 DECREMENT TIME COUNTER
 FE3C  16FE          JNE   TEST4              TIME OUT?
 FE3E  3045          LDCR  R5,1               YES: CHANGE STATE OF LED
 FE40  0545          INV   R5                 TOGGLE LED FLAG
 FE42  10FB          JMP   TEST4              CONTINUE
```

FIGURE 2-6. CODE TO TEST PORT WRITE AND READ

SECTION 3

PROGRAMMING THE TM 990/307

3.1 GENERAL

The four ports of the TM 990/307 can be programmed for the following functions:

- Read characters coming in to the TMS 9902
- Transmit characters via the TMS 9902
- Set baud rates, parity, character length, and other transmission specifications at the TMS 9902
- Turn onboard LEDs on and off
- Test the preset values at the two-bit data level switches
- Autocalling
- Modem operation
- Interrupt operation

Programming is through the Communications Register Unit (CRU) which is described in detail in your microcomputer user's guide. There are five CRU instructions, three single bit (SBZ, SBO, and TB) and two multibit (LDCR and STCR) CRU instructions. When executed, CRU instructions place an address on the address lines and then either (1) send one (or more) bits over the CRUOUT line of the microprocessor or (2) receive one (or more) bits at the CRUIN line or test the binary value at the CRUIN line. The desired address is first placed in register 12 before instruction execution; an address-line decoder then selects which CRU device to be enabled so that it can be accessed through the CRU input (CRUIN) or output (CRUOUT) lines. The relationship between the CRU bit address, the hardware base address and the software base address is shown in Figure 3-1 for the TMS 9900 microprocessor (the addressing varies somewhat for the TMS 9981 microprocessor, see your user's manual). Note that the CRU bit address is the resulting value on address lines A3 to A14 of the TM 990/307. This address line value is derived by adding a signed displacement (single-bit CRU instructions only) to the binary values in bits 3 to 14 of register 12 (bit 15 of register 12 is ignored), and then applying this sum on to address lines A3 to A14 of the TM 990/307.

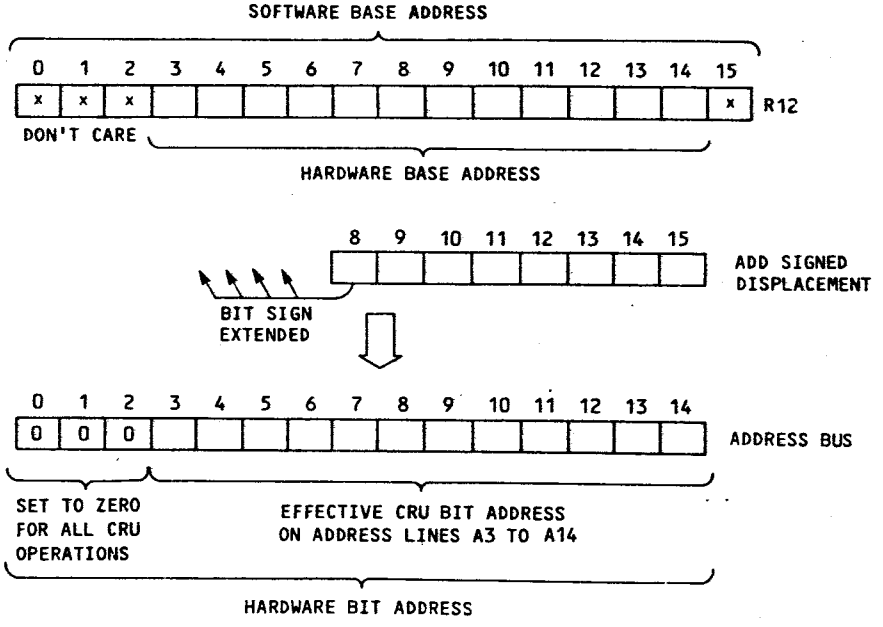


FIGURE 3-1. CRU ADDRESSING SCHEME

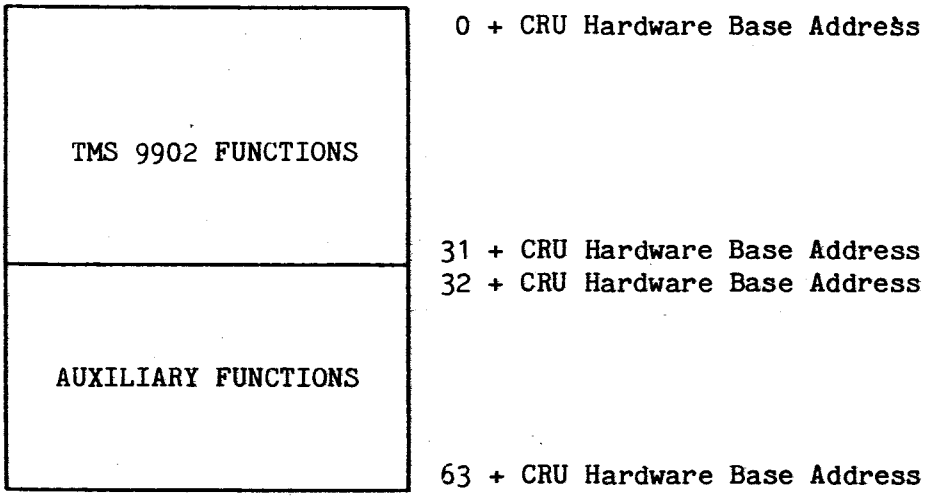


FIGURE 3-2. 64-BIT CRU ADDRESS AREA FOR EACH PORT

3.2 SELECTING THE CRU BASE ADDRESS

When CRU instructions are executed, address bus lines A3 to A14 are used to access the desired devices at a port. Each port represents 64 (40_{16}) bits of CRU addressing area with the port TMS 9902 at the start of the CRU area and the auxiliary functions at the end of the area. This 64-bit area is shown in Figure 3-2. When a CRU instruction is executed, address line assignments are as follows:

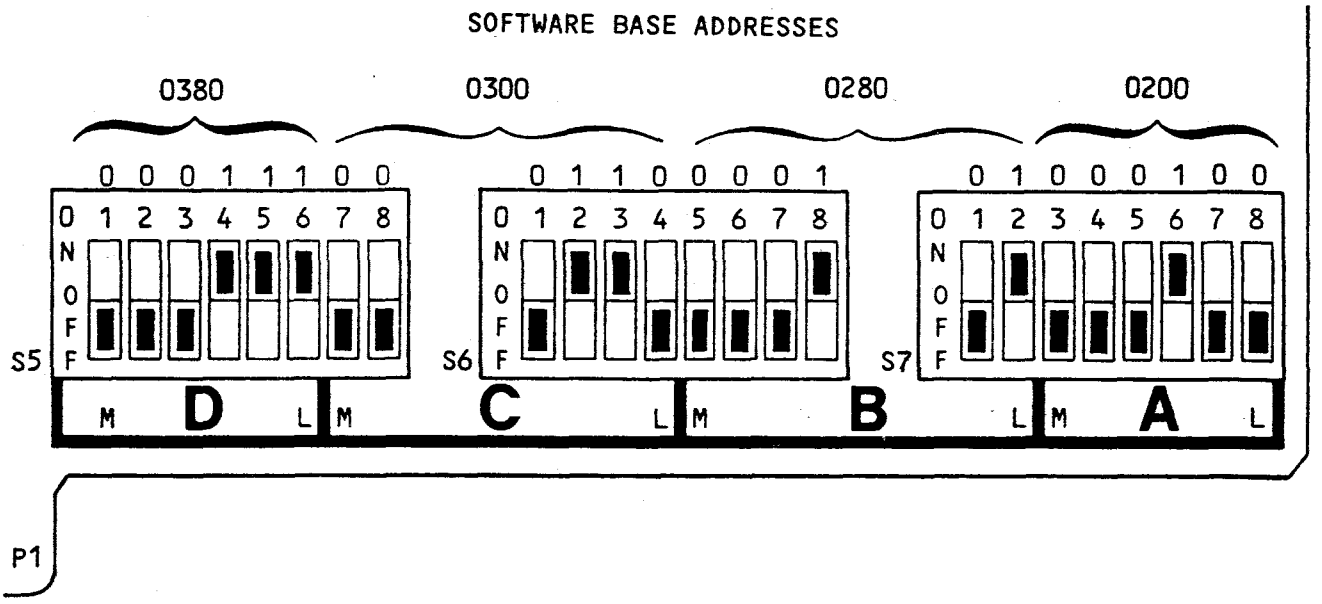
NOTE

The base address selected in switches S5, S6 and S7 as shown in Figure 3-3 must be different for each port.

- A3 to A8: These six lines are decoded and compared to the values set in DIP switches A, B, C, and D for ports A to D. If a match, the 64-bit CRU area can be driven via the address line values at A9 through A14 (these lines are explained below). The 24 DIP switches, in four groups of six, are labeled A to D -- corresponding to ports A to D -- and are located adjacent to connector P1. The leftmost switch in each group (marked M) represents the Most significant bit (line A3 equivalent), and the rightmost switch (marked L) is the Least significant bit (line A8). Switch settings are explained in detail in subsection 2.3.2. Figure 3-3 depicts switch settings that place the four TMS 9902s at the following CRU software base addresses (used in examples in this section):

  - Port A at 0200_{16}
  - Port B at 0280_{16}
  - Port C at 0300_{16}
  - Port D at 0380_{16}

- A9: Each port (A to D) represents 64 bits of CRU address space. The first 32 bits address the TMS 9902 for that port; the second 32 bits are for auxiliary functions (not all the second 32 bits are used). Address



Notes: 1. The dark area on switch is the position pressed.
2. Resulting CRU software base addresses (hex): Port A, 0200; Port B, 0280; Port C, 0300; Port D, 0380. These are used in examples in this section.

FIGURE 3-3. EXAMPLE OF SETTING CRU ADDRESSES AT SWITCHES S5, S6, AND S7

line A9 selects which 32-bit block will be affected by the values on address lines A10 to A14:

- If this line (A9) is a zero, the first 32 CRU bits that control the TMS 9902 are addressed starting with bit 0. The value on address lines A10 to A14 determine which specific TMS 9902 bit is addressed.

- If this line is a one, the second 32 bits that control auxiliary functions such as modem communication and the LEDs are addressed. The value on address lines A10 to A14 determine which specific auxiliary bit is being addressed.

- A10 to A14: These five lines (least significant bits) drive the TMS 9902 address select lines S0 (MSB) to S4 (LSB) respectively or drive the auxiliary bits such as the LEDs or modem signals (second 32 bits of the 64-bit area depending upon the value of address line A9 -- see above). It would be normal programming practice to specify the value on these lines via a displacement in the operand of a single-bit CRU instruction.

Table 3-1 lists the CRU bit assignments (signals and corresponding CRU address) in the 64-bit CRU area that can be addressed for port A and the autocall port, and Table 3-2 lists the CRU bit assignments for ports B, C, and D. Note that the 32 low-order (least-significant) bits control the TMS 9902, and the 32 high-order bits are used for modem, LED, and autocall control, Of these latter 32 bits, not all are used; over half are reserved for future use.

TABLE 3-1. CRU ADDRESSING FOR PORT A (Page 1 of 2)

Values on Address Lines[1] (Hex) (Note 1)		Dis-placement (Base 10)	Device and Device Signals			
			Input Description		Output Description	
A3 to A8	A9 to A14					
	00	00	RBR0	Rec buffer data	REG0	Register data bit 0
	01	01	RBR1		REG1	
	02	02	RBR2		REG2	
	03	03	RBR3		REG3	
	04	04	RBR4		REG4	
	05	05	RBR5		REG5	(Note 2)
	06	06	RBR6		REG6	
	07	07	RBR7	Rec buffer data	REG7	
	08	08	0		REG8	
	09	09	RCVERR	Receive error	REG9	
	0A	10	RPER	Receive parity error	REG10	Register data bit 10
	0B	11	ROVER	Receive overun error	LXDR	Load transmit data reg
	0C	12	RFER	Receive framing error	LRDR	Load receive data reg
Same	0D	13	RFBD	Receive full bit	LDIR	Load interval register
as	0E	14	RSBD	Receive start bit	LDCTRL	Load control register
the	0F	15	RIN	RIN pin status	TSTMD	Test mode
six						
swit-	10	16	RBINT	Receive interrupt	RTSON	Request to send is on
ches	11	17	XBINT	Transmit intrrupt	BRKON	Break on
for	12	18	0		RIENB	Receive interrupt enbl
Port	13	19	TIMINT	Timer interrupt	XBIENB	Xmit interrupt enable
A	14	20	DSCINT	Data set change intrp	TIMENB	Timer interrupt enable
	15	21	RBRL	Rcv buffer reg loaded	DSCENB	Data set chg intr enbl
	16	22	XBRE	Trnsmt buffer empty		
	17	23	XSRE	Trnsmt shft reg empty		
	18	24	TIMERR	Timer error		
	19	25	TIMELP	Timer elapsed		
	1A	26	RTS	Request to send		
	1B	27	DTR	Data term ready		
	1C	28	CTS	Clear to send		
	1D	29	DSCH	Data set status chng		
	1E	30	FLAG	Register load/break		
	1F	31	INT	Interrupt	RESET	Reset TMS 9902

NOTES: 1. The values in address lines 9 to 14 are also the displacement in hexadecimal from the CRU hardware base address.

2. In Register data bits 1 to 10, the TMS 9902 receives data for the following internal registers:
   - Control Register (character length, clock division, parity, and number of stop bits),
   - Receive Data Rate Register (set baud rate if different from that set in the Transmit Data Rate Register),
   - Interval Register (interval timer setting), and
   - Transmit Data Rate Register (set baud rate if different from that in the Receive Rate Register).

TABLE 3-1. CRU ADDRESSING FOR PORT A (Page 2 of 2)

Values on Address Lines (Hex) (Note 1) A3 to A8	A9 to A14	Displacement (Base 10)	Device and Device Signals: Input Description		Output Description		
	20	32	DTR	Data terminal ready	DTR	Data terminal ready	MODEM
	21	33	DSR	Data set ready			
	22	34	RI	Ring indicator			
	23	35					
	24	36	Data Level Sw LSB (S8-7)[3]		LED	Port A LED (DS1)	
	25	37	Data Level Sw MSB (S8-8)[3]				
	26	38					
	27	39					
	28	40	DTR	Data terminal ready	DTR	Data terminal ready	MODEM
	29	41	DSR	Data set ready			
	2A	42	RI	Ring indicator			
Same	2B	43					
as	2C	44	Data Level Sw LSB (S8-7)[3]		LED	Port A LED (DS1)	
the	2D	45	Data Level Sw MSB (S8-8)[3]				
six	2E	46					
swit-	2F	47					
ches							
for	30	48			NB1	Number bit 1	AUTO CALL
Port	31	49	PWI	Power indication	NB2	Number bit 2	
A	32	50	DSS	Data set status	NB4	Number bit 4	
	33	51	ACR	Abandon call, retry	NB8	Number bit 8	
	34	52	PND	Present next digit	DPR	Digit present	
	35	53	DLO	Data line occupied	CRQ	Call request	
	36	54					
	37	55			LED	Autocall LED (DS5)	
	38	56			NB1	Number bit 1	
	39	57	PWI	Power indication	NB2	Number bit 2	
	3A	58	DSS	Data set status	NB4	Number bit 4	
	3B	59	ACR	Abandon call, retry	NB8	Number bit 8	
	3C	60	PND	Present next digit	DPR	Digit present	
	3D	61	DLO	Data line occupied	CRR	Call request	
	3E	62					
	3F	63			LED	Autocall LED (DS5)	

NOTES (Continued):

3. Switches 1 to 8 at DIP S8 are shown in Figure 3-7 in the back of this section. Programming is explained in subsection 3.3.5. These switches can be set as desired by the user, then interpreted by the user program.

TABLE 3-2. CRU ADDRESSING FOR PORTS B, C, AND D (Page 1 of 2)

Values on Address Lines (Hex) (Note 1)		Dis-placement (Base 10)	Device and Device Signals			
			Input Description		Output Description	
A3 to A8	A9 to A14					
	00	0	RBR0	Rec buffer data	REG0	Register data bit 0
	01	1	RBR1		REG1	
	02	2	RBR2		REG2	
	03	3	RBR3		REG3	
	04	4	RBR4		REG4	
	05	5	RBR5		REG5	(Note 2)
	06	6	RBR6		REG6	
	07	7	RBR7	Rec buffer data	REG7	
	08	8	0		REG8	
	09	9	RCVERR	Receive error	REG9	
	0A	10	RPER	Receive parity error	REG10	[1]Register data bit 10
	0B	11	ROVER	Receive overun error	LXDR	Load transmit data reg
	0C	12	RFER	Receive framing error	LRDR	Load receive data reg
Same	0D	13	RFBD	Receive full bit	LDIR	Load interval register
as	0E	14	RSBD	Receive start bit	LDCTRL	Load control register
the	0F	15	RIN	RIN pin status	TSTMD	Test mode
six						
swit-	10	16	RBINT	Recieve interrupt	RTSON	Request to send is on
ches	11	17	XBINT	Transmit intrrupt	BRKON	Break on
for	12	18	0		RIENB	Receive interrupt enbl
Ports	13	19	TIMINT	Timer interrupt	XBIENB	Xmit interrupt enable
B to	14	20	DSCINT	Data set change intrp	TIMENB	Timer interrupt enable
D	15	21	RBRL	Rcv buffer reg loaded	DSCENB	Data set chg intr enbl
	16	22	XBRE	Trnsmt buffer empty	Not Used	
	17	23	XSRE	Trnsmt shft reg empty	Not Used	
	18	24	TIMERR	Timer error	Not Used	
	19	25	TIMELP	Timer elapsed	Not Used	
	1A	26	RTS	Request to snd	Not Used	
	1B	27	DTR	Data term ready	Not Used	
	1C	28	CTS	Clear to send	Not Used	
	1D	29	DSCH	Data set status chng	Not Used	
	1E	30	FLAG	Register load/break	Not Used	
	1F	31	INT	Interrupt	RESET	Reset TMS 9902

NOTES: 1. The values in address lines 9 to 14 are also the displacement in hexadecimal from the CRU hardware base address.

2. In Register data bits 1 to 10, the TMS 9902 receives data for the following internal registers:
   - Control Register (character length, clock division, parity, and number of stop bits),
   - Receive Data Rate Register (set baud rate if different from that set in the Transmit Data Rate Register),
   - Interval Register (interval timer setting), and
   - Transmit Data Rate Register (set baud rate if different from that in the Receive Rate Register).

TABLE 3-2. CRU ADDRESSING FOR PORTS B, C, AND D (Page 2 of 2)

Values on Address Lines (Hex) (Note 1) A3 to A8	A9 to A14	Displacement (Base 10)	Device and Device Signals				
			Input Description		Output Description		
	20	32	DTR	Data terminal ready	DTR	Data terminal ready	MODEM
	21	33	DSR	Data set ready	DTR	Data terminal ready	MODEM
	22	33	RI	Ring indicator	DTR	Data terminal ready	MODEM
	23	35			DTR	Data terminal ready	MODEM
	24	36	Data Level Sw LSB (S8-5,3,1)[3]		LED	LED for port	
	25	37	Data Level Sw MSB (S8-6,2,4)[3]		LED	LED for port	
	26	38			LED	LED for port	
	27	39			LED	LED for port	
	28	40	DTR	Data terminal ready	DTR	Data terminal ready	MODEM
	29	41	DSR	Data set ready	DTR	Data terminal ready	MODEM
	2A	42	RI	Ring indicator	DTR	Data terminal ready	MODEM
	2B	43			DTR	Data terminal ready	MODEM
	2C	44	Data Level Sw LSB (S8-5,3,1)[3]		LED	LED for port	
Same	2D	45	Data Level Sw MSB (S8-6,4,2)[3]		LED	LED for port	
as	2E	46			LED	LED for port	
the	2F	47			LED	LED for port	
six							
swit-	30	48	DTR	Data terminal ready	DTR	Data terminal ready	MODEM
ches	31	49	DSR	Data set ready	DTR	Data terminal ready	MODEM
for	32	50	RI	Ring indicator	DTR	Data terminal ready	MODEM
Ports	33	51			DTR	Data terminal ready	MODEM
B, C,	34	52	Data Level Sw LSB (S8-5,3,1)[3]		LED	LED for port	
& D	35	53	Data Level Sw MSB (S8-6,4,2)[3]		LED	LED for port	
	36	54			LED	LED for port.	
	37	55			LED	LED for port	
	38	56	DTR	Data terminal ready	DTR	Data terminal ready	MODEM
	39	57	DSR	Data set ready	DTR	Data terminal ready	MODEM
	3A	58	RI	Ring indicator	DTR	Data terminal ready	MODEM
	3B	59			DTR	Data terminal ready	MODEM
	3C	60	Data Level Sw LSB (S8-5,3,1)[3]		LED	LED for port	
	3D	61	Data Level Sw MSB (S8-6,4,2)[3]		LED	LED for port	
	3E	62			LED	LED for port	
	3F	63			LED	LED for port	

NOTES (Continued):

3. Data level switches 1 to 8 at DIP S8 are shown in Figure 3-7 and explained in subsection 3.3.5. Only the switches corresponding to the port addressed can be read at the displacement shown (e.g., if Port B is addressed, only S8-5 or S8-6 can be decoded at the displacement shown in the table above).

3.3 PROGRAMMING EXAMPLES

NOTE

In this subsection, mention is made of the registers and CRU bit functions of the TMS 9902. It is presumed that the reader is familiar with the TMS 9902; if not, the TMS 9902 data book is provided with this board for reference. Other programming examples can be found in this data book.

In the coding examples in this section, label CRUADR represents the software base address (R12 contents) for the program. For example purposes, the CRU software base addresses for each port are as listed below. Note that they have been chosen to be contiguous CRU areas, each 64_{10} (40_{16}) bits apart. The switch settings at the CRU address switches would have to conform to these settings as described in paragraph 2.3.2.

- Port A: 0200_{16}
- Port B: 0280_{16}
- Port C: 0300_{16}
- Port D: 0380_{16}

Other examples of programming the TMS 9902 are provided in the "TMS 9902 Asynchronous Communication Controller" data book and the "TM 990/401-3 TIBUG Monitor Listing" (P/N 1602013-9701).

3.3.1 Initialize TMS 9902 (Figures 3-4 and 3-5)

TMS 9902 initialization requires setting one or more internal registers:

- Control Register: Number of stop bits, parity, timer time base, and character length.
- Interval Register: Length of timer countdown to zero.
- Receive Data Rate Register: Receive baud rate.
- Transmit Data Rate Register: Transmit baud rate.

As explained in the TMS 9902 data manual, these registers are loaded by writing to bits 0-7 or 0-10 of the TMS 9902 CRU base address after initializing the registers either by setting CRU bits 11 to 14 or by setting bit 31 for a RESET (after setting the RESET bit, no input operation should occur for 11 clock cycles). Table 3-3 shows the required logic of CRU bits 11 to 14 to enable the loading of these registers. The registers occupy CRU bits 0-7 or bits 0-10.

TABLE 3-3. CRU-BIT LOGIC TO ENABLE TMS 9902 REGISTERS

Register(s) to be Loaded	CRU Bit Setting (Displacement from CRU Base Address)				
	Bit 14	Bit 13	Bit 12	Bit 11	Register Occupies Bits
Control Register	1	X	X	X	0 to 7
Interval Register	0	1	X	X	0 to 7
Both Receive and Transmit D. R. Regs*	0	0	1	1	0 to 10
Receive Data Rate Register only	0	0	1	0	0 to 10
Transmit Data Rate Register only	0	0	0	1	0 to 10

*Loading the Receive and Transmit Data Rate Registers at the same time loads them with the same baud rate.
X = don't care

Figure 3-4 shows example code to load the Control Register. Figure 3-5 shows example code to load all four registers. The enabling bits for these registers will be set to one upon a RESET (CRU bit 31 set to one); this allows writing to the register using the logic shown in Table 3-3 and used in Figure 3-5.

NOTE

After a register is loaded, its enabling bit is automatically reset to zero. This feature allows programming consecutive registers, beginning with the Control Register, without having to reset the enabling bit of the just-loaded register to obtain the logic patterns shown in Table 3-3 (i.e., load the Control Register, then the Interval Register, then the Data Rate Registers for programming ease).

Control Register. Stop bits, parity, clock division, and character length are set by writing to the TMS 9902 Control Register. See Figures 3-4 and 3-5.

The clock divide value allows choosing to divide the external clock input at pin 16 by a value of 3 or 4 using the following:

- CLK4M a one means divide by 4 (f_{int} = 1 MHz @ 4 MHz clock)
- CLK4M a zero means divide by 3 (f_{int} = 1 MHz @ 3 MHz clock)

Interval Register. The Interval Register contains the binary value to be counted down for timing. When the countdown reaches zero, an interrupt is issued if enabled by writing a one to CRU bit 20. If f_{int} = 1 MHz (see Control Register), each count lasts 64 usec.

Receive Data Rate Register. This register is set to the desired baud rate of the incoming data. For the Receive Data Rate and Transmit Data Rate Registers, CRU bits 0 to 10 contain register value. If f_{int} = 1 MHz (see Control Register) then baud rate is equal to 1 Mbps/(register value x 2) if bit 10 is a zero, or 1 Mbps/(register value x 2 x 8) if bit 10 is a one.

Transmit Data Rate Register. This register is set to the desired baud rate of the data to be transmitted (see Receive Data Rate Register above).

3.3.2 Receive Character Through Port A TMS 9902 (Figure 3-6)

A high-to-low transition on external line RIN (pin 3) activates the receiver circuitry of the TMS 9902. In the third line of Figure 3-6, bit 21 (RBRL) is tested to see that the Receive Buffer Register is loaded with a full character via the TMS 9902 RIN line (pin 3). Writing to bit 18 (RIENB) resets bit 21 so that it can be checked again for the next character received. Note that after resetting the TMS 9902 via the RESET bit (31), no input operation should occur for 11 clock cycles.

3.3.3 Transmit Character(s) Through Port A TMS 9902 (Figure 3-7)

Writing a one to bit 16 (RTSON) enables the external RTS- line (pin 5) low which is interpreted by the peripheral device. When the external CTS- line (pin 6) goes low, the transmitter is enabled. Bit 22 (XBRE) is tested to verify that the transmit buffer register is presently empty. Then the character is written to the TMS 9902 via the CRUOUT line of the host (to receive characters, the Transmit Buffer Register must be active, i.e., the other four TMS 9902 registers -- Control, Interval, and both Data Rate

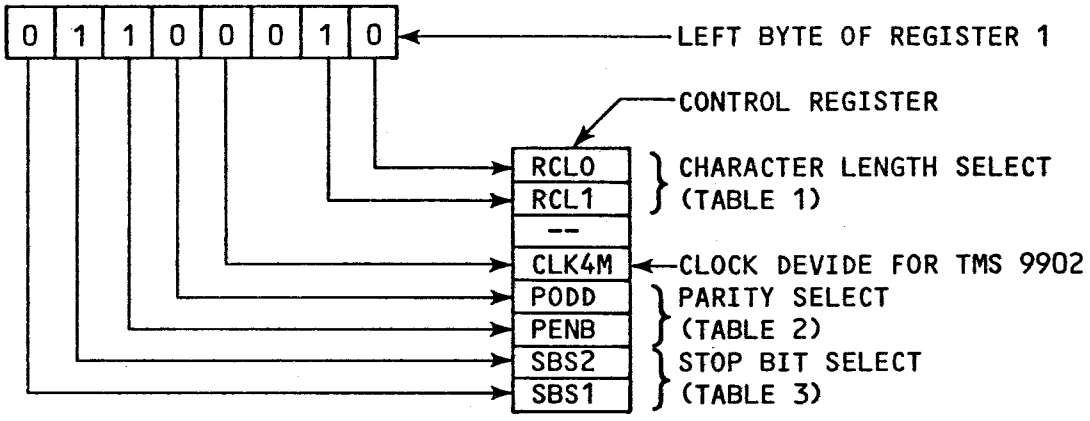


TABLE 1
CHARACTER LENGTH SELECTION

RCL1 BIT 1	RCL0 BIT 0	CHARACTER LENGTH
0	0	5 BITS
0	1	6 BITS
1	0	7 BITS
1	1	8 BITS

TABLE 2
PARITY SELECTION

PENB BIT 5	PODD BIT 4	PARITY
0	0	NONE
0	1	NONE
1	0	EVEN
1	1	ODD

TABLE 3
STOP BIT SELECTION

SBS1 BIT 7	SBS2 BIT 6	NUMBER OF TRANSMITTED STOP BITS
0	0	1½
0	1	2
1	0	1
1	1	1

```
LI    R1,>6200      LEFT BYTE CONTAINS CONTROL BITS
LI    R12,CRUADR    SET PORT CRU SOFTWARE BASE ADDRESS
SBO   31            RESET TMS 9902
LDCR  R1,8          APPLY BITS TO CONTROL REGISTER
```

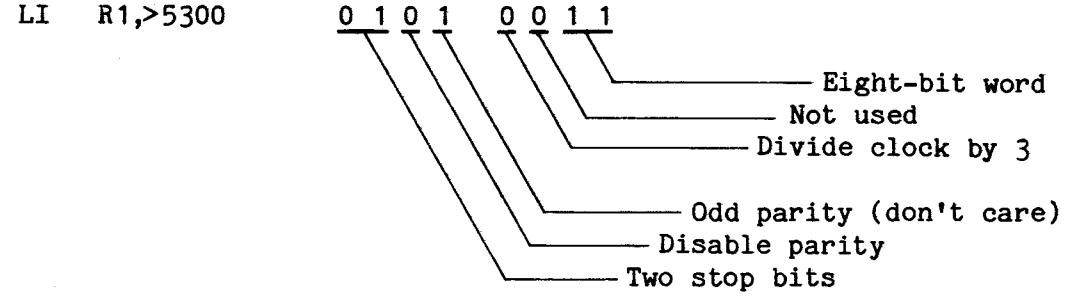
FIGURE 3-4. LOADING THE TMS 9902 CONTROL REGISTER

```
        LI    R12,CRUADR    CRU BASE ADDRESS IN R12
*RESET THE TMS 9902 (FOLLOW WITH NO-OP FOR STABILIZATION)
        SBO   31            RESET TMS 9902, ALL REG. LOAD BITS = 1
        NOP                 NO-OP TO USE 11 CYCLES OF 9902 CLOCK
*LOAD THE CONTROL REGISTER (REG. CONTENTS EXPLAINED BELOW)
        LI    R1,>5300      LOAD CONTROL REGISTER
        LDCR  R1,8          APPLY TO CONTROL REGISTER
** THE LOAD CONTROL REGISTER BIT AUTOMATICALLY RESET TO ZERO
*LOAD THE INTERVAL REGISTER
        LI    R1,>9C00      >9C YIELDS 9.984 MILLISECONDS
        LDCR  R1,8          APPLY TO INTERVAL REGISTER
** THE INTERVAL REGISTER BIT WAS AUTOMATICALLY RESET TO ZERO
*LOAD THE RECEIVE DATA RATE REGISTER (REG. EXPLAINED BELOW)
        LI    R1,>638       >0638 YIELDS 110.04 BITS PER SECOND
        LDCR  R1,10         APPLY TO RECEIVE DATA RATE REGISTER
** THE RCV DATA RATE REGISTER BIT WAS AUTOMATICALLY RESET TO ZERO
*LOAD THE TRANSMIT DATA RATE REGISTER
        LI    R1,>01A1      >01A1 YIELDS 1200 BITS PER SECOND
        LDCR  R1,11         APPLY TO TRANSMIT DATA RATE REGISTER
** ELEVENTH BIT CLEARS TRANSMIT DATA RATE BIT, READIES FOR
** LOADING THE TRANSMIT BUFFER REGISTER WITH A CHARACTER
```

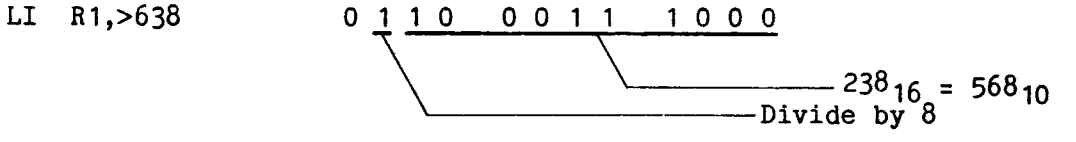
NOTE

If the same baud rate is needed for transmit as well as receive, delete the Load Receive Data Rate Register code above; then the Load Transmit Rate Register code also loads the Receive Data Rate Register as both CRU bits 11 and 12 are ones.

(a) Code to Initialize the TMS 9902



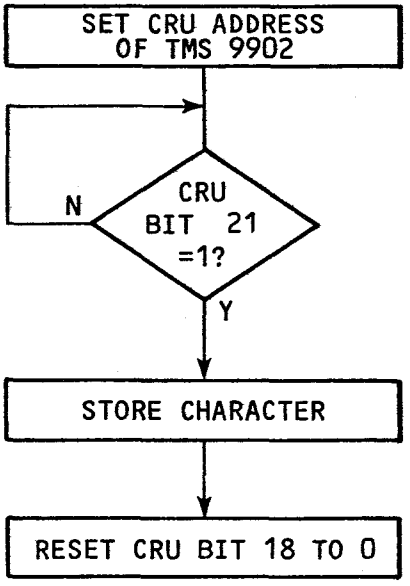
(b) Control Register Code



1 M/(568 x 2 x 8) = 110.04 bps baud rate

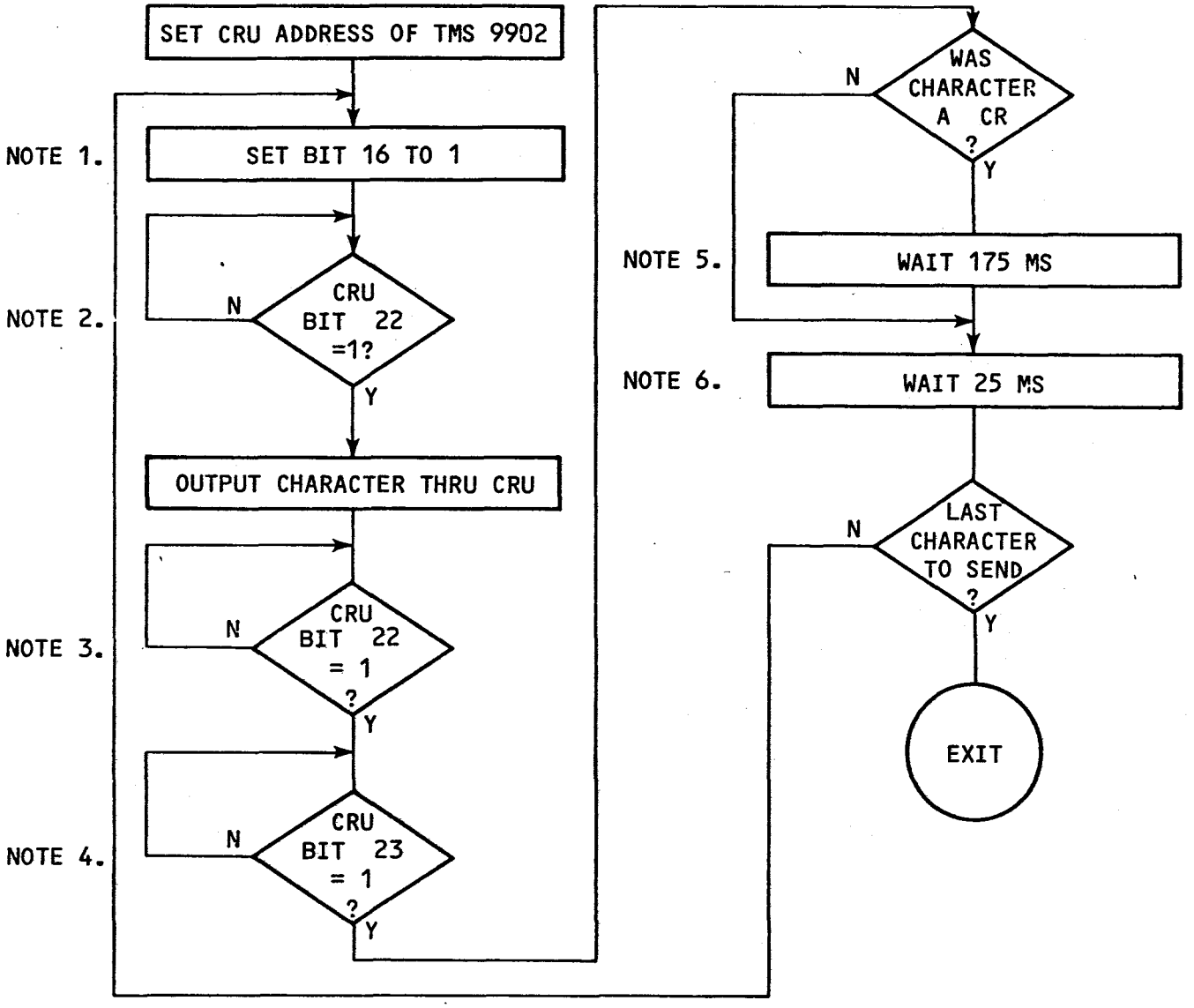
(c) Receive Data Rate Register Code

FIGURE 3-5. LOADING THE FOUR REGISTERS ON THE TMS 9902




```
        LI    R12,CRUADR    TMS 9902 CRU ADDRESS  IN R12
        LI    R1,STORE      MEMORY ADDRESS TO STORE CHARACTERS
        .
        .
        .
LOOP    TB    21            HAS CHARACTER BEEN RECEIVED (RBRL=1?)
        JNE   LOOP          NO, LOOP TO WAIT FOR CHARACTER
        STCR  R2,8          BRING 8-BIT CHARACTER TO R2
        CI    R2,>0400      WAS CHARACTER AN EOT?
        JEQ   EXIT          YES, EXIT
        MOVB  R2,*R1+       STORE CHARACTER IN MEMORY
        SBZ   18            RESET RBRL FLAG (OUTPUT BIT 21)
        JMP   LOOP          GET NEXT CHARACTER
EXIT
        .
        .
        .
```

FIGURE 3-6. RECEIVE CHARACTER(S) SAMPLE CODE



NOTES

1. TURN ON RTS
2. WAIT FOR TMS 9902 TRANSMIT BUFFER REGISTER TO BE EMPTY (XBRE = 1 ?)
3. WAIT FOR TMS 9902 TRANSMIT BUFFER REGISTER TO BE EMPTY (XBRG = 1)
4. WAIT FOR TMS 9902 TRANSMIT SHIFT REGISTER TO BE EMPTY (XSRE = 1)
5. A CARRIAGE RETURN ON A 733 ASR/KSR REQUIRES 200 MS DELAY FOR PRINTHEAD TRAVEL
6. A CHARACTER ON A 733 ASR/KSR REQUIRES 25 MS DELAY FOR 300 BAUD OPERATION

FIGURE 3-7. TRANSMIT CHARACTER(S) SAMPLE CODE (SHEET 1 OF 2)

```
        CLR   R2            INITIALIZE TEMPORARY STORAGE
        LI    R12,CRUADR    CRU SOFTWARE BASE ADDRESS
        LI    R1,STORE      STORAGE FOR RECEIVED CHARACTERS
        .
        .
        .

LOOP6   LI    R3,26253      LOOP COUNT FOR 175 MILLISECOND DELAY
        LI    R4,3750       LOOP COUNT FOR  25 MILLISECOND DELAY
        SBO   16            SET RTS TO ONE
LOOP1   TB    22            IS TRANSMIT BUFFER EMPTY?
        JNE   LOOP1         NO, WAIT UNTIL EMPTY
        LDCR  *R1,8         CHARACTER TO TMS 9902 VIA CRUOUT
LOOP2   TB    22            IS TRANSMIT BUFFER EMPTY?
        JNE   LOOP2         NO, WAIT UNTIL CHARACTER MOVED
LOOP3   TB    23            IS TRANSMIT SHIFT REGISTER EMPTY?
        JNE   LOOP3         NO, WAIT UNTIL CHARACTER SENT
        MOVB  *R1+,R2       MOVE CHARACTER TO R2
        CI    R2,>0D00      WAS IT A CARRIAGE RETURN?
        JNE   LOOP5         NO, SKIP EXTRA 175 MS DELAY
LOOP4   DEC   R3            DECREMENT COUNTER FOR 175 MS
        JNE   LOOP4         LOOP FOR 175 MS
LOOP5   DEC   R4            DECREMENT COUNTER FOR 25 MS
        JNE   LOOP5         LOOP FOR 25 MS
        CI    R2,0          WAS THAT LAST CHARACTER = 00?
        JNE   LOOP6         NO, GET NEXT CHARACTER
        .
        .
        .
```

NOTE

Above values are accurate for a 3 MHz system clock

FIGURE 3-6. TRANSMIT CHARACTER(S) SAMPLE CODE (SHEET 2 OF 2)

Registers -- must be disabled along with BREAKON). Bit 22 is then checked to see that the character has exited the TMS 9902 Receive Buffer Register, and then bit 23 is checked to see that the character has exited the Transmit Buffer Register so that proper timing can be set to pad characters for a particular baud rate. Characters are transmitted from the TMS 9902 via the XOUT line (pin 2). Note that after resetting the TMS 9902 via the RESET bit (31), no output operations should occur for 11 clock cycles.

3.3.4 Turn On LEDs at Ports A Through D

Each LED can be turned on by writing a zero to one of several CRU base addresses as listed in Tables 3-1 and 3-2. Conversely, the LED can be turned off by writing a one to the same CRU address. In these tables, the following are one (of several) effective displacements from the CRU hardware base address for LEDs DS1 to DS5:

- DS1 (Port A) to DS4 (Port D): 36_{10} from the hardware base address of the respective port.
- DS5 (Autocall): 55_{10} from the hardware base address of port A

The respective LED is lit by writing a zero (0) to its CRU bit address. The following example code will illuminate all five LEDs at the CRU address used for these examples:

```
LI    R12,>200      CRU SFTWR ADDR FOR PORT A,  AUTODIAL
SBZ   36            LIGHT PORT A LED (DS1)
SBZ   55            LIGHT AUTODIAL LED (DS5)
LI    R12,>280      CRU SOFTWARE BASE ADDRESS FOR PORT B
SBZ   36            LIGHT PORT B LED (DS2)
LI    R12,>300      CRU SOFTWARE BASE ADDRESS FOR PORT C
SBZ   36            LIGHT PORT C LED (DS3)
LI    R12,>380      CRU SOFTWARE BASE ADDRESS FOR PORT D
SBZ   36            LIGHT PORT D LED (DS4)
```

3.3.5 Read Data Level Decoder Switches

Ports A to D (<u>not</u> the autodial port) have two SPST switches at DIP package S8 which can be read (one or zero) via the CRU. Interpretation of these switches is up to the user's needs. For example, a common service routine for all four ports could read each switch pair and determine by their (binary) contents and a lookup table what baud rate to set for each specific port. In this way the user merely attaches the desired peripheral to the ports, set the switches to the prescribed code, and call for an initialization routine that sets the correct baud rate. Other uses are restricted only by the imagination.

The CRU bits that address the two switches come in pairs as shown in Tables 3-1 and 3-2. Note that in Figure 3-7 that the switch pairs are arranged from top to bottom to correspond to ports A to D as seen from the front of the board. However the top switch for any switch pair (even-numbered 8 to 2) is read by the most significant CRU bit of the two CRU bits and the bottom switch of each pair (odd-numbered 1 to 7) is read by the least significant CRU bit.

Switches are read as follows:

- A one is read from switches set to ON
- A zero is read from switches set to OFF.

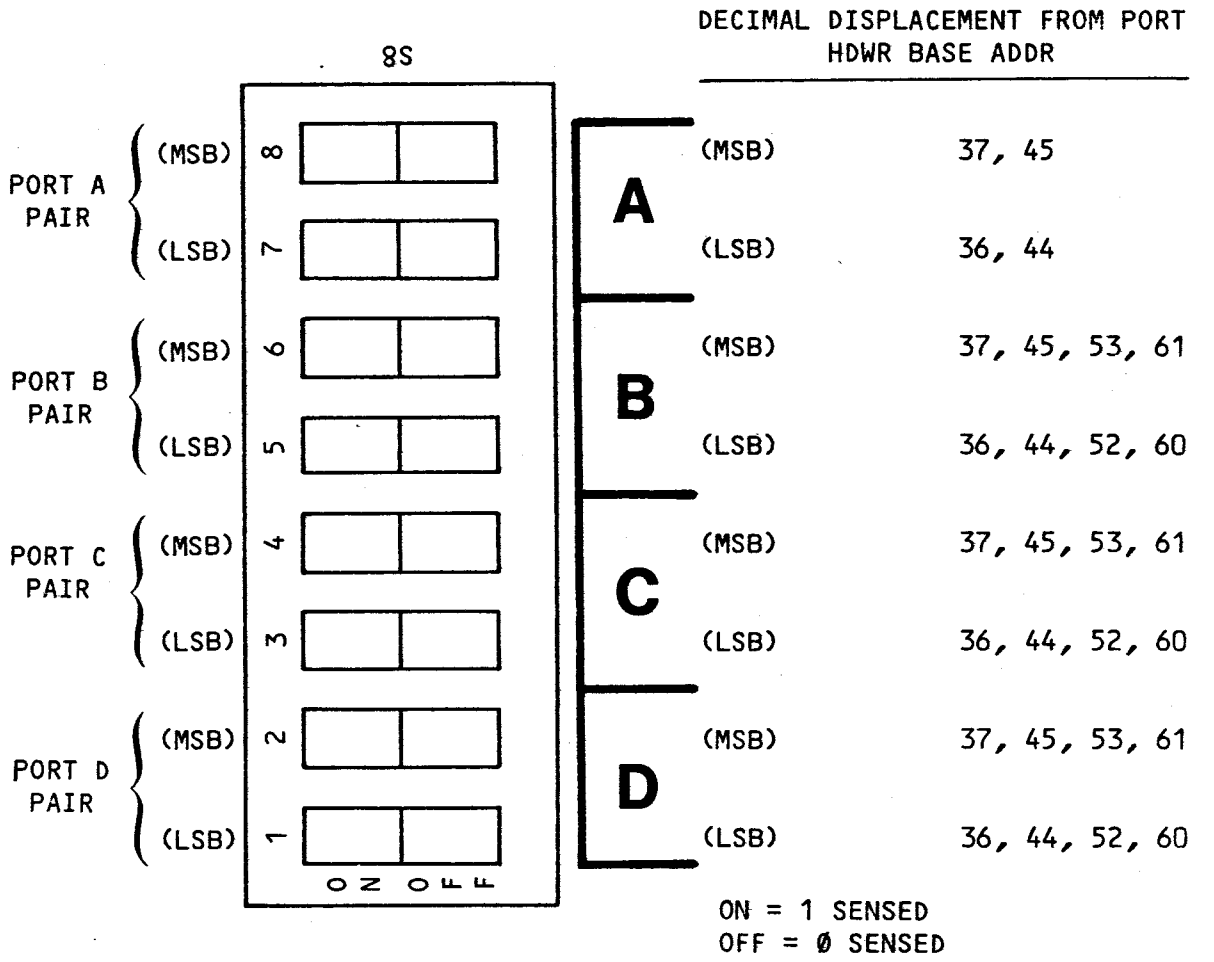


FIGURE 3-8. DATA LEVEL DECODER SWITCHES

Using the prescribed CRU software base addresses, the following code reads switches 8, 7, 6, and 5. If a one is found, the program exits to a particular routine; otherwise, the next switch is read.

```
        LI      R12,>200        PORT A CRU SOFTWARE BASE ADDRESS
SW8     TB      37              IS SW8-8 A ONE?
        JNE     SW7             NO, CHECK NEXT SWITCH (7)
        BL      @SUBRT8         YES, GO TO SUBROUTINE FOR SWITCH 8
SW7     TB      36              IS SW8-7 A ONE?
        JNE     SW6             NO, CHECK NEXT SWITCH (6)
        BL      @SUBRT7         YES, GO TO SUBROUTINE FOR SWITCH 7
        LI      R12,>280        PORT B CRU SOFTWARE BASE ADDRESS
SW6     TB      37              IS SW8-6 A ONE?
        JNE     SW5             NO, CHECK NEXT SWITCH (5)
        BL      @SUBRT6         YES, GO TO SUBROUTINE FOR SWITCH 6
SW5     TB      36              IS SW8-5 A ONE?
        JNE     EXIT            NO, EXIT
        BL      @SUBRT5         YES, GO TO SUBROUTINE FOR SWITCH 5
EXIT    EQU     $               SWITCHES CHECKED, CONTINUE
        .
        .
        .
```

The following program can be loaded into memory and executed as an example of data level switch reading. This program tests all odd-numbered switches (1 to 7) at DIP S8. If ON, it lights the LED for that port. If OFF, the LED is turned off (i.e., if a one or ON is sensed at the switch CRU address, it inverts this value, and sends a zero to the LED which completes the circuit and lights the LED).

```
Memory Object
Addr.  Code

FE00 02E0          LWPI >FE60
FE02 FE60
FE04 020C  TEST    LI   R12,>0248
FE06 0248
FE08 3441  TEST1   STCR R1,1
FE0A 0541          INV  R1
FE0C 3041          LDCR R1,1
FE0E 022C          AI   R12,>80
FE10 0080
FE12 028C          CI   R12,>3C8
FE14 03C8
FE16 12F8          JLE  TEST1
FE18 10F5          JMP  TEST
```

3.3.6 Autocall Feature

Refer to documentation on the particular autocall mechanism used such as:

- Data Auxiliary Set 801C (Automatic Calling Unit) Interface Specification (American Telephone & Telegraph Company)
- Data Auxiliary Sets 801C3 and 801C4 for Automatic Calling -- Theory of Operation and Supplementary Information (American Telephone and Telegraph Company)

3.3.7 Modem Operation

Table 3-4 is a list of the signals used in modem operation.

TABLE 3-4. SIGNALS USED IN MODEM OPERATION

RS-232-C Circuit	Function	Pin at Port	Signal at 9902/3	Signal at Port[1]
AA	Protective Ground	-1		[2]FRAME GND.
BA	Transmitter Data	-2	RIN-	RECEIVED DATA.
BB	Receiver Data	-3	XOUT-	TRANSMITTED DATA.
AB	Signal Ground	-7		[2]SIGNAL GND.
CF	Data Carrier Detect	-8	RTS-	TERMINAL DATA CARRIER DETECT.
CD	Data Terminal Ready	-20	DSR-	TERMINAL DATA TERMINAL READY.
CE	Ring Indicator	-22	Note 3	RI.
DB	Transmission Signal	-15	SCT-	[4]EIA SCT.
DD	Receiver Timing	-17	SCR	[4]EIA SCR.
CB	Modem Clear to Send	-16	CTS-	[5]MODEM CLEAR TO SEND.
CC	Modem Data Set Ready	-19	Note 3	MODEM-DSR.
CD	Modem Data Term.Ready	-21	Note 3	MODEM DTR.

NOTES: [1]Final letter (A, B, C, or D) is not given for these signals to show which port described; for example, FRAME GND.A is for port A, FRAME GND.B is for port B, etc.

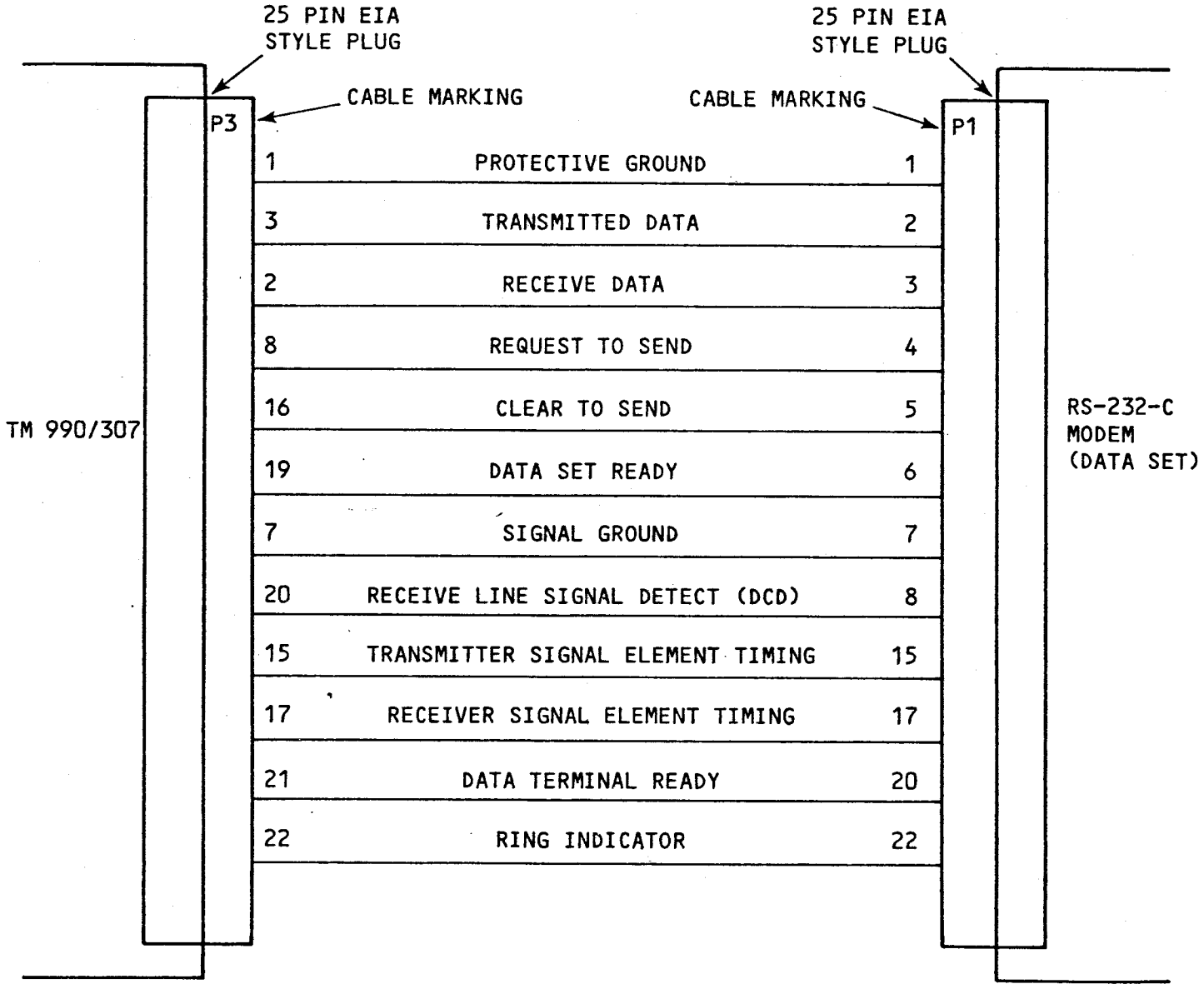
[2]Pins -1 and -7 (FRAME GND. and SIGNAL GND.) can be tied together via jumpers as shown in Table 2-4.

[3]Ring indicator, modem data set ready, and modem data terminal ready are CRU-addressable signals; these are shown in Tables 3-1 and 3-2.

[4]Pins -15 and -17 (EIA SCT. and EIA SCR.) are used for synchronous communication with a TMS 9903.

[5]Jumper E1 must be set E2-E3 for CTS- to connect to pin -16.

Wiring between the 25-pin edge connector and the modem is via a TM 990/506 cable. Pinouts of this cable are shown in Figure 3-6.



NOTE: SIGNAL NAME ASSIGNMENT IS PER EIA RS-232-C INTERFACE CONNECTIONS FOR INTERCONNECTION OF A DATA-ORIGINATING DEVICE TO A MODEM.

FIGURE 3-9. PINOUTS OF TM 990/506 CABLE BETWEEN MODEM AND EIA PORT

```
*PORT A CRU SOFTWARE BASE ADDRESS AT HEX 0200
*PORT B CRU SOFTWARE BASE ADDRESS AT HEX 0280
*PORT C CRU SOFTWARE BASE ADDRESS AT HEX 0300
*PORT D CRU SOFTWARE BASE ADDRESS AT HEX 0380
* EQUATES
TM9901 EQU  >0100          CRU ADDR OF TMS 9901 ON MICROCOMPUTER BRD
FLAG   EQU  R1             REG 1 IS FLAG REG TO SHOW PORT ISSUING INTERRUPT
A9902  EQU  >0200          CRU ADDR OF TMS 9902 FOR PORT A
C9902  EQU  >0300          CRU ADDR OF TMS 9902 FOR PORT C
RCVERR EQU  9              ERROR IN CHARACTER RECEIPT (READ BIT ON 9902)
RIENB  EQU  >12            ENABLE RECEIVER INTERRUPT (WRITE BIT ON 9902)
RBRL   EQU  >15            RECEIVE BUFFER HAS CHARACTER (READ BIT ON 9902)
       .
       .
       .

*SUBROUTINE TO ENABLE INTERRUPT 8 AT MICROCOMPUTER BOARD TMS 9901
EN9901 LI   R12,TM9901     ADDRESS TMS 9901 ON MICROCOMPUTER BOARD
       SBZ  0              ENTER INTERRUPT MODE
       SBO  8              ENABLE INTERRUPT 8
       RET                 RETURN TO CALLING PROGRAM
       .
       .
       .

*SUBROUTINE TO ENABLE THE ISSUING OF AN  INTERRUPT FROM EACH TMS 9902
*WHEN A CHARACTER IS RECEIVED AT THE TMS 9902
ENINTS LI   R12,A9902      ADDRESS PORT A VIA CRU
       SBO  >12            ENABLE PORT A RECEIVER INTERRUPT ENABLE BIT
       SBO  >92            ENABLE PORT B RECEIVER INTERRUPT ENABLE BIT
       LI   R12,C9902      ADDRESS PORT C VIA CRU
       SBO  >12            ENABLE PORT C RECEIVER INTERRUPT ENABLE BIT
       SBO  >92            ENABLE PORT D RECEIVER INTERRUPT ENABLE BIT
       RET                 RETURN TO CALLING PROGRAM
       .
       .
```

FIGURE 3-10. EXAMPLE PROGRAM USING INTERRUPTS TO RECEIVE CHARACTERS
(Sheet 1 of 2, see next page)

3.3.8 Interrupt Operation.

Figure 3-10 uses interrupts to know if characters have been received at the TMS 9902s. Several factors must be considered in interrupt operations:

- Interrupt levels for each port must be specified at switches S1 to S4 (ports A to D respectively).
- Each port can have the same interrupt level if desired.
- Interrupt level must be enabled at microcomputer board's TMS 9901 and in the processor's interrupt mask before interrupt can be received.
- Four events can cause interrupts to be issued by the TMS 9902 as specified in the TMS 9902 data manual. These are:
  1) Receipt of a character (Receive Buffer Full)
  2) Character is transmitted (character shifted from Transmit Buffer Register to Transmit Shift Register).
  3) Timer counts down to zero
  4) DSR- or CTS- inputs change (data set change)

```
*INTERRUPT SERVICE ROUTINE
** DETERMINE WHICH OF THE FOUR PORTS ISSUED THE INTERRUPT
       CLR  FLAG          CLEAR FLAG REGISTER (R1)
PORTA  LI   R12,A9902     ADDRESS PORT A VIA CRU
       TB   >1F           DID PORT A ISSUE INTERRUPT?
       JEQ  GETCHR        YES, GET CHARACTER, FLAG = 0
       INC  FLAG          NO, SET FLAG TO ONE (INDICATE PORT B)
PORTB  TB   >9F           DID PORT B ISSUE INTERRUPT?
       JEQ  GETCHR        YES, GET CHARACTER, FLAG = 1
       INC  FLAG          NO, SET FLAG TO TWO (INDICATE PORT C)
PORTC  LI   R12,C9902     ADDRESS PORT C VIA CRU
       TB   >1F           DID PORT C ISSUE INTERRUPT?
       JEQ  GETCHR        YES, GET CHARACTER
PORTD  INC  FLAG          NO, SET FLAG TO THREE (INDICATE PORT D)
       TB   >9F           DID PORT D ISSUE INTERRUPT?
       JNE  ERROR8        NO, CHECK IF ERROR OCCURRED IN INT8
** PORT IDENTIFIED, PLACE CRU ADDRESS OF PORT IN R12
GETCHR LI   R12,A9902     SET CRU SOFTWARE BASE ADDRESS TO HEX 0200
       SLA  FLAG,7        MULTIPLY FLAG REGISTER CONTENTS BY HEX 80
       A    FLAG,R12      ADD FLAG VALUE TO R12 FOR CRU ADDRESS OF PORT
** CHECK FOR ERRORS, IF NONE, RECEIVE AND STORE CHARACTER
       TB   RBRL          IS CHARACTER IN RECEIVE BUFFER OF 9902?
       JNE  ERROR1        NO, CHARACTER NOT RECEIVED, CHECK FOR ERROR
       TB   RCVERR        ERROR OCCURRED IN CHARACTER RECEIPT?
       JEQ  ERROR2        YES, GO TO ERROR ROUTINE
       STCR R2,8          MOVE CHARACTER TO 8 MSBS OF R2
       SBO  RIENB         RE-ENABLE INTERRUPT FOR NEXT CHARACTER RECEIVED
       JMP  STORE         GO STORE CHARACTER RECEIVED IN PORT BUFFER AREA
       .
       .
       .
*STORE CHARACTER, CHECK CHARACTER, COMPARE FOR CONTROL CODE, ETC.
STORE  .
       .
       .
       RTWP
```

FIGURE 3-10. EXAMPLE PROGRAM USING INTERRUPTS TO RECEIVE CHARACTERS (Sheet 2 of 2)

As described in the TMS 9902 data manual, these interrupts must be enabled by writing a one to a bit on the TMS 9902. When enabled, an interrupt will be issued from the TMS 9902 (INT- low) to the interrupt level selected at eight-switch DIPs S1 to S4 (INT8- to INT15- for each port).

Figure 3-10 contains example code to use interrupts to receive characters at the four EIA ports. For interrupt map efficiency, all use interrupt level 8 (switches S1-1, S2-1, S3-1, and S4-1 set to ON; the others set to OFF). Sheet 1 of the figure contains code to enable interrupt level 8 at the TMS 9901 on the microcomputer board. To simplify the CRU map, the four ports are placed in four contiguous CRU software base addresses begining 0200_{16}. Displacements are used to set the interrupt enabling bits for character received at the four ports. Sheet 2 of Figure 3-9 is the interrupt service routine. Since it receives the same level interrupt from each port, it checks the contiguous CRU areas of each port to determine which port recived the character. Errors are checked for and the character is read at the TMS 9902 and stored.

SECTION 4

THEORY OF OPERATION

4.1 GENERAL

This section covers the theory of operation of the TM 990/307. The architecture is presented first followed by a description of the main sections of this module. Explanations will be keyed to schematic diagrams for maximum clarity.

Information in the following manuals can be used to supplement the material in this section:

- The TTL Data Book
- TMS 9902 Asynchronous Communications Controller Data Manual
- TMS 9903 Synchronous Communication Controller Data Manual
- Data Auxiliary Set 801C (Automatic Calling Unit) Interface Specification.

4.2 TM 990/307 ARCHITECTURE

The block diagram for the TM 990/307 is given in Figure 4-1. The main sections include the following: 1) system bus buffers, 2) ports A-D CRU base address select/decoding, 3) ports A-D secondary select signal decoding, 4) ports A-D I/O, and 5) ports A-D interrupt level selection. Each of these sections will be described in the sections that follow.

4.2.1 System Bus Buffers

The system bus buffer circuitry is shown in Figure 4-2. The 74LS244 (U6) and 74LS125 (U1) buffers provide non-inverted 3-state outputs while the 74LS240 (U5) buffers provide 3-state inverted outputs. This circuitry provides buffering for address lines A3.B through A14.B, MEMEN.B-, CRUOUT.B, CRUCLK.B-, IORST.B-, and REFCLK.B-. The address lines are used for selecting both the desired port and the output function.

The buffered value of IORST.B- (CLRCRU-) is used to reset the I/O ports. CRUOUT and CRUCLK are used for data output operations involving ports A-D and MEMEN.B- is used to avoid bus conflicts. The buffered value of REFCLK.B- (ϕ3-) is used by the I/O controller as a TTL clock.

4.2.2 Ports A-D CRU Base Address Select/Decode

The same circuitry is used to implement the CRU base address select/decode function for each port. Due to this similarity, it is necessary only to describe the circuitry for port A. The port CRU base address select/decode circuitry is given in Figure 4-3. The value on address lines A3- through A8- is compared with the CRU base address selected by the setting on switches S7-3 through S7-8 for port A (CRU base address selection is covered in Section 2.3.2). If the values are the same, a port select signal (SELA) is generated. SELA is used to develop another signal (ISELA-) that selects a specific port (Port A in this case) and also to prevent the selection of more than one port at a time. The select signals (SELA through SELD) that are generated by the

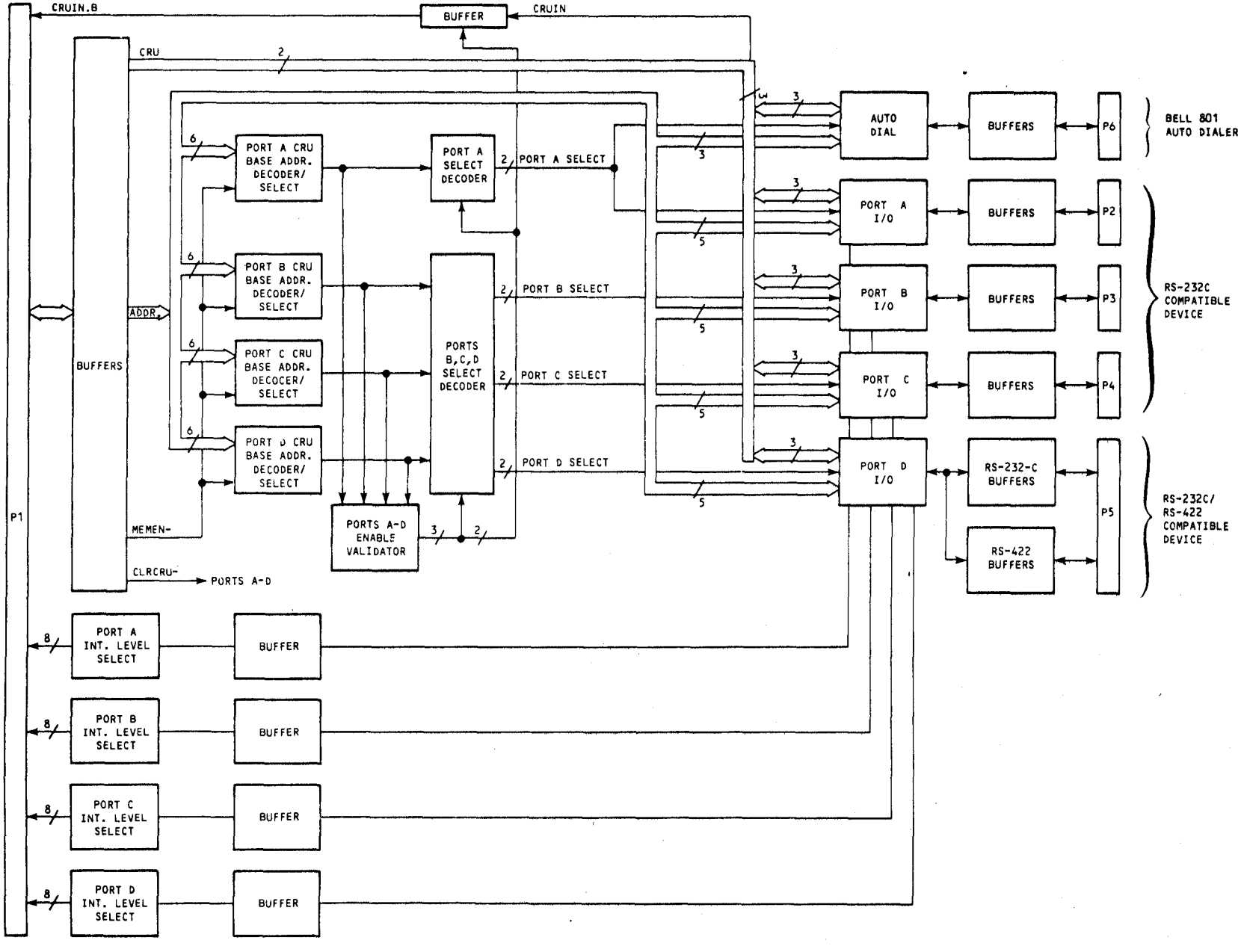


FIGURE 4-1. TM 990/307 BLOCK DIAGRAM

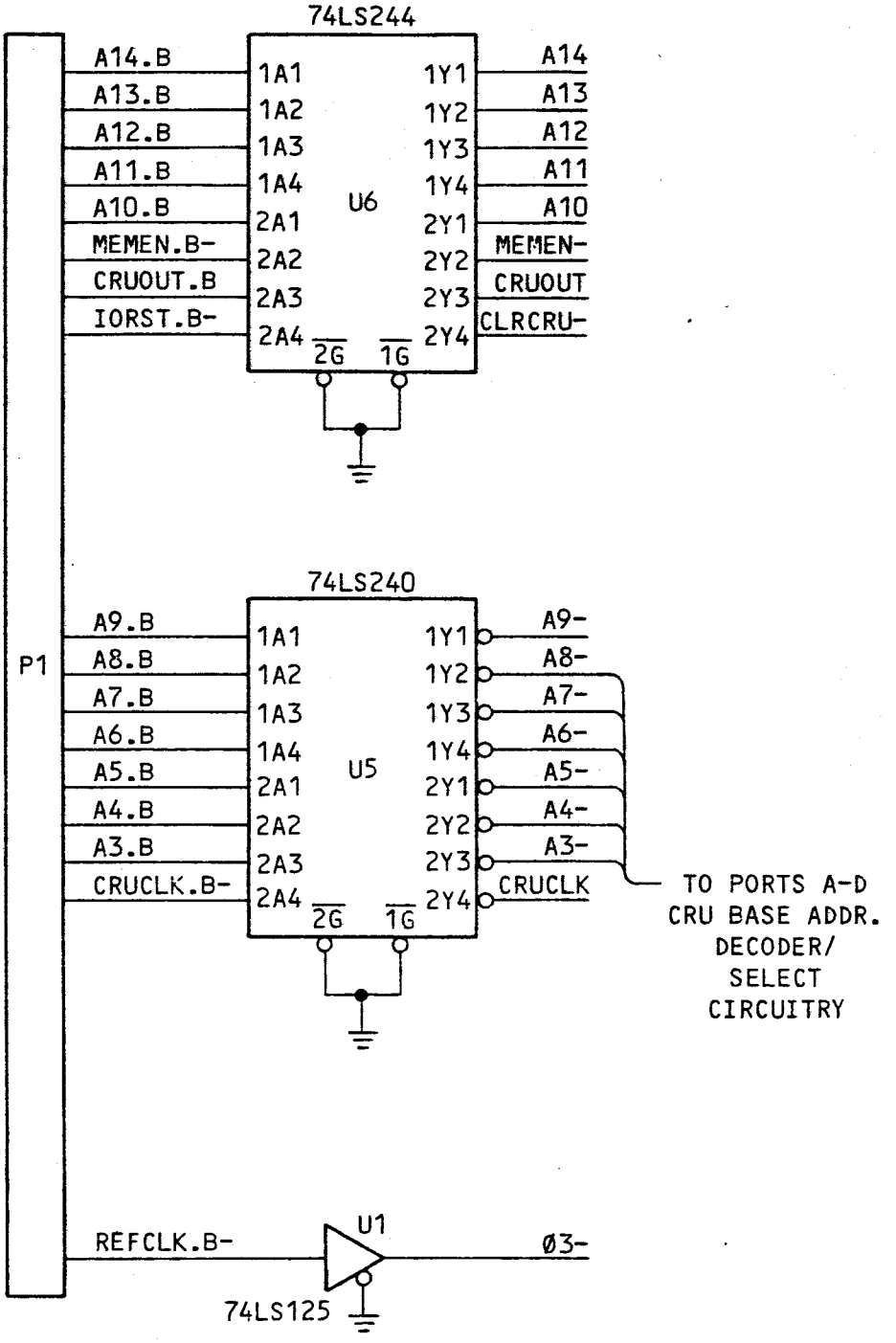


FIGURE 4-2. SYSTEM BUS BUFFERS

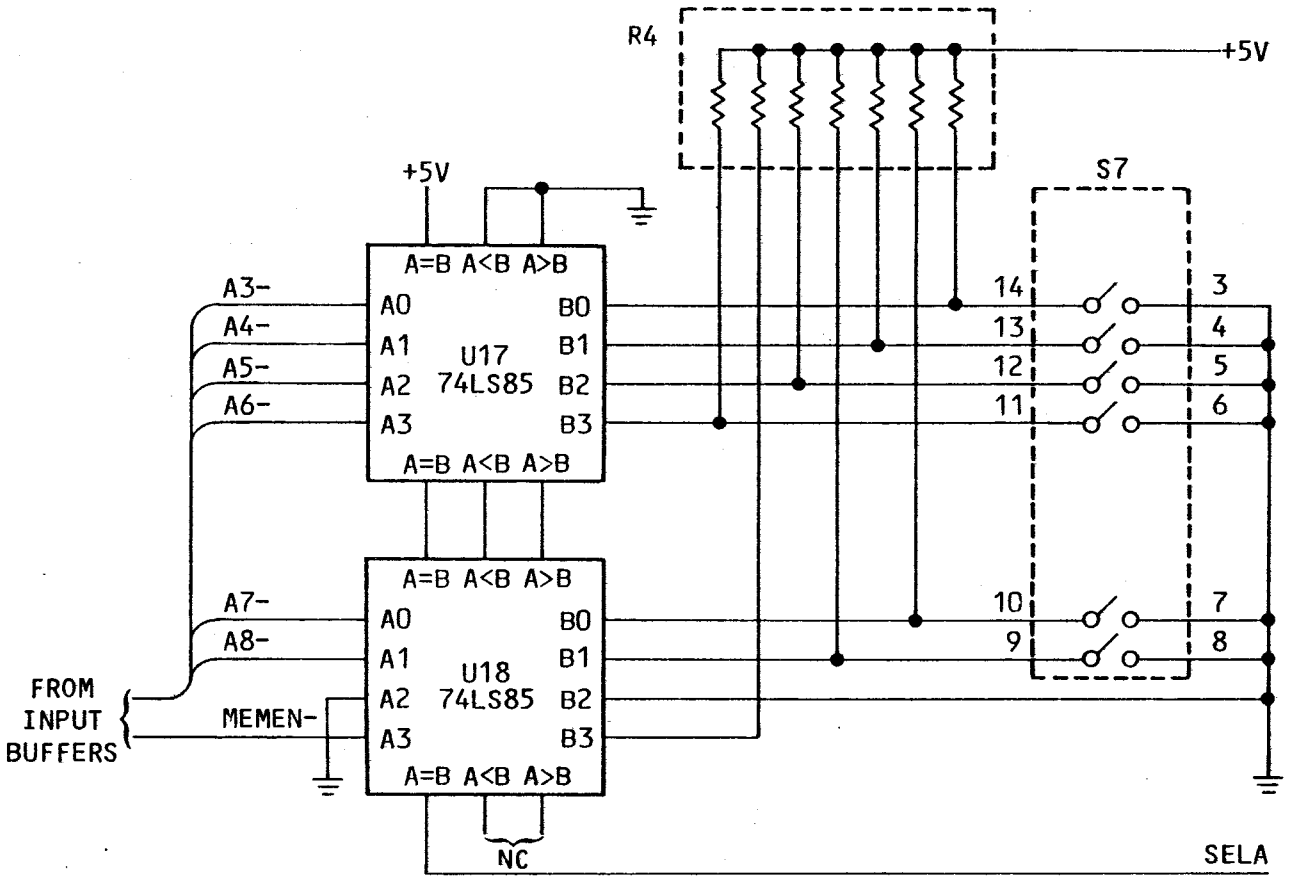


FIGURE 4-3. CRU BASE ADDRESS SELECT/DECODE

CRU address decoders will be referred to as primary port select signals; whereas signals (ISELA- through ISELD-) will be referred to as secondary port select signals. This distinction is important to the explanations that follow.

4.2.3 Ports A-D Select Decoding

Figure 4-4 shows the select decoding for ports A-D. This circuitry selects the I/O controller (TMS 9902 or TMS 9903) or other functions controlled by 74LS259 or 74LS251 devices. Table 4-1 lists the functions of the select signals generated by this circuitry.

TABLE 4-1. SECONDARY SELECT SIGNALS

SIGNAL	PORT	DESCRIPTION
9902A-	A	Select I/O controller (TMS 9902 or TMS 9903)
251A-	A	Select modem control signals/select data levels
259A-	A	Select port A LED/select modem control
9902B-	B	Select I/O controller (TMS 9902 or TMS 9903)
ISELB-	B	Select modem control/select data levels/select port B LED
9902C-	C	Select I/O controller (TMS 9902 or TMS 9903)
ISELC-	C	Select modem control/select data levels/select port C LED
9902D-	D	Select I/O controller (TMS 9902 or TMS 9903)
ISELD-	D	Select modem control/select data levels/select port D LED

The select signal decoding circuitry uses three sections to develop the secondary port select signals. These sections are the ports A-D enable validator (U10), the ports B, C, D secondary select signal decoder (U2 and U3), and the port A secondary select signal decoder (U9).

The first section involves the 74LS151 (U10). If any primary port select signal (SELA through SELD) is active (high), U10's Y output ENCRUIN will be active (high). This signal allows the 74LS10 NAND gates (U2 and U3) which comprise the ports B, C, D select signal decoder to develop active secondary port select signals depending on the status of their other inputs. Also, with any primary port select signal active, the U10's W output will be active (low) also. This signal gates on CRUIN buffer U1 and also 74LS139 port A secondary select signal decoder U9. If all primary select signals (SELA through SELD) are inactive (low), ENCRUIN will be low. This signal gates off the CRUIN buffer, holds the port B, C, D secondary select signal decoder (U2 and U3) outputs inactive (high), and gates off the port A secondary select signal decoder (U9).

The second section of the select signal decoding circuitry involves the ports B, C, D secondary port select signal decoder (U2 and U3). This decoder uses 3-input NAND gates to develop the proper select signals. All three inputs to these gates must be high in order for the gate to develop an active (low) output signal. If any port (A through D) is addressed, the ports A-D CRU base address select/decode circuitry will provide an active primary port select signal (SELA-SELD). The ports A-D enable validator (U10) produces an active ENCRUIN signal to the NAND gates. The second active signal for these gates will be SELB, SELC, or SELD depending on the port that was addressed. The final input (A9-) will determine whether the TMS 9902 I/O controller/modem control or data levels/port LED functions will be selected. When signal A9- is high, the selected port's 9902 select line will be activated. When A9- is low, ISELB-, ISELC-, or ISELD- signals will be activated allowing the user to read from the pre-set data switches or to activate the port's LED.

The third section of the select signal decoding circuitry involves U9. This section is used to provide control signals that are used for the auto dialer, the I/O controller, the readable data levels, and the port's LED indicator. If SELA is inactive (low), all of U10's select output signals will be inactive

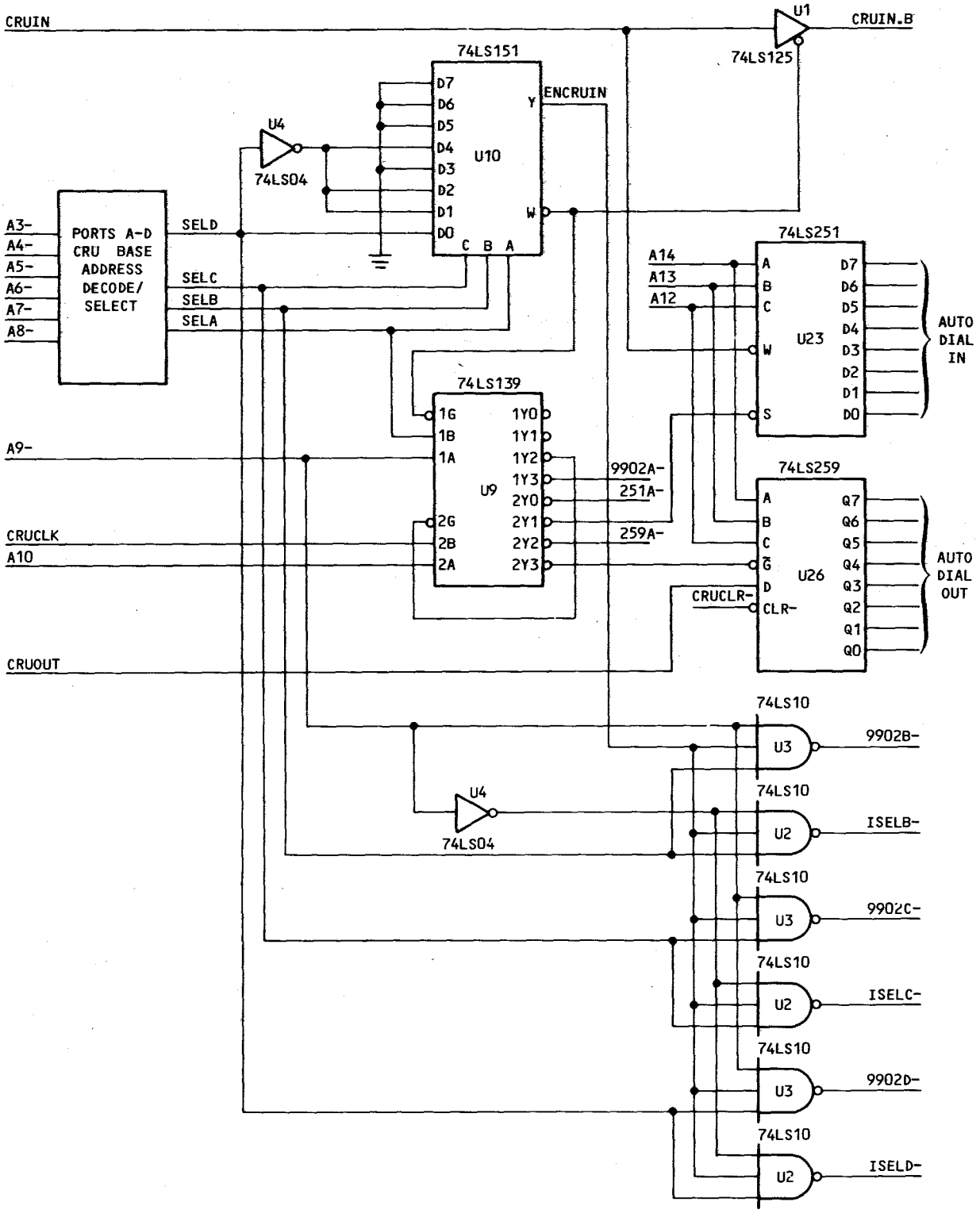


FIGURE 4-4. PORTS A-D SELECT DECODING

(high). When SELA is active (high), U10's select signal output depends on the logic level on A9-. When A9- is low, 1Y2 will be active (low). The signal from 1Y2 gates on the lower section of the U9 which provides secondary select signals depending on the logic levels of CRUCLK and A10. When both CRUCLK and A10 are high, output 2Y3 will be active (low) and gate on 8-bit addressable latch 74LS259 (U26) which is used for auto dial output operations. With A10 high but CRUCLK low, output 2Y1 will be active (low) and gate on data selector/multiplexer 74LS251 (U23) which is used for auto dial input operations. With A10 low, the output select signal depends on the level of CRUCLK. When CRUCLK is low, output 2Y0 is active thus selecting the modem control and data levels. When CRUCLK is high, output 2Y2 is active thus selecting the port A LED or output control signals. When A9- is high, 1Y3 will be active (low), thus selecting port A's TMS 9902 I/O controller.

4.2.4 Ports A-D I/O

Port A differs from the other ports in that it includes the auto dialer interface. Ports B, C, and D are the same with exception that port D provides buffer interfaces for both RS-232-C and RS-422 compatible devices.

4.2.4.1 Port A I/O. The port A I/O circuitry is shown in Figure 4-5. It essentially consists of an I/O controller (TMS 9902 or TMS 9903), an addressable latch (74LS259 for writing to an LED and the modem DTR control), a data selector/multiplexer (74LS251 for selecting switch controlled data levels and providing modem control signals), and RS-232-C line buffers. The auto dialer interface that is affiliated with port A is described in Section 4.2.4.2.

The TMS 9902 I/O controller interfaces to the TM 990/10X CPU module via the communications register unit (CRU). The CRU interface consists of five address select lines (S0-S4), chip enable (CE-), and three CRU lines (CRUIN, CRUOUT, and CRUCLK). An additional input to the CPU module is the TMS 9902's interrupt line (INT-). The TMS 9902 occupies 32 bits of CRU space; each of the 32 bits are selected individually by processor address lines A10-A14 which are connected to the TMS 9902's select lines (S0-S4), respectively. The chip enable (CE-) signal comes from the port A select decoding circuitry previously described. The CRU input and output bit functions are given in The TMS 9902 Asynchronous Communications Controller Data Manual.

The 74LS259 eight-bit addressable latch (U24) is used to drive the port A LED (DS1): it also controls the modem DTR signal. This LED can be addressed and selected for test/evaluation purposes.

The 74LS251 data selector/multiplexer (U37) serves two purposes: (1) it provides a means where logic levels can be inserted for test/evaluation purposes, and (2) it provides the communications link between the CPU module and modem control signals. Modem control signal DSR- (data set ready) and RI- (receive input) when addressed and selected are fed to the CPU module via CRUIN.

4.2.4.2 Auto Dial Interface. The auto dial interface is shown in Figure 4-6. This interface is selected by signals from the port A secondary select signal decoder U9. These signals control auto dial input/output operations. The 74LS259 (U26) is used for auto dial output operations while the 74LS251 (U23) is used for auto dial input operations. The CPU module's IORST- signal after being buffered (CLRCRU-) is used to reset the 74LS259 latch. The auto dial input data selector (U23) provides serial input via its W output (CRUIN). This

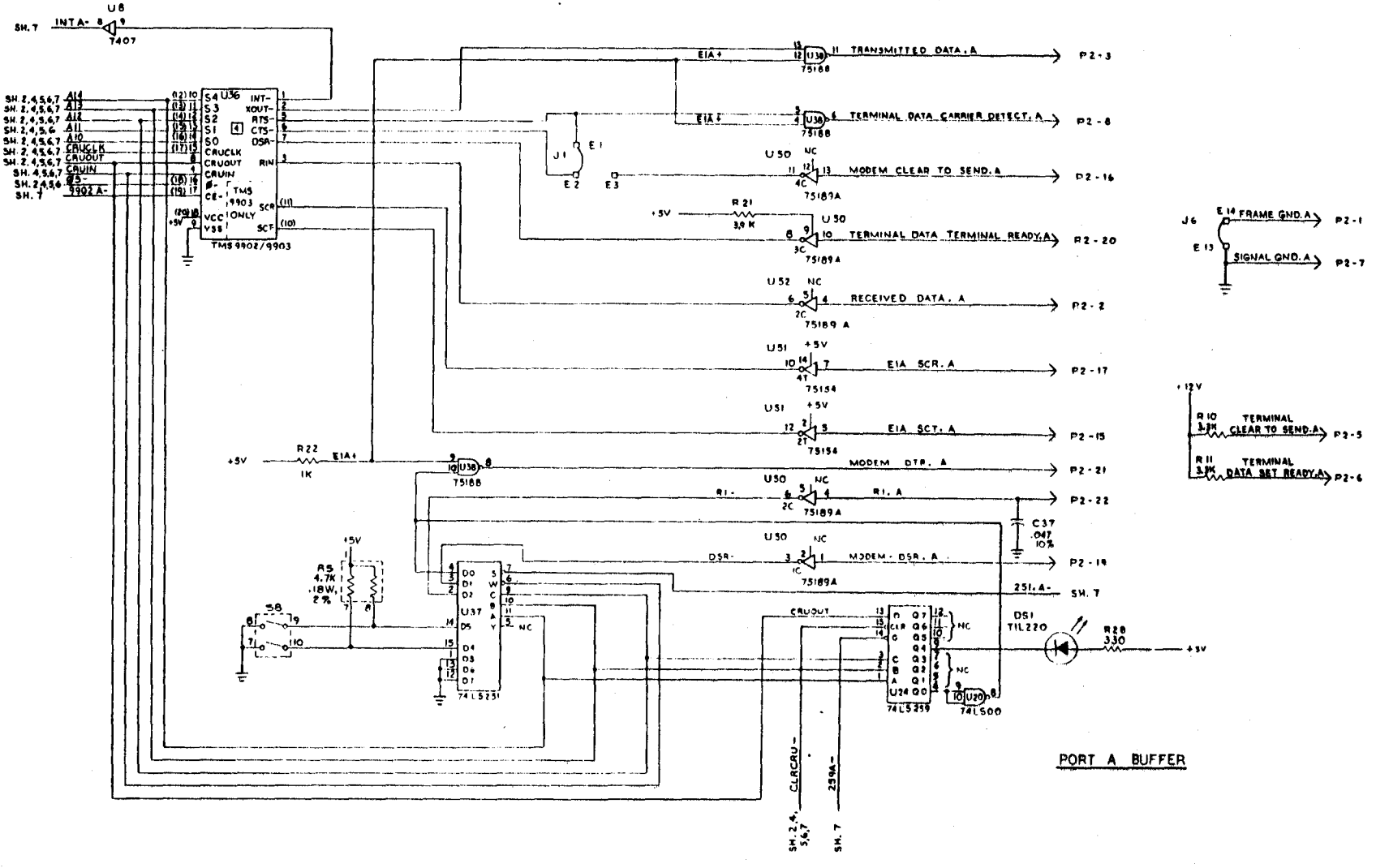


FIGURE 4-5. PORT A INPUT/OUTPUT CIRCUITRY

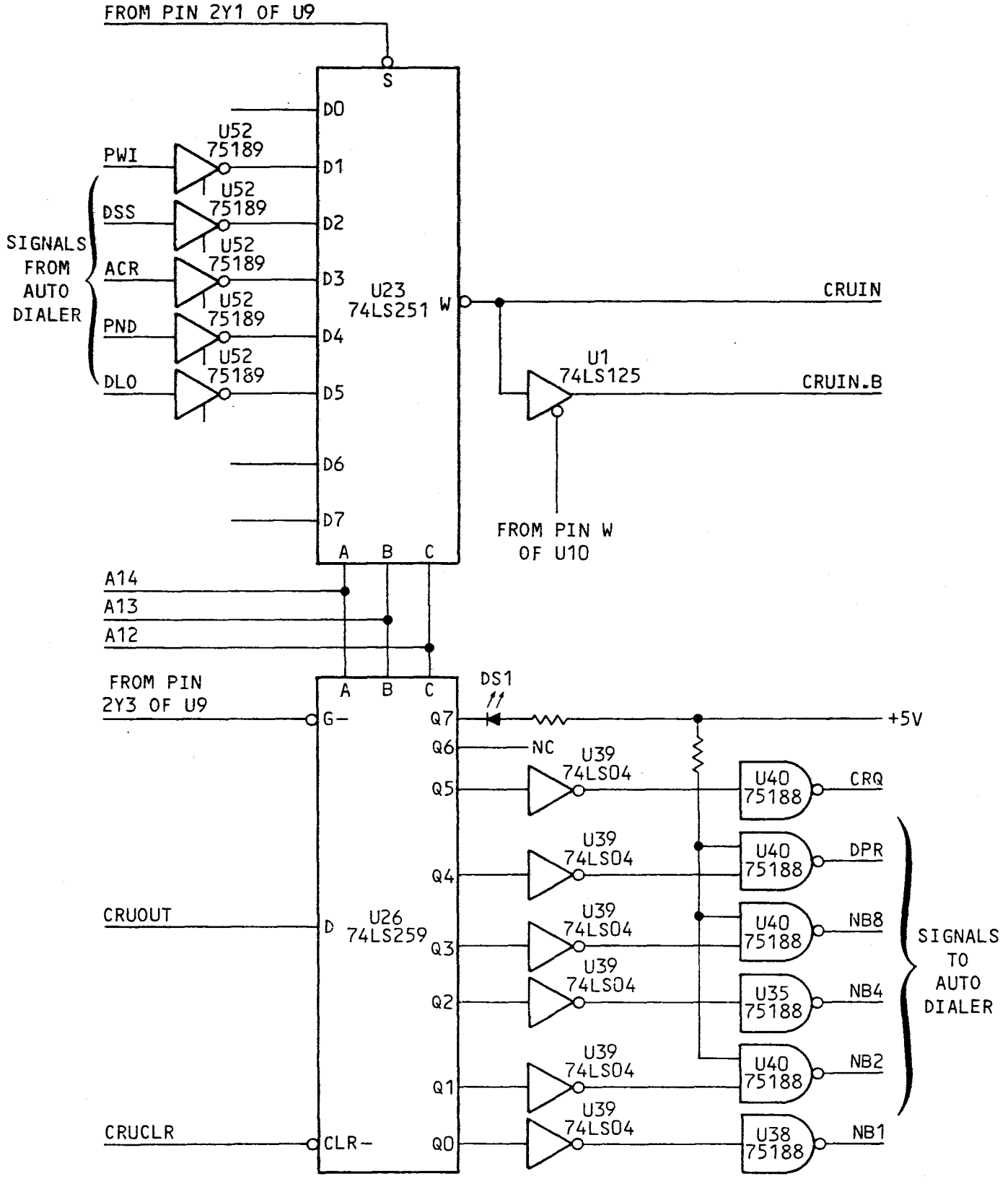


FIGURE 4-6. AUTO DIAL INTERFACE

output is buffered (CRUIN.B) prior to being coupled to the CPU module.

Auto dial input and output signals are also buffered. Auto dial input signals (DLO, PND, ACR, DSS, and PWI are inverted by 75189's and then fed to 74LS251 data selector/multiplexer (U23). U23's W output is buffered by U1 and then fed to the CPU module via the TM 990 system bus. Auto dial output signals (QCRQ, QDPR, QNB8, QNB4, QNB2, and QNB1) are inverted then fed to 75188 gates prior to being coupled to the auto dialer as signals CRQ, DPR, NB8, NB4, NB2, and NB1. A description of auto dial signals and their function can be found in the Data Auxiliary Set 801C (Automatic Calling Unit) Interface Specification from American Telephone and Telegraph Company.

4.2.4.3 Ports B, C, D I/O. The port B, C, D I/O circuitry is similar to port A with the following exceptions: (1) ports B, C, and D have no auto dialer interface (only port A has this interface), (2) signals ISELB-, ISELC-, and ISELD- select both the LED and modem control signals/data levels (port A has select signals for input/output auto dialer operations and separate signals for LED and modem control/data levels).

Port D differs from ports B and C in that it provides both RS-232-C and RS-422 buffers whereas ports B and C provide only RS-232-C buffers. Port D I/O circuitry with both RS-232-C and RS-422 buffers is shown in Figure 4-7.

The RS-422 interface uses a DS3486 line receiver (U42) and a DS3487 tri-state line driver (U46). Three jumpers are provided so that the RS-422 lines may be terminated by 100 ohm resistors if required. To terminate the RS-422 lines, connect jumpers from E22 to E23, E25 to E26, and E28 to E29.

Ports A through D can use either a TMS 9902 asynchronous communications controller or a TMS 9903 synchronous communications controller. If a TMS 9903 is used in port D, then the RS-422 interface must be used.

4.2.5 Ports A-D Interrupt Level Selection

The circuitry that is used for interrupt level selection is the same for all four ports. Due to this fact, only the interrupt level selection circuitry for port A will be described. The circuitry for port A is given in Figure 4-8. The TMS 9902's interrupt line (INT-) is buffered then fed to switch S1 for interrupt level selection. Interrupt levels INT8- through INT15- can be selected by the use of this switch.

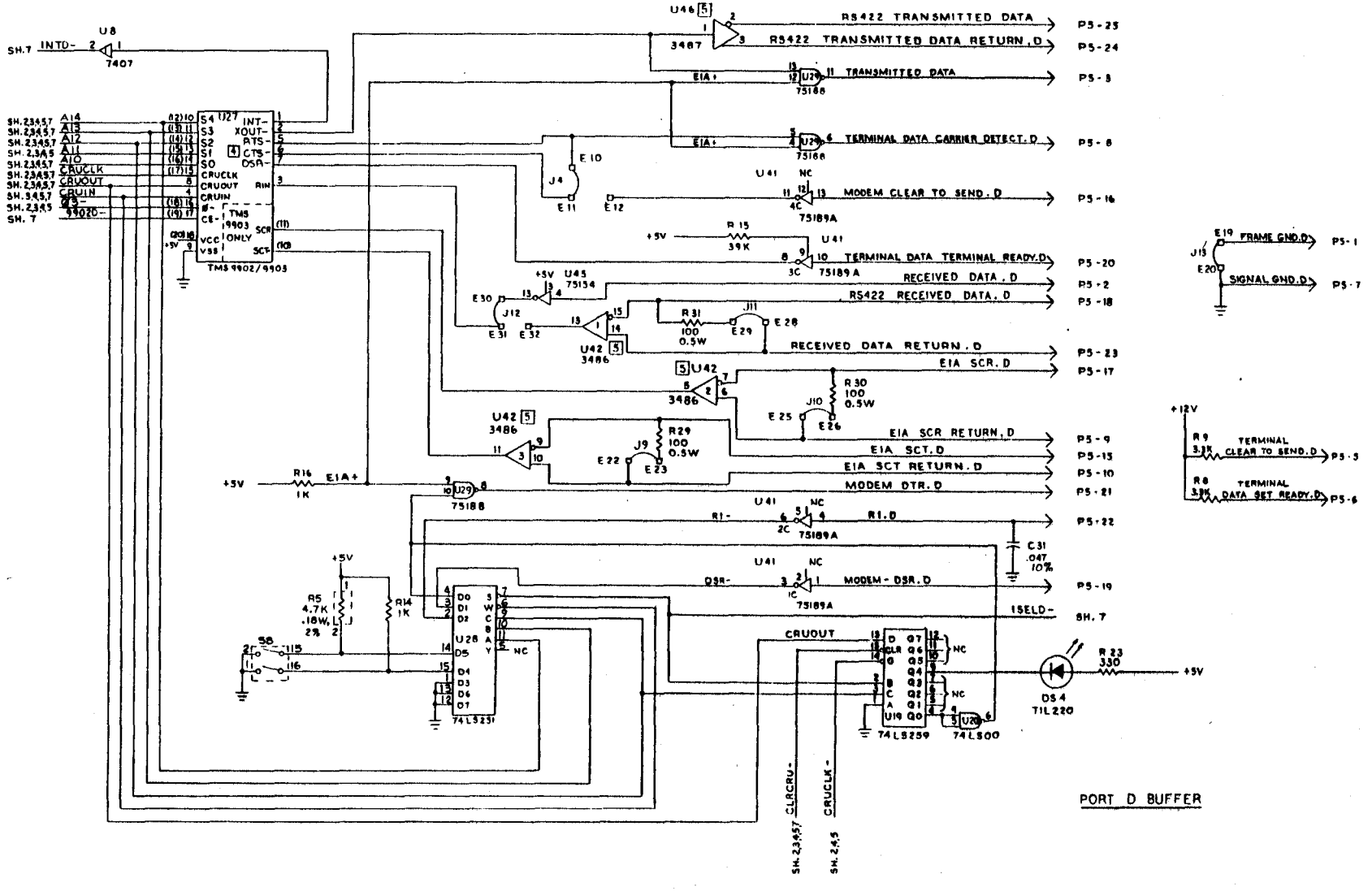


FIGURE 4-7. PORT D INPUT/OUTPUT CIRCUITRY

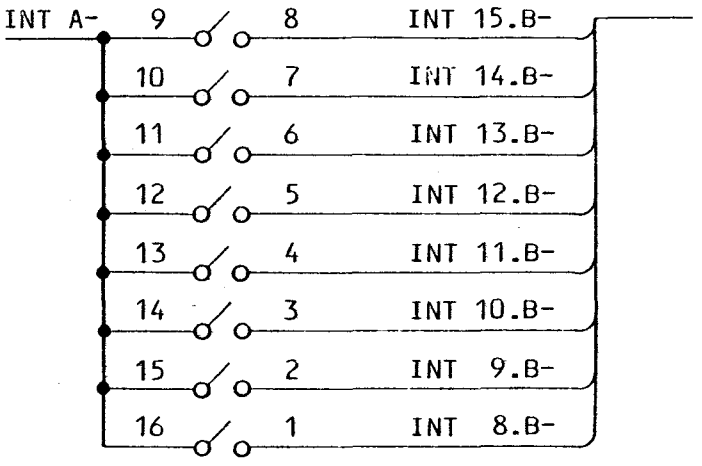


FIGURE 4-8. INTERRUPT LEVEL SELECTION

APPENDIX A

SCHEMATICS

PART NO. 1600165 REV. 1

REVISIONS

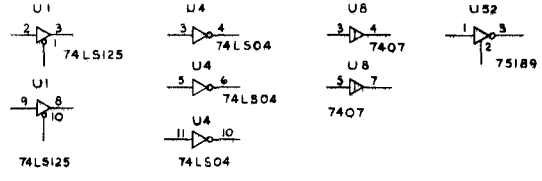
REV	DESCRIPTION	DATE	APPROVED
A	CN 148629 INF A. Thompson 2-13-80	2/14/80	

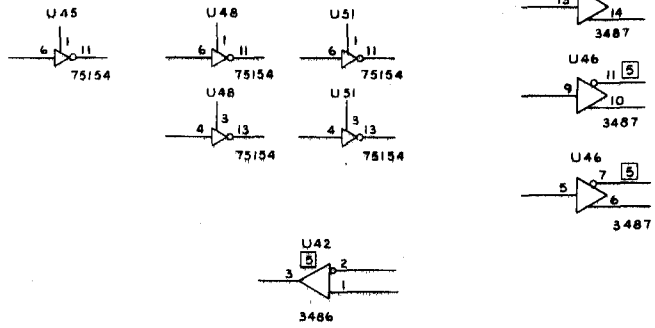
NOTES UNLESS OTHERWISE SPECIFIED

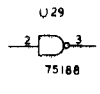
1. CAPACITANCE VALUES ARE IN MICROFARADS
2. RESISTANCE VALUES ARE IN OHMS
3. ALL RESISTOR ARE .25W, 5%
4. PIN NUMBERS IN PARENTHESIS AT LOCATIONS U27, U30, U33 & U36 ARE FOR ALTERNATE DEVICE /9903 ONLY
5. USER'S OPTION

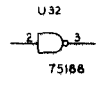
REFERENCE DESIGNATORS	
USED	NOT USED
C1 - C39	
DS1 - DS5	
E1 - E34	E21, E24, E27
J1 - J13	
P1 - P6	
R1 - R31	
S1 - S8	
U1 - U52	U7, U43

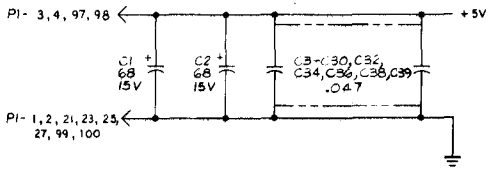
SPARES











SEQ NO.	IDENT	F.SPEC	NO	ADDITIONAL	NOTES
	PROCESS			CLASSIFICATION	

PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS SEE TI DRAWING 729487

1600167	8117
1600168	8117
NEXT ASSY	USED ON
APPLICATION	

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

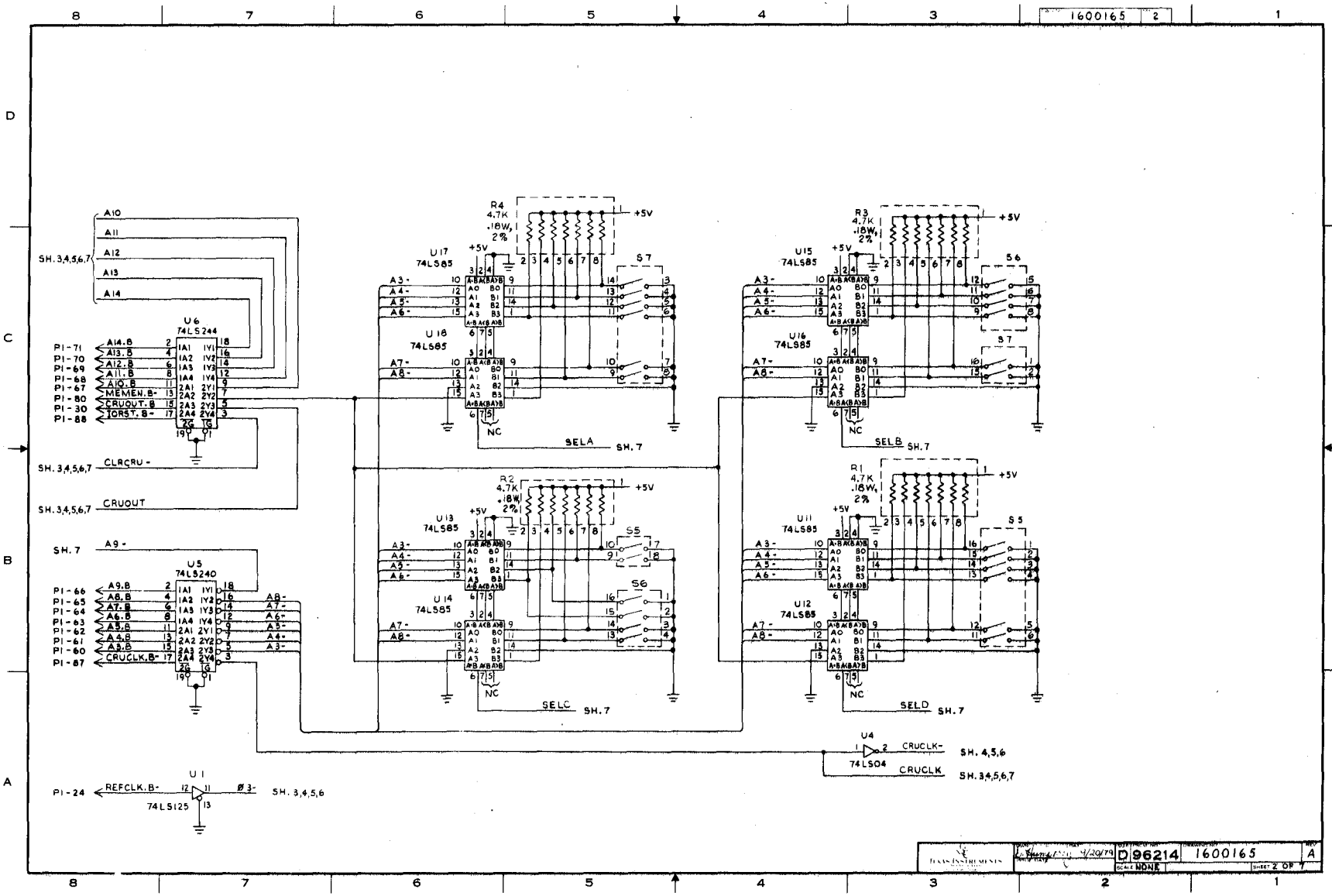
DRAWN	CHECKED	ENGR	MFG	QUAL

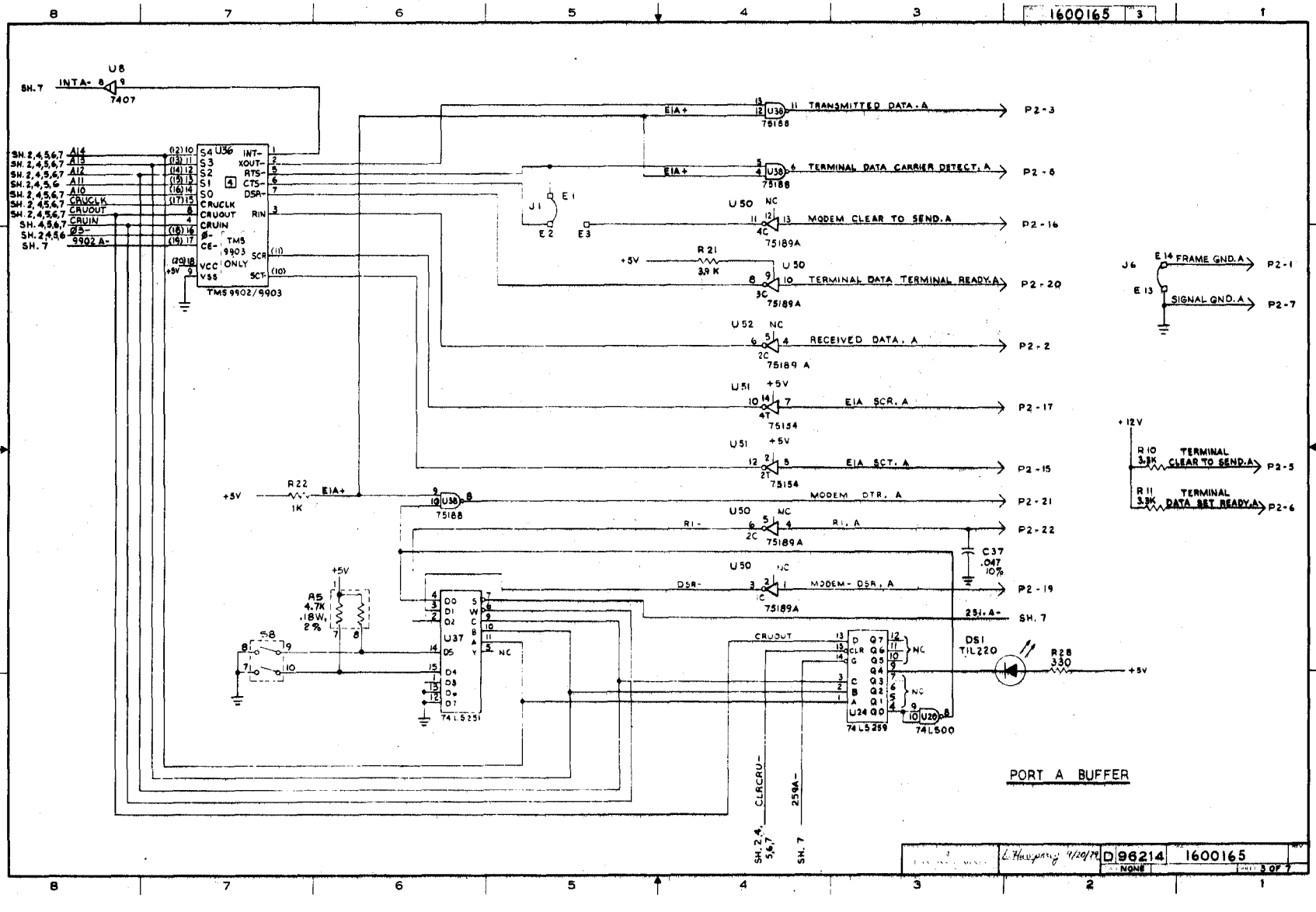
TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

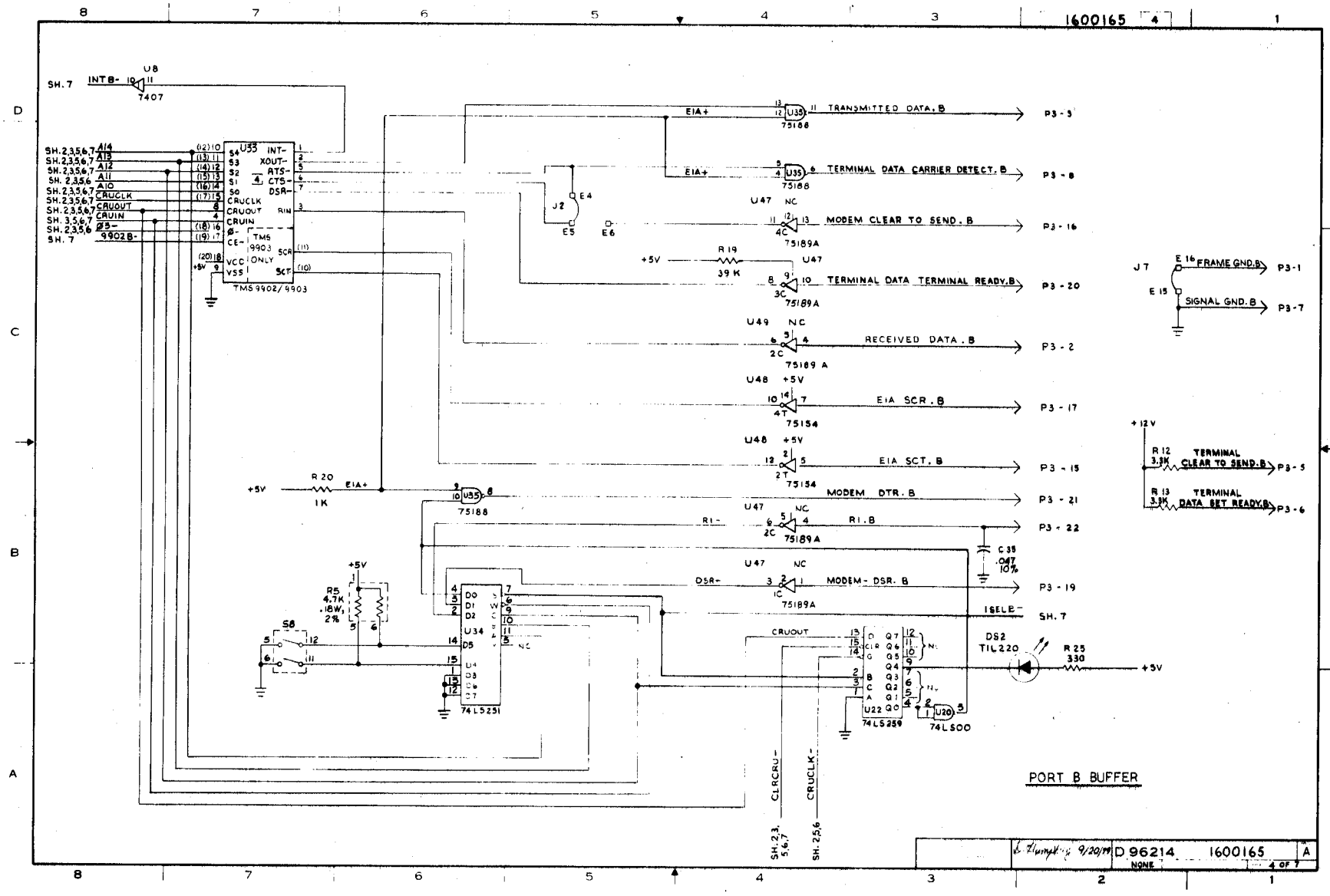
DIAGRAM, LOGIC
TM 990/307

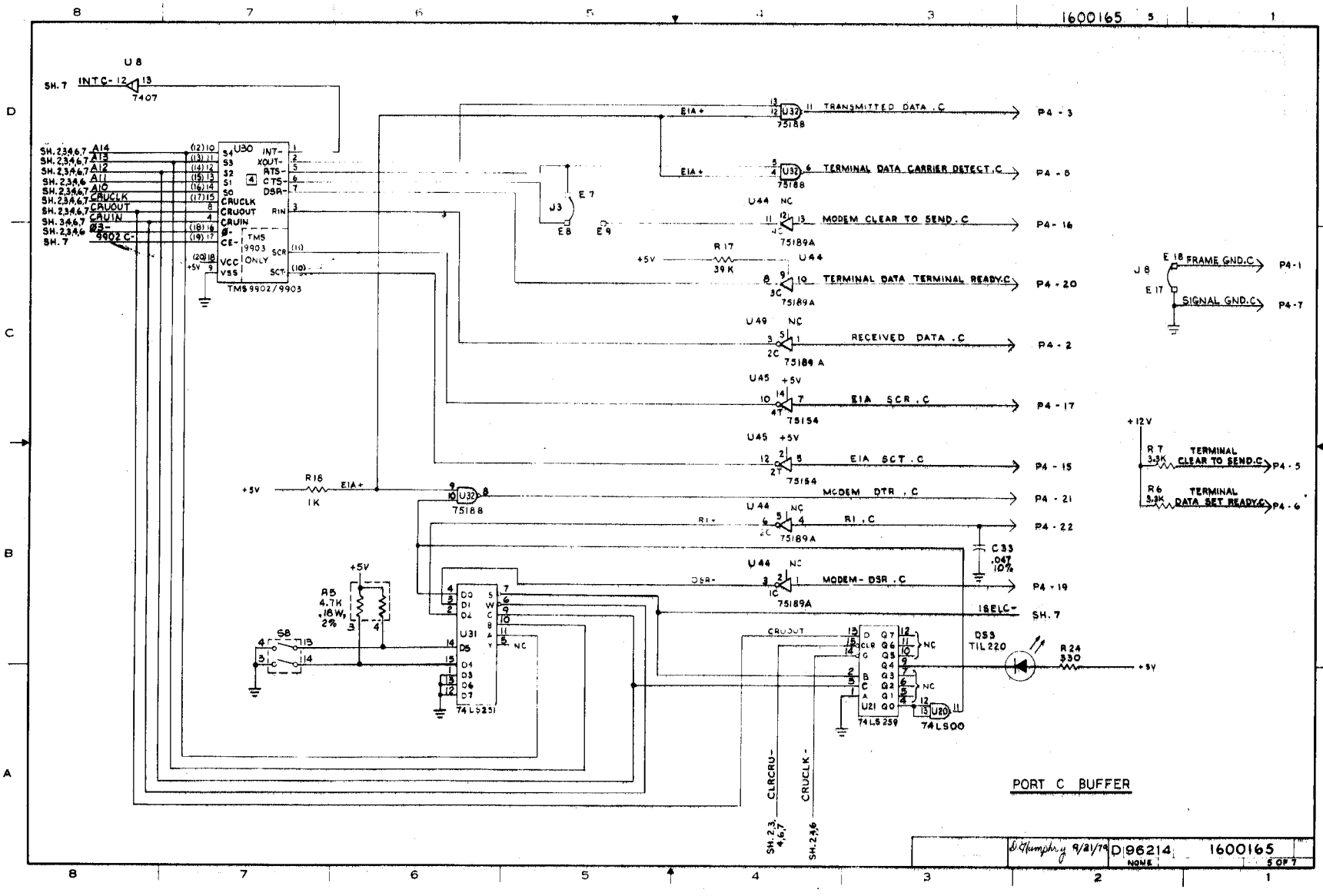
SIZE D | FSCM NO. 96214 | DRAWING NO. 1600165

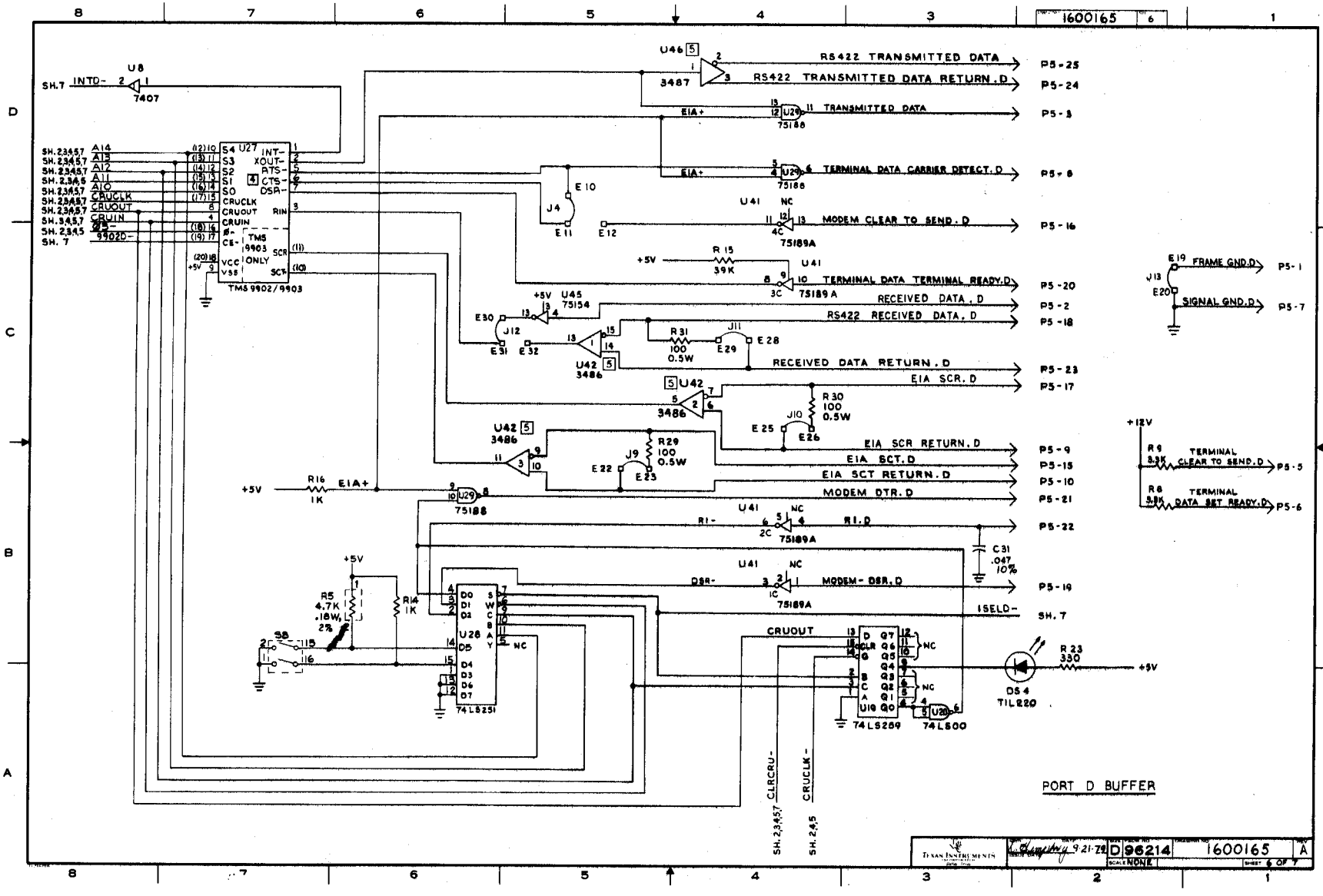
SCALE NONE | SHEET 1 OF 7

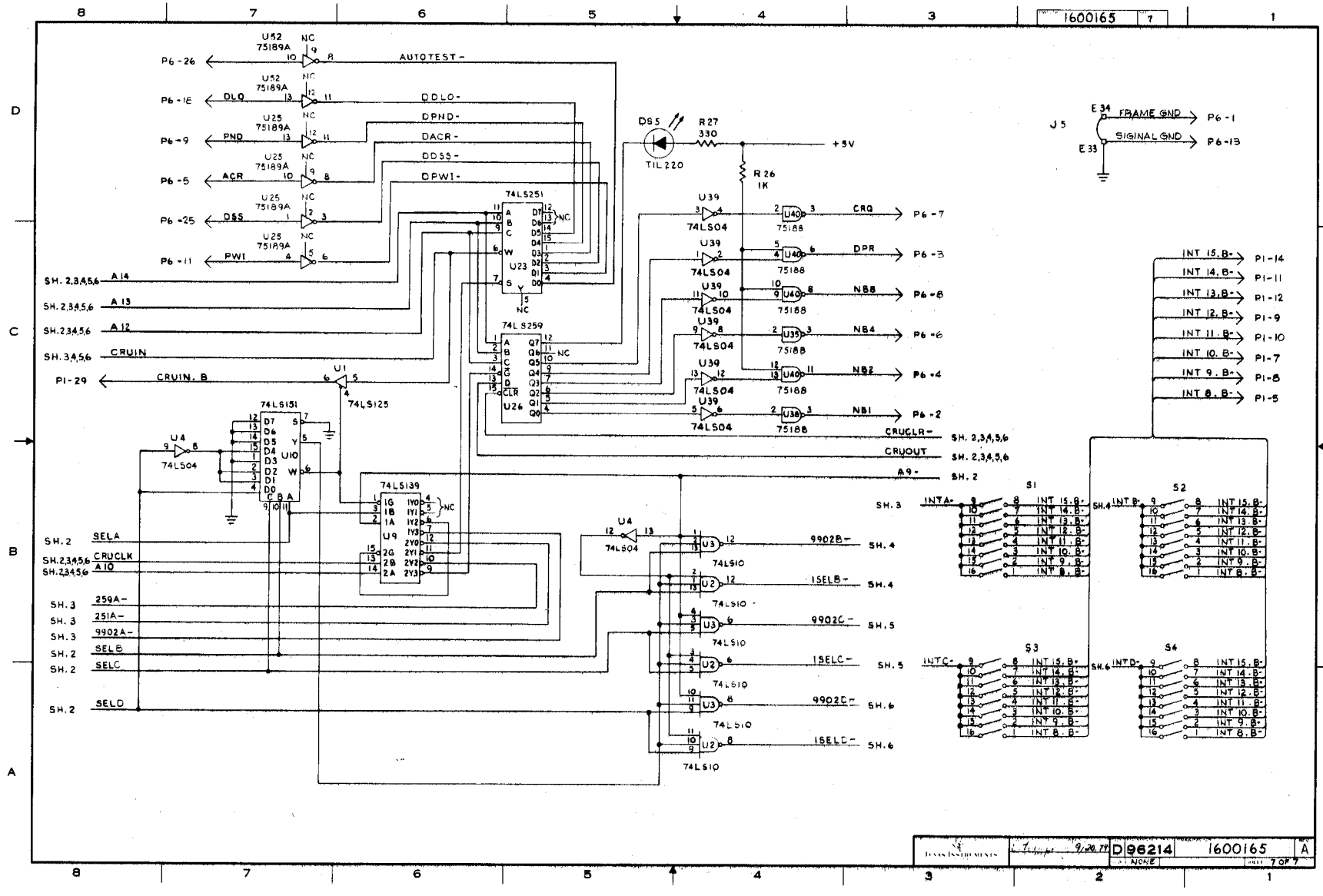

1600165 2
A10
A11
A12
A13
A14
SH. 3,4,5,6,7
U6
74LS244
P1-71
P1-70
P1-69
P1-68
P1-67
P1-80
P1-30
P1-88
A14.B
A13.B
A12.B
A11.B
A10.B
MEMEN.B-
CRUOUT.B
IORST.B-
SH. 3,4,5,6,7 CLRCRU-
SH. 3,4,5,6,7 CRUOUT
SH. 7 A9-
U5
74LS240
P1-66
P1-65
P1-64
P1-63
P1-62
P1-61
P1-60
P1-87
A9.B
A8.B
A7.B
A6.B
A5.B
A4.B
A3.B
CRUCLK.B-
A8-
A7-
A6-
A5-
A4-
A3-
U1
74LS125
P1-24 REFCLK.B-
Ø3-
SH. 3,4,5,6
R4
4.7K
.18W,
2%
+5V
U17
74LS685
A3-
A4-
A5-
A6-
S7
U18
74LS685
A7-
A8-
NC
SELA SH. 7
R3
4.7K
.18W,
2%
U15
74LS685
S6
U16
74LS685
SELB SH. 7
R2
4.7K
.18W,
2%
U13
74LS685
S5
U14
74LS685
S6
SELC SH. 7
R1
4.7K
.18W,
2%
U11
74LS685
S5
U12
74LS685
SELD SH. 7
U4
74LS04
CRUCLK-
SH. 4,5,6
CRUCLK
SH. 3,4,5,6,7
TEXAS INSTRUMENTS
D 96214
1600165
A
SCALE NONE
SHEET 2 OF 7
A-3


1600165
U8
7407
INTA-
TMS 9902/9903
TRANSMITTED DATA, A
TERMINAL DATA CARRIER DETECT, A
MODEM CLEAR TO SEND, A
TERMINAL DATA TERMINAL READY, A
RECEIVED DATA, A
EIA SCR, A
EIA SCT, A
MODEM DTR, A
RI, A
MODEM- DSR, A
FRAME GND, A
SIGNAL GND, A
TERMINAL CLEAR TO SEND, A
TERMINAL DATA SET READY, A
PORT A BUFFER
CRUOUT
CLKCRU-
259A-
D96214
1600165


1600165
U8
SH. 7
INT8-
7407
U33
TMS 9902/9903
TMS 9903 ONLY
SH. 2,3,5,6,7 A14
SH. 2,3,5,6,7 A13
SH. 2,3,5,6,7 A12
SH. 2,3,5,6,7 A11
SH. 2,3,5,6 A10
SH. 2,3,5,6,7 CRUCLK
SH. 2,3,5,6,7 CRUOUT
SH. 2,3,5,6,7 CRUIN
SH. 3,5,6,7 Ø5-
SH. 2,3,5,6 Ø-
SH. 7 9902B-
INT-
XOUT-
RTS-
CTS-
DSR-
SCR
SCT
RIN
EIA+
TRANSMITTED DATA. B
P3 - 3
TERMINAL DATA CARRIER DETECT. B
P3 - 8
MODEM CLEAR TO SEND. B
P3 - 16
TERMINAL DATA TERMINAL READY. B
P3 - 20
RECEIVED DATA. B
P3 - 2
EIA SCR. B
P3 - 17
EIA SCT. B
P3 - 15
MODEM DTR. B
P3 - 21
RI. B
P3 - 22
MODEM- DSR. B
P3 - 19
ISELE-
SH. 7
J2
E4
E5
E6
J7
E16
FRAME GND. B
P3-1
E15
SIGNAL GND. B
P3-7
+5V
+12V
R19
39 K
R20
1K
R5
4.7K
.18W, 1%
S8
U34
74LS251
U22
74LS259
U20
74LS00
DS2
TIL220
R25
330
C35
.047
10%
R12
3.3K
TERMINAL CLEAR TO SEND. B
P3-5
R13
3.3K
TERMINAL DATA SET READY. B
P3-6
CRUOUT
CLRCRU-
CRUCLK-
SH. 2,3, 5,6,7
SH. 2,5,6
PORT B BUFFER
D 96214
1600165
A
NONE
4 OF 7


1600165
U8
SH. 7 INTC- 12 13
7407
SH. 2,3,4,6,7 A14
SH. 2,3,4,6,7 A13
SH. 2,3,4,6,7 A12
SH. 2,3,4,6 A11
SH. 2,3,4,6 A10
SH. 2,3,4,6,7 CRUCLK
SH. 2,3,4,6,7 CRUOUT
SH. 2,3,4,6,7 CRUIN
SH. 3,4,6,7 Ø3-
SH. 2,3,4,6 9902 C-
SH. 7
U30
TMS 9903 ONLY
TMS 9902/9903
INT-
XOUT-
RTS-
CTS-
DSR-
CRUCLK
CRUOUT
CRUIN
RIN
SCR
SCT
VCC
VSS
+5V
EIA+
U32
75188
TRANSMITTED DATA .C
P4 - 3
TERMINAL DATA CARRIER DETECT.C
P4 - 8
MODEM CLEAR TO SEND. C
P4 - 16
TERMINAL DATA TERMINAL READY.C
P4 - 20
RECEIVED DATA .C
P4 - 2
EIA SCR .C
P4 - 17
EIA SCT .C
P4 - 15
MODEM DTR .C
P4 - 21
RI .C
P4 - 22
MODEM- DSR .C
P4 - 19
!SELC-
SH. 7
J3
E7
E8
E9
R17
39K
U44
U49
U45
75189A
75154
C33
.047
10%
R18
1K
R1-
DSR-
U31
74LS251
S8
R5
4.7K
.18W,
2%
CRUOUT
U21
74LS259
U20
74LS00
DS3
TIL 220
R24
330
E18 FRAME GND.C
P4-1
E17 SIGNAL GND.C
P4-7
+12V
R7
3.3K
TERMINAL CLEAR TO SEND.C
P4-5
R6
3.3K
TERMINAL DATA SET READY.C
P4-6
CLRCRU-
CRUCLK-
SH. 2,3, 4,6,7
SH. 2,3,6
PORT C BUFFER
B Humphry 9/21/79
D 96214
1600165
NONE
5 OF 7


1600165
U8
7407
INTD-
SH.7
U27
TMS 9902/9903
TMS 9903 ONLY
U46
3487
RS422 TRANSMITTED DATA
RS422 TRANSMITTED DATA RETURN.D
TRANSMITTED DATA
TERMINAL DATA CARRIER DETECT.D
MODEM CLEAR TO SEND.D
TERMINAL DATA TERMINAL READY.D
RECEIVED DATA.D
RS422 RECEIVED DATA.D
RECEIVED DATA RETURN.D
EIA SCR.D
EIA SCR RETURN.D
EIA SCT.D
EIA SCT RETURN.D
MODEM DTR.D
RI.D
MODEM-DSR.D
ISELD-
CRUOUT
PORT D BUFFER
FRAME GND.D
SIGNAL GND.D
TERMINAL CLEAR TO SEND.D
TERMINAL DATA SET READY.D
DS4
TIL220
74LS251
74LS259
74LS00
CLRCRU-
CRUCLK-
A-7


1600165
U52 75189A
P6-26
AUTOTEST-
P6-18
DLO
DDLO-
U25 75189A
P6-9
PND
DPND-
P6-5
ACR
DACR-
P6-25
DSS
DDSS-
P6-11
PWI
DPWI-
74LS251
U23
74LS259
U26
D85
TIL220
R27
330
+5V
R26
1K
J5
E34
FRAME GND
P6-1
E33
SIGNAL GND
P6-13
U39
74LS04
U40
75188
U38
CRQ
P6-7
DPR
P6-3
NBB
P6-8
NB4
P6-6
NB2
P6-4
NB1
P6-2
CRUCLR-
CRUOUT
A9-
INT 15.B-
INT 14.B-
INT 13.B-
INT 12.B-
INT 11.B-
INT 10.B-
INT 9.B-
INT 8.B-
P1-14
P1-11
P1-12
P1-9
P1-10
P1-7
P1-8
P1-5
S1
S2
S3
S4
INTA-
INTB-
INTC-
INTD-
U1
74LS125
U4
74LS04
U10
74LS151
U9
74LS139
U2
U3
74LS10
A14
A13
A12
CRUIN
CRUIN.B
SELA
CRUCLK
A10
259A-
251A-
9902A-
SELB
SELC
SELD
9902B-
1SELB-
9902C-
1SELC-
9902D-
1SELD-
SH. 2,3,4,5,6
SH. 2
SH. 3
SH. 4
SH. 5
SH. 6
D 96214
1600165
A
NONE
7 OF 7

A-8

APPENDIX B

PARTS LIST

Symbol	Description
C1, C2	Capacitor, tantalum, 68 uF, 15 V
C3-C30, C32, C34 C36, C38, C39	Capacitor, 0.047 uF
C31, C33, C35, C37	Capacitor, 0.047 uF, ±10%
DS1-DS4	Diode, LED, TIL 220
DS5	Diode, LED, right angle
E1-E20, E22, E23 E25, E26, E28-E34	0.025 in. square pins
J1-J13	Jumper plug Mfr. by: Berg Electronics, Inc. Rt. 3 New Cumberland, Pa. 17070 P/N 65474-005
R1-R5	Resistor, 4.7 kilohms, 8-pin SIP, 0.18 W, ±2%
R6-R13	Resistor, 3.3 kilohms, 1/4 W, ±5%
R14, R16, R18, R20 R22, R26	Resistor, 1 kilohm, 1/4 W, ±5%
R15, R17, R19, R21	Resistor, 3.9 kilohms, 1/4 W, ±5%
R23-R25, R27, R28	Resistor, 330 ohms, 1/4 W, ±5%
R29, R30, R31	Resistor, 100 ohms, 1/2 W, ±5%
S1-S8	Switch, 8-position, DIP
U1	IC, 74LS125
U2, U3	IC, 74LS10
U4, U39	IC, 74LS04
U5	IC, 74LS240
U6	IC, 74LS244
U8	IC, 7407
U9	IC, 74LS139
U10	IC, 74LS151
U11-U18	IC, 74LS85
U19,U21,U22,U24,U26	IC, 74LS259
U20	IC, 74LS00
U23,U28,U31,U34,U37	IC, 74LS251
U25,U41,U44,U47,U49	IC, 75189A
U27, U30, U33, U36	IC, TMS 9902
U29,U32,U35,U38,U40	IC, 75188
U45, U48, U51	IC, 75154
U50, U52	IC, 75189A
XU27, XU30, XU33, XU36	Socket, 20-pin
XU42, XU46	Socket, 16-pin

APPENDIX C

PORTS A-D (P2-P5) PIN ASSIGNMENTS

TABLE C-1. PORT A (P2) I/O PIN ASSIGNMENTS

P2 PIN NUMBER	SIGNAL/DESCRIPTION
1	FRAME GND.A
2	RECEIVED DATA.A
3	TRANSMITTED DATA.A
5	TERMINAL CLEAR TO SEND.A
6	TERMINAL DATA SET READY.A
7	SIGNAL GND.A
8	TERMINAL DATA CARRIER DETECT.A
15	EIA SCT.A
16	MODEM CLEAR TO SEND.A
17	EIA SCR.A
19	MODEM- DSR.A
20	TERMINAL DATA TERMINAL READY.A
21	MODEM DTR.A
22	RI.A

TABLE C-2. PORT B (P3) I/O PIN ASSIGNMENTS

P3 PIN NUMBER	SIGNAL/DESCRIPTION
1	FRAME GND.B
2	RECEIVED DATA.B
3	TRANSMITTED DATA.B
5	TERMINAL CLEAR TO SEND.B
6	TERMINAL DATA SET READY.B
7	SIGNAL GND.B
8	TERMINAL DATA CARRIER DETECT.B
15	EIA SCT.B
16	MODEM CLEAR TO SEND.B
17	EIA SCR.B
19	MODEM- DSR.B
20	TERMINAL DATA TERMINAL READY.B
21	MODEM DTR.B
22	RI.B

TABLE C-3. PORT C (P4) I/O PIN ASSIGNMENTS

P4 PIN NUMBER	SIGNAL/DESCRIPTION
1	FRAME GND.C
2	RECEIVED DATA.C
3	TRANSMITTED DATA.C
5	TERMINAL CLEAR TO SEND.C
6	TERMINAL DATA SET READY.C
7	SIGNAL GND.C
8	TERMINAL DATA CARRIER DETECT.C
15	EIA SCT.C
16	MODEM CLEAR TO SEND.C
17	EIA SCR.C
19	MODEM- DSR.C
20	TERMINAL DATA TERMINAL READY.C
21	MODEM DTR.C
22	RI.C

TABLE C-4. PORT D (P5) I/O PIN ASSIGNMENTS

P5 PIN NUMBER	SIGNAL/DESCRIPTION
1	FRAME GND.D
2	RECEIVED DATA.D
3	TRANSMITTED DATA
5	TERMINAL CLEAR TO SEND.D
6	TERMINAL DATA SET READY.D
7	SIGNAL GND.D
8	TERMINAL DATA CARRIER DETECT.D
9	EIA SCR RETURN.D
10	EIA SCT RETURN.D
15	EIA SCT.D
16	MODEM CLEAR TO SEND.D
17	EIA SCR.D
18	RS422 RECEIVED DATA.D
19	MODEM- DSR.D
20	TERMINAL DATA TERMINAL READY.D
21	MODEM DTR.D
22	RI.D
23	RECEIVED DATA RETURN.D
24	RS422 TRANSMITTED DATA RETURN.D
25	RS422 TRANSMITTED DATA

INDEX

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- Page numbers preceded by an F indicate the subject matter is explained in a figure.
- Page numbers preceded by a T indicate the subject matter is explained in a table.