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Colin Hinson
In the village of Blunham, Bedfordshire.

TECHNICAL MANUAL

FOR

MODEL MCU-8

MATRIX CONTROL UNIT

## DELTA ELECTRONICS

DELTA ELECTRONICS, INC.
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ALEXANDRIA, VIRGINIA 22312

# TECHNICAL MANUAL FOR <br> MODEL MCU-8 <br> MATRIX CONTROL UNIT 

THIS TECHNICAL MANUAL APPLICABLE TO MODEL MCU-8C MATRIX CONTROL UNIT PART NUMBER Dl3-62-97, REVISION A SERIAL NUMBER 195 DELTA ELECTRONICS REFERENCE L62

## NOTICE

This technical manual is applicable to the Model MCU-8C Matrix Control Unit, Delta Electronics, Inc. Part Number D13-62-97, Serial Number 195. This unit provides control and status display of the Model SLS-4M (20 X 2l) Strip Line Switch, Serial Number 317. In addition to the standard remote control and status display features, the subject Model MCU-8C provides automatic grounding of cleared antennas by connecting the unused antenna to the antenna ground row of the Model SLS-4M Strip Line Switch.

As described in Section 5 of this technical manual, Row $A$ on the switch provides the antenna ground function, and the first equipment input to the switch is Row B. Thus, the TX 01 control and status display functions correspond to Row $B$ of the switch. In a similar manner, the TX 02 functions correspond to Row $C$, the TX 03 functions correspond to Row $D$ and so forth through the TX 20 functions which correspond to Row $W$ of the switch. The ANT 01 through ANT 20 control and status display functions correspond to Column 1 through Column 20 of the switch, respectively. The MCU-8 transmitter and antenna numbers correlate with the proposed equipment assignments as shown in the Matrix Configuration Diagram, Figure 10-2, of the Model SLS-4M ( 20 X 21 ) Strip Line Switch technical manual. Regardless of actual equipment assignments to the switch, use TX 01 through TX 20 for inputs to the switch and ANT 01 through ANT 20 for outputs from the switch when controlling the switch with the MCU-8. Matrix Control Unit and the remote control system.

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FOR
MODEL MCU-8

## MATRIX CONTROL UNIT

SECTION 1
GENERAL INFORMATION

## SCOPE

This Technical Manual covers the description, installation, operation and maintenance of the Matrix Control Unit, Model MCU-8, manufactured by Delta Electronics, Inc.

### 1.2 GENERAL DESCRIPTION OF THE MCU-8

The Model MCU-8 Matrix Control Unit utilizes microprocessor logic to provide remote control and status display of Model SLS-IM, SLS-4M, SLS-5M and SLS-7M Strip Line Switches. As shown in Figure 8-1, the MCU-8 provides keypad entry of the matrix control commands and a video display of the matrix status. The video status display is either a schematic diagram of the RF paths through the switch matrix or a tabular listing of the transmitter and antenna connections.

Matrix control commands are entered using transmitter and antenna numeric selections from the keypad. These selections as well as the status of the selected transmitter and antenna are displayed on the bottom line of the video display for confimation. Operation of the Enable key initiates the interconnection of the selected transmitter and antenna. The indicator harness of the matrix switch is then read and the status display of the MCU-8 is updated. The standard MCU-8 also displays the interlock status, reports interconnection faults, protects active or busy transmitter/antenna circuits and identifies unavailable transmitter/antenna circuits via a lockout memory. Optional MCU-8 features include protection of priority circuits, external or additional video displays, and multiple matrix control systems.

The microprocessor logic used in the MCU-8 facilitates adaptation of the program to meet special customer requirements such as descriptive labels for transmitters and antennas, provision for inter-matrix trunking control, control of antenna slew switches or rotatable antennas, and display of transmitter operating modes.

The MCU-8 interfaces the motorized crosspoint actuators of the Strip Line Switch with an Actuator Interface Unit (AIU). The AIU decodes the low level row/column select logic from the MCU-8 and provides the high current/high voltage levels and timing signals required to operate the selected crosspoint. The AIU is normally mounted on or adjacent to the matrix switch. The MCU-8 connects to the AIU with two or more 50 -conductor cables depending on the matrix switch size.

### 1.4 STANDARD MCU-8 CONFIGURATIONS

The MCU-8 is available in the following basic models:
MCU-8A - This model provides for local control of the matrix switch. The system consists of a Local Control Unit with internal video display and keypad, Actuator Interface Unit, power supply or supplies as required for the matrix, and MCU-8/AIU interconnecting cables up to 100 ft . ( 30 m .) in length.

MCU-8B - This model provides a complete system for local and remote control. The system consists of a Local Control Unit with auxiliary items per above MCU-8A description and a Remote Control Unit with internal video display and keypad. The local and remote units provide an RS-232-C interface for use with customer supplied $300 / 4800$ baud full duplex modems and voice grade telephone lines or radio circuits.

MCU-8C - This model provides both for local control and for an RS-232-C interface to a customer's control system or computer. The system includes all MCU-8A items plus two-way ASCII data interface in a customized format at standard data rates from 50 to 19200 baud.

MCU-8D - This model provides a complete system for local and remote control using an economical "nonintelligent" remote terminal with keyboard and video display or printer. The system includes all MCU-8A items, a remote terminal, and ASCII/RS-232-C interface for use with customer supplied $300 / 4800$ baud full duplex modens and voice grade telephone lines or radio circuits.

MCU-8E - This model provides for an RS-232-C interface to a customer's control system or computer. It is designed for installation adjacent to the matrix switch and does not provide direct local control or status display. The Actuator Interface Unit components are incorporated within the MCU-8E chassis. A composite video output connector and keypad interface connector permit operation with an optional external video display unit and keypad for local maintenance procedures.

To accormodate the operational features of the different MCU-8 models and the custom interface formats or program features available through adaptation of the microprocessor program, the Principles of Operation, Installation, Operation and Maintenance sections of this manual present general information applicable to all MCU-8 configurations. These sections may be customized to present information applicable only to the subject MCU-8 system. The Lists of Material in Section 7 are customized as needed to reflect the assemblies and components of the specific MCU-8 system. The customized sections are differentiated from standard sections by the reference number suffix to the technical manual number on each page of the customized sections.

### 1.6 APPENDED TECHNICAL MANUALS

The internal video display of the Model MCU-8 is a Motorola 9-inch display module, part number M2000-355. The service manual for this display module is included as Appendix $A$ to this technical manual. Technical manuals for ancillary equipment such as data modens and remote displays are appended to this technical manual as required by the operational configuration of the MCU-8 system.

### 1.7 EQUIPMENT AND DOCUMENTS FURNISHED OR REQUIRED

Section 7.2, MCU-8 System Components, lists all items furnished for the subject MCU-8 system. Refer to the technical manual supplied with the Model SLS Strip Line Switch for items furnished with the switch. The troubleshooting instructions in Section 6 require standard test equipment such as an oscilloscope or digital voltmeter. This technical manual does not contain information on operating or maintaining the test equipment.

## SPECIFICATIONS

| Number of Transmitters: | Up to 16 (Schematic Status Display) <br>  <br> Up to 40 (Tabular Status Display) |
| :--- | :--- |
| Number of Antennas/Loads: | Up to 20 (Schenatic Status Display) <br>  <br> Up to 40 (Tabular Status Display) |
| Matrix/Transmitter/  <br> Antenna Selection: Twenty button keypad for selection and cormand <br> initiation.  |  |
| Status Display: | 9-inch CRT with 22 line by 40 or 52 character |
|  | per line format. |


| Power Requirements: | $120 / 240 \mathrm{VAC} \pm 10 \%, 50 / 60 \mathrm{~Hz}, 50$ watts nominal per unit. |
| :---: | :---: |
| Temperature: | Operating: $0^{\circ} \mathrm{C}$ to $+40^{\circ} \mathrm{C}$ |
|  | Non-operating: $-10^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Humidity: | $0 \%$ to $90 \%$ noncondensing |
| Matrix Actuator | D14-18 provided for use with $16 \times 16$ or smaller |
| Interface Unit: | SLS-1M switch. Dl4-19 provided for use with 16 X |
|  | 16 or smaller SLS-4M/5M switches. D14-33 or |
|  | D14-39 provided for use with $12 \times 12$ or smaller |
|  | or $16 \times 16$ or smaller SLS-7M switches, |
|  | respectively. Custom AIU provided for use with larger matrices. |
| Interconnecting Cable: | For interface of Local Control Unit and Matrix AIU. Standard 100 ft . ( 30 m .) cables and connectors provided. Longer cable assemblies optionally available. |
| Data Modens: | Full duplex with RS-232-C Data Interface for 10 bit asynchronous data, 300 to 4800 baud. (Not included in standard system.) |
| External Video | 10-1/2" high rack mounting unit with 14" |
| Display Unit: | display. Composite video input with |
|  | loop-through or internal 75 ohm termination. |
|  | $120 / 240 \mathrm{VAC}, 50 / 60 \mathrm{~Hz}$. (Not included in standard system.) |
| MCU-8D Remote Terminal: | Video Display/Keyboard KSR Terminal standard |
|  | full duplex 110/4800 baud. 120/240 VAC, 50/60 |
|  | Hz . |
|  | Optional: 300 or 1200 baud printer/keyboard |
|  | KSR terminals. |

## SECTION 3

## PRINCIPLES OF OPERATION

### 3.1 GENERAL

3.1.1 The MCU-8 Matrix Control Unit utilizes microprocessor logic to provide remote control and status display of Model SLS-1M, SLS-4M, SLS-5M and SLS-7M Strip Line Switches. The standard features of the MCU-8 include display of the interlock status, reporting of interconnection or switching faults, protection of active transmitter/antenna circuits and identification of unavailable transmitter/antenna circuits. The MCU-8 microprocessor logic facilitates adaptation of the program to include optional features such as a multiple matrix control system or to meet special customer requirements such as descriptive labels for the transmitters and antennas.
3.1.2 Since only the microprocessor program requires modification to incorporate optional features or special customer requirements, the basic circuit assemblies comprising the MCU-8 and their principles of operation remain standard for most MCU-8 units. Thus, the principles of operation described in this section are applicable to all MCU-8 configurations and circuit assemblies. Operational features and circuit assemblies not provided on the subject MCU-8 system that are included in this standard principles of operation section should be disregarded.

### 3.2 STANDARD MCU-8 CONFIGURATIONS

The MCU-8 is available in the following basic models:
MCU-8A - This model provides for local control of a matrix switch. The Local Control Unit provides an internal video display and front panel keypad assembly.

MCU-8B - This model provides a complete system for local and remote control. The system consists of a Local Control Unit and a Remote Control Unit each with an internal video display unit and keypad assembly. Each unit provides an RS-232-C interface for customer supplied modems.

MCU-8C - This model provides a Local Control Unit with internal video display, front panel keypad assembly and a customized RS-232-C interface to a customer's control system or computer.

MCU-8D - This model provides a complete system for local and remote control similar to the MCU-8B system except the Remote Control Unit is replaced by a standard "nonintelligent" terminal with keyboard and video display or printer.

MCU-8E - This model, designed for installation adjacent to the matrix switch, provides for control and status reporting via a customized RS-232-C interface to a customer's control system or computer and does not provide direct local control or status display. A composite video output connector and keypad interface connector permit local operation with an optional external video display unit and keypad assembly for maintenance procedures.

### 3.3 LOCAL UNIT

### 3.3.1 General

The MCU-8 Local Control Unit provides the matrix control and status display features and interfaces the remote control device, either an MCU-8B Remote Control Unit, an MCU-8D Terminal or a customer supplied control system. Figure 3-1 is a simplified block diagram of the MCU-8 Local Unit which shows typical connections to a Model SLS Strip Line Switch and other external units. The figure shows the circuit assemblies which mate with a Mother Board Assembly that provides a printed circuit bus system to support the 6502 microprocessor system. The Local Unit of each standard MCU-8 configuration utilizes some or all of the following assemblies:
(1) Microprocessor Assembly -

Provides 6502 microprocessor and associated random access memory (RAM) and programmable read only memory (PROM) integrated circuits.
(2) Video Assembly -

Provides video controller (CRTC), character generator and sync circuits for the video display unit.
(3) Video Memory Assembly -

Provides nonvolatile (battery backup) RAM for the video display unit and other memory files.
(4) PIA/Buffer Assembly -

Two or more of these assemblies are used depending on the matrix size. Provides interface to the Actuator Interface Unit (AIU) for the command and status read functions. Two assemblies will accommodate up to a $16 \times 16$ matrix.
(5) Keypad Assembly -

Mounted on front panel for command entry. Provides 16 hexadecimal keys and 4 special purpose keys.
(6) Video Display Unit -

9-inch video display unit for matrix status display.
(7) Serial Interface Assembly -

Provides RS-232-C two-way data interface for direct or modem connection to the MCU-8 Remote Unit or a customer's control system.

(8) Mother Board Assembly -

Provides printed circuit bus system to interconnect Microprocessor Assembly with support assemblies and Power Supply Assembly.
(9) Power Supply Assembly -

Provides all required supplies for the unit.

### 3.3.2 Local Mode

When in the Local mode, matrix commands are entered from the keypad assembly. Overriding the busy protection and updating the lockout memory may be performed from the keypad when required. When the keypad is not active, matrix status is updated periodically. Upon receiving a status request from the MCU-8 Remote Unit or a customer's control system, the Local Unit reads the matrix status and sends a status message to the remote device.

### 3.3.3 Remote Mode

When operating in the Remote mode, the keypad of the Local Unit is disabled and the unit periodically updates status and responds to status requests from the remote unit. Upon receiving a command message from the remote control device, the matrix will be operated to provide the selected transmitter to antenna connection.

### 3.3.4 Actuator Interface

The MCU-8 Local Unit utilizes Peripheral Interface Adapter (PIA) Assemblies to provide 12 volt CMOS logic level interface to the AIU which is normally mounted on or near the matrix switch. The AIU has an input for each row and column of the matrix to permit addressing in an $X-Y$ manner. Selected row and column inputs are pulled down and an Enable signal is applied to initiate actuator operation. The AIU provides row and column drivers which switch power to the actuators to accomplish the desired crosspoint switching.

### 3.3.5 Matrix Status Interface

The matrix status indicator switches are wired to row and column buses with isolating diodes wired in series with each switch. When in the Matrix Status Read mode one PIA Assembly provides a 12 volt CMOS signal to select a transmitter bus. The second PIA Assembly then reads the signals on the antenna buses in groups of eight antennas at a time.

### 3.3.6 Interlock Status Interface

When in the Interlock Status Read mode, a PIA Assembly provides buffered inputs to read the transmitter interlock relay contact closures in groups of eight transmitters at a time.

The Remote Unit which interfaces with the MCU-8 Local Control Unit may be either an MCU-8B Remote Control Unit, an MCU-8D Terminal or a customer supplied control system. The MCU-8B Remote Control Unit incorporates all of the features and circuit assemblies of the Local Control Unit except for the PIA/Buffer Assemblies. Unless otherwise noted, circuit assembly principles of operation are applicable to both the MCU-8B Local and Remote Control Units. The principles of operation for the terminal supplied with the MCU-8D system are included in the Technical Manual supplied with the subject terminal. Interface characteristics of the customer supplied remote control device to be used with the MCU-8C or MCU-8E Local Control Units are detailed in Sections 4 and 5 of this Technical Manual.
3.5 DESCRIPTION OF CIRCUIT ASSEMBLIES

### 3.5.1 General

The MCU-8 circuits are organized around a bus system. The components for each of the major subcircuits are mounted and interconnected on a printed circuit assembly. These assemblies are mounted and connected to the bus system by a series of card-edge connectors mounted on the Mother Board Assembly. Like pins on all connectors are connected together on the Mother Board Assembly by a printed circuit bus system. Thus, in principle, the location of any particular assembly is unimportant. Additional assemblies to perform additional functions may be plugged into unused connectors on the Mother Board Assembly without regard to location except for the connector adjacent to the power transformer which is reserved for the Power Supply Assembly.

The bus system carries supply voltages for all assemblies, address information used by the processor to individually select the circuits, an eight line data bus for exchange of data, and control lines to supervise and time the circuit functions. Figure 3-2, Mother Board Assembly Bus Assignment, tabulates the function of each bus circuit. These circuits are available to all assemblies on the bus. In addition, there are special circuits which are used to connect the assemblies to circuits outside of the bus system and circuits which interconnect only selected assemblies within the system. These circuits are connected via header connectors, ribbon cables or special cables such as coaxial cables.

Figure 8-4, Matrix Control Unit Block Diagram, details all the connections between the circuit assemblies. Individual schematic diagrams for each assembly are cited by figure number in the block representing the assembly. Figure 8-5, Power Supply Schematic Diagram, details the power supply circuit which includes circuits on the Power Supply Assembly (shown in dashed lines on the schematic diagram) and chassis mounted components.

The Power Supply Assembly is not technically on the bus system. It, therefore, must always be mounted in the connector adjacent to the power transformer. The front panel mounted Keypad Assembly connects to the bus system via a ribbon cable which connects to the Serial Interface Assembly. The Video Display Unit (VDU) receives 12 VDC power from the Video Power switch and video/sync signals from the Video Assembly through a plug-in cable assembly connected to the rear of the VDU.

| PIN | FUNCTION | PIN | FUNCTION |
| :---: | :---: | :---: | :---: |
| 1 | +5 VDC | A | A0 ADRS LINE |
| 2 | BATTERY BACK-UP | B | Al ADRS LINE |
| 3 | RESET SWITCH | C | A2 ADRS LINE |
| 4 | RESET | D | A3 ADRS LINE |
| 5 | IRQ | E | A4 ADRS LINE |
| 6 | NMI | F | A5 ADRS LINE |
| 7 | D0 DATA LINE | H | A6 ADRS LINE |
| 8 | Dl DATA LINE | J | A7 ADRS LINE |
| 9 | D2 DATA LINE | K | A8 ADRS LINE |
| 10 | D3 data line | L | A9 ADRS LINE |
| 11 | D4 DATA LINE | M | Al0 ADRS LINE |
| 12 | dS data line | N | All ADRS LINE |
| 13 | D6 DATA LINE | P | Al2 ADRS LINE |
| 14 | D7 DATA LINE | R | Al3 ADRS LINE |
| 15 | +12 VDC | S | Al4 ADRS LINE |
| 16 | -5 VDC | T | R/W |
| 17 | PWR LOSS DET | U | K1, MEM BLK SEL |
| 18 | RAM R/W | V | K2, MEM BLK SEL |
| 19 | EXT CLOCK | W | K3, MEM BLK SEL |
| 20 | PHASE 2 | X | K4, MEM BLK SEL |
| 21 | -12 VDC | Y | K5, MEM BLK SEL |
| 22 | GND | Z | K6, MEM BLK SEL |

### 3.5.2 Power Supply

The Power Supply provides the regulated $+5 \mathrm{VDC},-5 \mathrm{VDC},+12 \mathrm{VDC}$ and -12 VDC supplies for the integrated circuit components of the MCU-8 assemblies, a separate regulated +12 VDC supply for the VDU and an unregulated +24 VDC supply. The power supply consists of a printed circuit Power Supply Assembly A3 containing the rectifiers and low current $-5,+12$ and -12 voltage regulators and chassis mounted components including the AC input filter, power switches, power transformer and the high current +5 and +12 voltage regulators.

With reference to Figure 8-5, Power Supply Schematic Diagram, the $120 / 240 \mathrm{VAC}, 50 / 60 \mathrm{~Hz}$ main power is applied to the primary of the power transformer Tl via the line filter FLl, line fuse Fl, main power switch Sl and barrier strip TBl. Varistor RVl is connected across terminals 1 and 3 of line filter FLl to suppress voltage transients on the AC power line. The power transformer has dual primary windings each with $+10 \%$ taps. The transformer is shown connected for 120 VAC operation in Figure 8-5. Series connection of the primary windings using TBI as shown in the insets of Figure 8-5 permits operation with either 220 VAC or 240 VAC main power. The main power switch is an illuminated, alternate action pushbutton switch located on the lower right section of the front panel. The switch is illuminated when AC power is applied to the MCU-8 by a lamp powered from the 12 VDC regulated video supply.

The transformer secondary has two 18 VRMS windings which are connected to the Power Supply Assembly via the Mother Board Assembly. The Mother Board Assembly provides connections between terminals 3 through 8 and connector Jl pins $F$ through $U$ as shown in Figure $8-5$. These pin functions differ from the bus assignments of Figure 3-2 and thus, the Power Supply Assembly must always be plugged into the Mother Board Assembly card-edge connector Jl adjacent to the power transformer. Bridge rectifier A3CR1 rectifies the 18 VRMS center-tapped output of Tl to drive the +5 and the -5 VDC regulator. Bridge rectifier A3CR2 rectifies the 36 VRMS center-tapped output of Tl to drive the two +12 and the -12 VDC regulators.

The full-wave rectified positive output of A3CR1 is filtered by chassis mounted capacitor Cl and applied to the +5 VDC logic supply regulator VRl. Regulator VRl and its stabilizing capacitors C3 and C4 are rear panel mounted. The +5 VDC output of VRl returns to the Power Supply Assembly and connects to pin 1 of the Mother Board Assembly bus for distribution to the assemblies plugged into the Mother Board Assembly. Should VRl fail and the output increase above approximately 5.25 VDC, over-voltage protector A3Ul will trigger A3CR7 to clamp the 5 volt bus to ground, initially protecting all assemblies operating from the +5 VDC bus. After approximately ten seconds of operation with regulator VRl in its short circuit current limit mode, fuse A3Fl blows to protect all components associated with the +5 VDC supply.

The full-wave rectified positive output of A3CR2 is filtered by chassis mounted capacitor C2 and applied to the +12 VDC video display unit regulator VR2. Regulator VR2 and its stabilizing capacitors C5 and C6, overvoltage protector VR3 and fuse F2 are rear panel mounted. If VR2 fails and the video supply voltage increases above approximately 13.7 volts, VR3 will effectively short circuit and clamp the 12 volt video supply to ground.

After approximately five seconds of short circuit current, fuse F 2 blows to protect the video equipment and power supply. If F 2 blows, there will be no display on the MCU-8 video screen, but the MCU-8 will continue to operate. The +12 VDC output of VR2 connects to the video display unit via switch S 2 . Video power switch S2 is an illuminated, alternate action pushbutton switch located on the lower left section of the front panel. This switch is illuminated when $D C$ power is applied to the video display unit. The video display can be turned off independently of the rest of the MCU-8 system.

Power Supply Assembly mounted voltage regulators A3VR1, A3VR2 and A3VR3 provide the regulated $-12 \mathrm{VDC},+12 \mathrm{VDC}$ and -5 VDC , respectively, to the assemblies plugged into the Mother Board Assembly. Rectifiers A3CR3 and A3CR4, resistor A3R5 and capacitor A3C6 form the rectifier and filter circuit for the +24 V unregulated supply which is not normally used in the MCU-8.

Integrated circuit A3U2 is a voltage comparator which detects low main AC voltage conditions and provides a forewarning of system power loss. A sample of the $D C$ filtered input to VRI is compared against a reference voltage established by zener diode A3CR6 and potentiometer A3R16. The reference voltage is adjusted so that when the AC main voltage falls below approximately 90 VAC for 120 VAC primary power, below approximately 165 VAC for 220 VAC primary power, or below approximately 180 VAC for 240 VAC primary power due to either a power outage or a low AC voltage condition, the reference voltage will exceed the sample of the VRl input voltage. Under this condition, the comparator takes the normally high power loss detect bus to a logic low state. The active low power loss detect signal disconnects the random access memories from the system address bus and takes the processor to the reset condition. The hysteresis circuit of comparator A3U2 maintains the power loss detect bus in a low state until the main AC voltage reaches 94 VAC for 120 VAC primary power, 172 VAC for 220 VAC primary power, or 188 VAC for 240 VAC primary power. At this point, the power loss detect returns high, restoring the access to the random access memories and restarting the processor program from the beginning. Under a complete power outage condition, as the random access memory supply voltage drops to approximately 4.1 volts, the random access memory supply will be switched to the backup batteries BT1, BT2 and BT3 which maintain a data retention supply voltage to the memories.

### 3.5.3 Microprocessor Assembly

The Microprocessor Assembly, reference designation A4, provides the 6502 microprocessor and its associated support circuits including random access memory, programmable read-only memory and the address decoding logic circuits.

With reference to Figure 8-6, Microprocessor Assembly Schematic Diagram, integrated circuit $U l$ is an 8 -bit microprocessor. The microprocessor operates at a 1 MHz clock rate using the external clock, Phase 0, generated by the Video Assembly. By deriving the processor clock from the Video Assembly clock, video memory access conflicts between the processor and the video display circuits do not occur. When the processor clock, Phase 2, is high, the video memory is accessed by the processor. When the Phase 2 clock is low, the video memory is accessed by the video display
circuits. This transparent operation of the video refresh memory permits the memory to be changed by the processor without update glitches on the video display.

Integrated circuit U2 provides the reset circuit which initiates processor operation either on power up or upon operation of the reset switch. The processor is also reset via the power loss detect circuit of the Power Supply Assembly upon momentary power outages or low main AC voltage conditions. Integrated circuit U2 also compares the +5 VDC supply to the backup battery supply voltage and switches the RAM supply (VBATT) to the backup battery supply if the +5 VDC supply falls below the battery supply to provide nonvolatile memory.

Integrated circuit $U 3$ is a hex inverter which buffers both the Phase 2 clock and the read/write signal ( $\mathrm{R} / \mathrm{W}$ ) prior to distribution to the assemblies plugged into the Mother Board Assembly.

Integrated circuit U 4 is a BCD -to-Decimal decoder which decodes the highest three address lines Al3, Al4 and Al5, to produce the six memory block select signals Kl through K 6 . These block select signals function as chip select signals for the peripheral circuits of the MCU-8 and correspond to the following hexadecimal address ranges:

| Block Select | Selects |
| :---: | :---: |
| K1 | $\$ 2000-\$ 3 \mathrm{FFF}$ |
| K2 | $\$ 4000-\$ 5 \mathrm{FFF}$ |
| K3 | $\$ 6000-\$ 7 \mathrm{FFF}$ |
| K4 | $\$ 8000-\$ 9 \mathrm{FFF}$ |
| K5 | $\$ A 000-\$ \mathrm{BFFF}$ |
| K6 | $\$ C 000-\$ \mathrm{DFFF}$ |

Integrated circuit U5, a triple 3-input NAND gate, provides latching Enable pulses for the $8 \mathrm{~K} \times 8$ random access memory and removes this memory from the rest of the circuit when a power loss is detected to retain the data stored. The circuit also generates the RAM $\mathrm{R} / \mathrm{W}$ signal by ANDing the Phase 2 clock with the processor $\mathrm{R} / \mathrm{W}$ clock.

Integrated circuit U6 is the 8192 X 8 random access memory (RAM) used for scratch memory, processor stack and data files in the MCU-8. It is powered from the VBATT output of integrated circuit U2. This output is the +5 VDC logic supply during normal operation but is switched by $U 2$ to the backup battery supply during a power outage or power-down condition to maintain operating voltage to the RAM and thereby provide nonvolatile memory.

Integrated circuits U8 and U9 are the programmed read-only memory (PROM) which contain the operating program for the MCU-8 system. Generally, the MCU-8 uses either one or two $8 \mathrm{~K} \times 8$ PROMs and the programmable jumpers W1 and W2 are installed as shown in Figure 8-6. When the operating program
exceeds the standard 16 K capacity of U 8 and U 9 combined, then either U 8 only or U8 and U9 are changed to $16 \mathrm{~K} X 8$ PROMs to provide program capacity of 24 K or 32 K , respectively. For this expanded memory case, programmable jumpers W1 and W2 are installed as tabulated in Figure 8-6. Refer to the Microprocessor Assembly List of Material in Section 7 for the utilization and part numbers of U8 and U9.

### 3.5.4 Keypad Assembly

The Keypad Assembly, reference designation A5, provides ten numeric keys, 0 through 9; four control keys, Matrix, Transmitter, Antenna and Enable; and six special function keys $A$ through $F$ for command entry. The circuits of this assembly sense the key depression and translate the key number to a binary code to be read by the processor over the data bus. The Keypad Assembly interfaces the processor bus system using a 16-conductor ribbon cable assembly wh which connects Jl of the Keypad Assembly to J2 of the Serial Interface Assembly.

With reference to Figure 8-7, Keypad Assembly Schematic Diagram, integrated circuit Ul is a scanning keypad decoder with an internal clock timed by capacitors Cl and C2. The keypad switches are connected in a 4 column by 4 row matrix for scanning by Ul. Special function keys C, D, E and F on bus Y 4 are enabled via jumper Wl on the MCU-8 unit.

Integrated circuit U 2 functions as an address decoder circuit to permit the processor to address and read the decoded outputs of Ul , D0 through D4 and the buffered outputs of U3, D5, D6 and D7. Integrated circuit U3 is a tristate data bus buffer which connects external switch closures on D5 and D6 and the keypad active signal on D7 to the processor data bus. The front panel Local/Remote switch or Norm/Priority switch is connected to pin 5 and pin 2 of connector J2. Thus, the status of this switch is indicated by data bit D5.

Transistor Ql and associated components RI and C 4 provide an interrupt circuit which allows the Keypad Assembly to interrupt the processor when a key is depressed. The MCU-8 unit does not use an interrupt driven keypad routine and jumper $W 2$ is normally omitted.

### 3.5.5 Serial Interface Assembly

The Serial Interface Assembly, reference designation A6, provides an RS-232-C interface for transmission and reception of serial data between MCU-8 units or between an MCU-8 unit and a computer control system. This assembly also connects the Keypad Assembly to the processor bus system and reads the status of the diagnostic switches and custom feature jumpers.

With reference to Figure 8-8, Serial Interface Assembly Schematic Diagram, integrated circuit Ul is an Asynchronous Communications Interface Adapter (ACIA) which interfaces the serial data information to the microprocessor bus system. Data characteristics such as number of data bits, number of stop bits and parity are programmed by the processor. Received data is checked for proper formatting and errors and converted to parallel data to be read by the processor. Data to be transmitted is
written to the ACIA by the processor. Internal ACIA registers accessible to the processor indicate the status of the Transmit Data register, the Receive Data register and error checking logic.

Integrated circuit U 2 is a peripheral interface adapter which interfaces the status of the custom feature jumpers W6 through W13 and the status of the diagnostic switches to the microprocessor bus system. Integrated circuit U2 also interfaces the status of the MCU-8 address switches S1 and S2 to the bus and provides via the CA2 output an Enable signal to the line driver circuit $U 4$ to switch it from the high impedance mode to the active mode. The MCU-8 address switches S1 and S2 establish the unit address for all serial communications. For two digit address applications, $S l$ provides the LSD and S2 provides the MSD. For single digit address applications, S1 and S2 are set to the ASCII code for the desired address. Thus, for an address of 1 , switch $S 1$ is set to 1 and switch $S 2$ is set to 3 yielding the code 31 , the ASCII representation of 1 . Custom feature jumpers $W 6$ through $W 9$ provide programmable information to the processor such as $50 / 60 \mathrm{~Hz}$ sync for the video display, and even/odd parity for the serial data. Jumpers W10 through W13 are normally not used and the upper four PB ports monitor the chassis mounted diagnostic switches 57 through Sl0 which are connected via connector J3. These diagnostic switches provide special diagnostic information and commands to the processor such as reload lockout memory from PROM and defeat crosspoint lockout status test.

Integrated circuit U3 is a dual baud rate generator that provides independent receive and transmit clocks to the ACIA. Switch S3 selects the baud rate for serial reception and switch S 4 selects the baud rate for serial transmission according to the following table:

| Switch Position | Baud Rate |
| :---: | :---: |
| 0 |  |
|  | 50 |
| 2 | 75 |
| 3 | 110 |
| 4 | 134.5 |
| 5 | 150 |
| 6 | 300 |
| 7 | 600 |
| 8 | 1200 |
| 9 | 1800 |
| A | 2000 |
| B | 2400 |
| C | 3600 |
| D | 4800 |
| E | 7200 |
| F | 9600 |
|  | 19200 |

The serial output of the ACIA is at a TML logic level. Integrated circuit U4 inverts and converts this level to nominal RS-232-C levels of +6 and -6 volts. This circuit is switched from a tristate or high impedance output mode to an active output mode under the control of the CA2 signal from U2. When used with dedicated serial data communications circuits, the

U4 output is always active. When used with multi-drop data circuits, U4 output is normally tristate and is switched to an active mode only when the MCU-8 transmits serial data.

The received $R S-232-C$ serial data is buffered by operational amplifier U6 to provide a high input impedance for multi-drop data circuits. Line receiver circuit $U 5$ inverts and converts to TTL logic level the received serial data.

Relay Kl is energized whenever AC power is applied to the MCU-8. The contacts of this relay switch the serial output of $U 4$ to the serial interface connector. These contacts open when AC power is not applied to the MCU-8 to prevent U 4 from loading the multi-drop data circuit.

The Serial Interface Assembly connects to the rear panel serial connector Jl using a 24-conductor ribbon cable assembly, W4.

### 3.5.6 Video Assembly

The Video Assembly, reference designation A7, provides the video signals corresponding to the contents of the video memory, the vertical sync and the horizontal drive to the internal video display unit. The assembly also provides a composite video signal for an external monitor and the synchronous 1 MHz clock signals for the processor.

With reference to Figure 8-9, Video Assembly Schematic Diagram, integrated circuit Ul is a CRT Controller (CRTC) which performs the processor interface to raster scan CRT displays. The CRTC is programmed for display attributes such as number of characters per line and number of lines per displayed page through the processor bus system. The CRTC addresses the video refresh memory via connector Jl and provides character row addresses to the character generator.

Integrated circuit U2 is a dot matrix character generator which contains a read-only memory programmed with 128 characters in a $7 \times 11$ dot matrix. U2 also provides a high speed video shift register to produce the serial video output on pin 2.

Integrated circuits U9C and U9D.and crystal Yl form a 10 MHz dot clock oscillator. This oscillator provides the clock for the character generator shift register and the clock from which the processor clock is derived.

Integrated circuit U6, a divide by ten counter, divides the 10 MHz dot clock down to the 1 MHz Phase 0 processor clock. This circuit also provides the timing signals for the blanking flip-flop, the reverse video flip-flop and the character generator parallel load enable, PE. The output signals of U6 are decoded by integrated circuits U9A, U9B, U7C and U10A. Integrated circuit U1OD provides the clock for the CRTC and the address strobe for the character generator. The video memory data bits MD0 through MD6 form the seven bit address for the character generator read-only memory. The eighth data bit, MD7, drives the reverse video flip-flop, U5. When MD7 is low, the video is normal and conversely, when MD7 is high, the video is reversed, i.e., the character is dark and the background color is light.

The serial video output from the character generator shift register is applied to integrated circuit U8A, an exclusive OR gate used as a programmable inverter. The second input to this gate is driven by the reverse video flip-flop, U5, When the Q2 output of U5 is low, the serial video data is not inverted providing normal video and when the Q 2 output of U5 is high, the serial video is inverted and the displayed video is reversed. Integrated circuit UlOB mixes the blanking signals from the blanking flip-flop, U4, with the serial video data from U8A. Integrated circuit UlOC buffers the video signals to drive the video mixer circuit consisting of transistors Q2 and Q3. The vertical sync and horizontal sync from integrated circuit Ull are mixed by integrated circuit U8B. The output of U8B drives transistor $Q 1$ which adds the sync signals to the mixer circuit. The composite video output of the mixer circuit is variably attenuated by the contrast control R9 and then applied to connector J3, pin 1 for distribution to the internal video display unit and the rear panel composite video output connector.

The vertical sync output signal from the CRTC triggers the $B$ section of the dual monostable multivibrator Ull which generates a 190 microsecond vertical sync pulse. Both positive and negative sync pulses are generated by UllB. In the MCU-8 the positive polarity pulse is applied via jumper W6 to connector J3, pin 5 which connects to the vertical sync input of the internal video display unit. The MCU-8 does not utilize the interrupt generating circuits consisting of transistor $Q 4$ and jumper $W 8$.

The buffered horizontal sync signal from integrated circuit U8C triggers the A section of the dual monostable multivibrator Ull which generates a 27.5 microsecond horizontal drive signal. This signal is applied to connector J3, pin 3 which connects to the horizontal drive input of the internal video display unit.

Integrated circuits U7A and U7B provide the address decoder logic for the Video Assembly.

Connector Jl connects to connector Jl of the Video Memory Assembly using a 24 -conductor ribbon cable assembly W6. This cable assembly provides the video address signals from the CRTC to the video memory and the video refresh data from the video memory to the CRTC.

Connector J3 connects to the internal video display unit and provides composite video, horizontal sync and vertical sync. The composite video is also distributed to the rear panel connector Jl2 for connection to an external video monitor.

### 3.5.7 Video Memory Assembly

The Video Memory Assembly, reference designation A8, provides the random access memory which is used as the refresh memory for the video display. This memory is accessed alternately by the processor to store the data to be displayed and then by the CRTC to display the data.

With the reference to Figure 8-10, Video Memory Assembly Schematic Diagram, the MCU-8 uses integrated circuit U5 to provide 8192 bytes ( $8 \mathrm{~K} \times 8$ ) of random access video memory. For the standard MCU-8 with a video format of 52 columns by 22 rows, 1144 bytes are required for the video data.

Lockout memory data, optional user assignable equipment labels, scratch memory and miscellaneous data files are also stored in this random access memory. Pull-up resistor network Ul8 maintains the memory data lines, MD0 through MD7, in a logic high state when the data lines are not being accessed by either the processor or the CRTC. The power loss detect signal deselects the memory circuit to prevent writing data to memory during a power loss condition.

The random access memory circuits are made non-volatile by the battery back-up assembly. Regulator VRl provides 5 VDC to the memory circuits in normal operation. During a power down condition, diodes CRI and CR3 switch the RAM supply to the back-up battery assembly providing non-volatile memory.

As noted, the processor and the CRTC share access to the video memory. The address lines and the data lines for the memories are available to the processor when the phase 2 clock is high and are available to the CRTC when the Phase 2 clock is low. Integrated circuits U1, U2, U3 and U4 are quadruple 2-line-to-l-line data multiplexers that switch the memory address lines between the processor and the CRTC. Integrated circuits U8 and $U 9$ are tristate multiplexers that switch the data lines between the processor and the CRTC. Integrated circuits U6 and U7 provide the address decoder logic and the multiplexer drive logic.

Connector Jl connects to connector Jl of the Video Assembly using a 24 -conductor ribbon cable assembly, W6. This cable assembly provides the video address signals from the CRTC to the video memory and the video refresh data from the video memory to the CRTC.

### 3.5.8 Row Address PIA Assembly

The Row Address PIA Assembly, reference designation A9A, provides the interface between the MCU-8 and the circuits of the Row Driver Actuator Interface Unit. This PIA Assembly is used for a large matrix with seventeen to forty rows. This assembly outputs the row select signals for Rows A through $R R$ and outputs the matrix enable signals.

With reference to Figure 8-11, D33-299-1, Row Address Peripheral Interface Assembly Schematic Diagram, integrated circuit Ul is a peripheral interface adapter which interfaces the processor data lines to the CMOS/TIL level converter/buffer integrated circuits U2 through U7. Integrated circuit Ul provides two 8-bit bidirectional peripheral data buses, PA0 through PA7 and PB0 through PB7, and four control lines, CA1, CA2, CB1 and CB2. The 8-bit data bus, PA0 through PA7, is used to write to the buffers the row select data. The 8-bit data bus, PBO through PB7, is used as a control signal bus that enables buffers U2, U3, U4, U5 or U6 and provides matrix enable signals via buffer U7. Control line CB2 is used as a control signal to enable buffer U7. Control lines CAl, CA2 and CBl are not used.

The functional configuration of Ul is programmed by the processor through the data bus. At system initialization, the PA data lines, the PB data lines, and the CB2 control line are programmed as outputs.

Integrated circuits U2 through U7 are 8-bit bidirectional CMOS/TTL level converters. They provide conversion of the TTL logic level outputs of Ul to the 12 Volt CMOS logic level inputs of the AIU. Their bidirectional feature provides the reverse function of 12 Volt CMOS level conversion to TTL level inputs to Ul. A third high-impedance (tristate) mode permits the $P A$ data lines of $U l$ to be bused to multiple buffers, functioning as either input or output buffers, without bus contention.

The three operating modes of the level converting integrated circuits are established by the state of the enable input and the disabie input. Once a buffer is dedicated as either an input or an output, it can be toggled between the active mode and the high-impedance mode by controlling the enable input for output buffers or the disable input for input buffers. The configuration of $U 2$ through $U 7$ is established by jumpers W3 through W8, respectively. On the Row Address PIA Assembly, integrated circuit U 2 is an output and is controlled by the PBO data line of U1. In a similar manner, U3, U4, U5 and U6 are outputs and are controlled by data lines PB1, PB2, PB3 and PB4, respectively. Buffer $U 7$ is configured as an output and is controlled by CB2 as programmed by jumper W16C. The data lines to buffer U6 are programmed by jumpers W15A, W15C, W15E and W15G to be PAO through PA7. The data lines to buffer $U 7$ are programmed by jumpers W15B, W15D, W15F and W15H to be PA0 through PA3 and PB4 through PB7. This technique allows control signals such as the matrix enable to be applied to the AIU using PB4 through PB7 while the PA0 through PA7 data is also applied to the AIU via another active buffer.

Integrated circuits U 2 through U6 provide the Row Address data to the AIU. The selected transmitter or antenna is decoded into a 1-of-8 code and a buffer select code and written over the data bus to Ul. For transmitters or antennas assigned to Rows A through H, U2 will be enabled and one of the eight outputs, corresponding to the selected transmitter or antenna, will be an active low. In a similar manner, for an address of Rows J through R, U4 will be enabled; for an address of Rows $S$ through $Z$, U6 will be enabled; for an address of Rows AA through HH, U3 will be enabled and for an address of Rows JJ through RR, U5 will be enabled. In each case, only one output of the five buffers will be an active low. The Row Driver Actuator Interface Unit uses the active low row input to establish the desired transmitter to antenna switching on the matrix.

Integrated circuit U7 provides the Phase l, Phase 2 and Phase 3 timing signals via control lines PB5, PB6 and PB7 to the Row Driver Actuator Interface Unit. The Row Driver AIU trunks through the Phase 1 and Phase 2 signals to the Column Driver AIU. These timing signals control the switching of the matrix to establish the transmitter to antenna connection specified by the Row Select buffers of the Row Address PIA Assembly and the Col Select buffers of the Column Address PIA Assembly.

Resistors R1 through R6 ensure that the buffers U2 through U7 start up in a high-impedance mode prior to initialization of Ul and subsequent processor control of the high-impedance mode. Pull-up resistor network Ul3 provides bias for the Phase 1, phase 2 and Phase 3 timing signals.

Connector Jl of the Row Address PIA Assembly connects to rear panel connector J2 using a 50 -conductor ribbon cable assembly, W2A.

The Column Address PIA Assembly, reference designation AlOA, provides the interface between the MCU-8 and the circuits of the Column Driver Actuator Interface Unit. This PIA Assembly is used for a large matrix with seventeen to forty columns. This assembly outputs the column select signals for Columns 1 through 40 and inputs the Power Supply Status signals.

With reference to Figure 8-12, D33-299-2, Column Address Peripheral Interface Assembly Schematic Diagram, integrated circuit Ul is a peripheral interface adapter which interfaces the processor data lines to the CMOS/TTL level converter/buffer integrated circuits U2 through U7. Integrated circuit Ul provides two 8-bit bidirectional peripheral data buses, PAO through PA7 and PB0 through PB7, and four control lines, CA1, CA2, CBI and CB2. The 8-bit data bus, PAO through PA7, is used to write to the buffers the column select data. The 8-bit data bus, PBO through PB7, is used as a control signal bus that enables buffers U2, U3, U4, U5, U6 or U7. Control lines CA1, CA2, CB1 and CB2 are not used.

The functional configuration of Ul is programmed by the processor through the data bus. At system initialization, the PA data lines and the PB data lines are programmed as outputs. When a read of the Power Supply Status via buffer $U 7$ is required, the PA lines are programmed as inputs, the power supply data is inputted, and the PA lines are then reprogrammed to their normal output function.

Integrated circuits U2 through U7 are 8-bit bidirectional CMOS/TTT level converters. They provide conversion of the TII logic level outputs of Ul to the 12 Volt CMOS logic level inputs of the AIU. Their bidirectional feature provides the reverse function of 12 Volt CMOS level conversion to TTL level inputs to Ul. A third high-impedance (tristate) mode permits the PA data lines of $U l$ to be bused to multiple buffers, functioning as either input or output buffers, without bus contention.

The three operating modes of the level converting integrated circuits are established by the state of the enable input and the disable input. Once a buffer is dedicated as either an input or an output, it can be toggled between the active mode and the high-impedance mode by controlling the enable input for output buffers or the disable input for input buffers. The configuration of U 2 through U 7 is established by jumpers W3 through W8, respectively. On the Column Address PIA Assembly, integrated circuit U2 is an output and is controlled by the PBO data line of Ul. In a similar manner, U3, U4, U5 and U6 are outputs and are controlled by data lines PB1, PB2, PB3 and PB4, respectively. Buffer U7 is configured as an input and is controlled by PB5 as programmed by jumper Wl6D. The data lines to buffer U6 are programmed by jumpers W15A, W15C, WL5E and WL5G to be PA0 through PA7. The data lines to buffer U7 are programmed by jumpers W15B, W15D, W15F and W15H to be PAO through PA7.

Integrated circuits U2 through U6 provide the Column Address data to the AIU. The selected antenna or transmitter is decoded into a l-of-8 code and a buffer select code and written over the data bus to Ul. For antennas or transmitters assigned to Columns 1 through 8 , U 2 will be enabled and one of the eight outputs, corresponding to the selected antenna or
transmitter, will be an active low. In a similar manner, for an address of Columns 9 through 16, U4 will be enabled; for an address of Columns 17 through 24, U6 will be enabled; for an address of columns 25 through 32, U3 will be enabled and for an address of Columns 33 through 40 , U5 will be enabled. In each case, only one output of the five buffers will be an active low. The Column Driver Actuator Interface Unit uses the active low column input to establish the desired transmitter to antenna switching on the matrix.

Integrated circuit $U 7$ reads the Power Supply Status provided by the relay contact closures on the AIU Timing Control Assembly. When interfaced with an SLS-1M or 7 M matrix, the three Power Supply Status inputs are read via data lines PA0, PAl and PA2. When interfaced with an SLS -4 M or 5 M matrix, the single Power Supply Status input is read via data line PA0.

Resistors Rl through R6 insure that the buffers U2 through U7 start up in a high-impedance mode prior to initialization of Ul and subsequent processor control of the high-impedance mode. Pull-up resistor network Ul3 provides bias for the contacts of the Power Supply Status relays.

Connector Jl of the Column Address PIA Assembly connects to rear panel connector J3 using a 50-conductor ribbon cable assembly, W3A.

### 3.5.10 Row Status PIA Assembly

The Row Status PIA Assembly, reference designation A9B, provides the interface between the MCU-8 and the row indicator circuits of the Model SLS Switch. This PIA Assembly is used for a large matrix with seventeen to forty rows. This assembly outputs the row status signals for Rows A through RR.

With reference to Figure 8-13, D33-299-3, Row Status Peripheral Interface Assembly Schematic Diagram, integrated circuit Ul is a peripheral interface adapter which interfaces the processor data lines to the CMOS/TTL level converter/buffer integrated circuits U2 through U7. Integrated circuit Ul provides two 8-bit bidirectional peripheral data buses, PAO through PA7 and PB0 through PB7, and four control lines, CA1, CA2, CB1 and CB2. The 8-bit data bus, PA0 through PA7, is used to write to the buffers the row status data. The 8-bit data bus, PB0 through PB7, is used as a control signal bus that enables buffers U2, U3, U4, U5, U6 or U7. Control lines CAl, CA2, CB1 and CB2 are not used.

The functional configuration of Ul is programmed by the processor through the data bus. At system initialization, the PA data lines and the $P B$ data lines are programmed as outputs.

Integrated circuits U2 through U7 are 8-bit bidirectional CMOS/TTL level converters. They provide conversion of the TTL logic level outputs of Ul to the 12 Volt CMOS logic levels of the status circuits. Their bidirectional feature provides the reverse function of 12 Volt CMOS level conversion to TTL level inputs to U1. A third high-impedance (tristate) mode permits the PA data lines of $U 1$ to be bused to multiple buffers, functioning as either input or output buffers, without bus contention.

The three operating modes of the level converting integrated circuits are established by the state of the enable input and the disable input. Once a buffer is dedicated as either an input or an output, it can be toggled between the active mode and the high-impedance mode by controlling the enable input for output buffers or the disable input for input buffers. The configuration of U 2 through U 7 is established by jumpers W3 through W8, respectively. On the Row Status PIA Assembly, integrated circuit U2 is an output and is controlled by the PBO data line of U1. In a similar manner, U3, U4, U5 and U6 are outputs and are controlled by data lines PB1, PB2, PB3 and PB4, respectively. Buffer U7 is configured as an output and is controlled by PB5 as programmed by jumper W16D. The data lines to buffer U6 are programmed by jumpers Wl5A, Wl5C, Wl5E and Wl5G to be PAO through PA7. The data lines to buffer $U 7$ are programmed by jumpers W15B, W15D, W15F and W15H to be PA0 through PA7. Although buffer U7 is programmed and controlled in a manner similar to the other buffers, it is not used on the Row Status PIA Assembly and is provided only to permit PIA Assembly interchangeability.

Integrated circuits U2 through U6 provide the Row Status data to the row indicator harness of the matrix. Similar integrated circuits on the Column Status PIA Assembly interface to the column indicator harness of the matrix. When a transmitter to antenna connection exists on the matrix, the Row Status (indicator) line will be switched to the Column Status (indicator) line at that particular crosspoint. Thus, the Column Status PIA Assembly will input an active low signal on the corresponding Column Status line when the Row Status PIA Assembly takes the corresponding Row Status line active low. (As the MCU-8 performs a read of the indicator harness to determine the matrix status, the row status lines are sequentially taken to an active low state. While a given Row Status line is active, the column Status PIA Assembly reads the Column Status lines for all active columns. 1 The data read from these column status lines thus indicate the column connected to the subject row. A fault condition where multiple columns have been switched to the same row is detected since more than one Column Status line will be in the active low state for a given row.

Resistors R1 through R6 insure that the buffers U2 through U7 start up in a high-impedance mode prior to initialization of Ul and subsequent processor control of the high-impedance mode.

Connector Jl of the Row Status PIA Assembly connects to rear panel connector J4 using a 50-conductor ribbon cable assembly, W2B.

### 3.5.11 Column Status PIA Assembly

The Column Status PIA Assembly, reference designation AlOB, provides the interface between the MCU-8 and the column indicator circuits of the Model SLS Switch. This PIA Assembly is used for a large matrix with seventeen to forty columns. This assembly inputs the column status signals for Columns 1 through 40.

With reference to Figure 8-14, D33-299-4, Column Status Peripheral Interface Assembly Schematic Diagram, integrated circuit Ul is a peripheral interface adapter which interfaces the processor data lines to the CMOS/TTL level converter/buffer integrated circuits U2 through U7. Integrated circuit Ul provides two 8-bit bidirectional peripheral data buses, PA0
through PA7 and PB0 through PB7, and four control lines, CA1, CA2, CB1 and CB2. The 8-bit data bus, PA0 through PA7, is used to read from the buffers the column status data. The 8-bit data bus, PB0 through PB7, is used as a control signal bus that enables buffers U2, U3, U4, U5, U6 or U7. Control lines CA1, CA2, CB1 and CB2 are not used.

The functional configuration of Ul is programmed by the processor through the data bus. At system initialization, the PA data lines are programmed as inputs and the PB data lines are progranmed as outputs.

Integrated circuits U 2 through U 7 are 8 -bit bidirectional CMOS/TTL level converters. They provide conversion of the TTL logic level outputs of Ul to the 12 Volt CHOS logic levels of the status circuits. Their bidirectional feature provides the reverse function of 12 Volt CMOS level conversion to TTL level inputs to Ul. A third high-impedance (tristate) mode permits the PA data lines of $U l$ to be bused to multiple buffers, functioning as either input or output buffers, without bus contention.

The three operating modes of the level converting integrated circuits are established by the state of the enable input and the disable input. Once a buffer is dedicated as either an input or an output, it can be toggled between the active mode and the high-impedance mode by controlling the enable input for output buffers or the disable input for input buffers. The configuration of U 2 through U 7 is established by jumpers W3 through W8, respectively. On the Column Status PIA Assembly, integrated circuit U 2 is an input and is controlled by the PBO data line of Ul . In a similar manner, U3, U4, U5 and U6 are inputs and are controlled by data lines PB1, PB2, PB3 and PB4, respectively. Buffer U7 is configured as an input and is controlled by PB5 as programmed by jumper WI6D. The data lines to buffer U6 are programmed by jumpers W15A, W15C, Wl5E and Wl5G to be PA0 through PA7. The data lines to buffer U7 are programmed by jumpers W15B, Wl5D, W15F and Wl5H to be PA0 through PA7. Although buffer U7 is programmed and controlled in a manner similar to the other buffers, it is not used on the Column Status PIA Assembly and is provided only to permit PIA Assembly interchangeability.

Integrated circuits U 2 through U6 read the Column Status data from the column indicator harness of the matrix. Similar integrated circuits on the Row Status PIA Assembly interface to the row indicator harness of the matrix. When a transmitter to antenna connection exists on the matrix, the Row Status (indicator) line will be switched to the Column Status (indicator) line at that particular crosspoint. Thus, the Column Status PIA Assembly will input an active low signal on the corresponding Column Status line when the Row Status PIA Assembly takes the corresponding Row Status line active low. As the MCU-8 performs a read of the indicator harness to determine the matrix status, the row status lines are sequentially taken to an active low state. While a given Row Status line is active, the Column Status PIA Assembly reads the Column Status lines for all active columns. The data read from these column status lines thus indicate the column connected to the subject row. A fault condition where multiple columns have been switched to the same row is detected since more than one Column Status line will be in the active low state for a given row.

Resistors Rl through R6 insure that the buffers U2 through U7 start up in a high-impedance mode prior to initialization of $U l$ and subsequent processor control of the high-impedance mode. Pull-up resistor networks U8 through Ul2 provide bias for the Column Status lines.

Connector Jl of the Column Status PIA Assembly connects to rear panel connector J5 using a 50 -conductor ribbon cable assembly, W3B.

### 3.5.12 Interlock Status PIA Assembly

The Interlock Status PIA Assembly, reference designation A9C, provides the interface between the MCU-8 and the interlock status circuits of the Model SLS Switch. This PIA Assembly is used for a large matrix with seventeen to forty interlock status circuits. This assembly inputs the interlock status signals corresponding to transmitters 1 through 40.

With reference to Figure 8-15, D33-299-5, Interlock Status Peripheral Interface Assembly Schematic Diagram, integrated circuit Ul is a peripheral interface adapter which interfaces the processor data lines to the CMOS/TTL level converter/buffer integrated circuits U2 through U7. Integrated circuit Ul provides two 8-bit bidirectional peripheral data buses, PA0 through PA7 and PB0 through PB7, and four control lines, CAl, CA2, CB1 and CB2. The 8-bit data bus, PA0 through PA7, is used to read from the buffers the interlock status data. The 8-bit data bus, PB0 through PB7, is used as a control signal bus that enables buffers U2, U3, U4, U5, U6 or U7. Control lines CA1, CA2, CBl and CB2 are not used.

The functional configuration of Ul is programmed by the processor through the data bus. At system initialization, the PA data lines are programmed as inputs and the PB data lines are programmed as outputs.

Integrated circuits U 2 through U 7 are 8 -bit bidirectional CMOS $/ T T L$ level converters. They provide conversion of the TTL logic level outputs of Ul to the 12 Volt CMOS logic levels of the interlock status circuits. Their bidirectional feature provides the reverse function of 12 Volt CMOS level conversion to TTL level inputs to U1. A third high-impedance (tristate) mode permits the PA data lines of $U l$ to be bused to multiple buffers, functioning as either input or output buffers, without bus contention.

The three operating modes of the level converting integrated circuits are established by the state of the enable input and the disable input. Once a buffer is dedicated as either an input or an output, it can be toggled between the active mode and the high-impedance mode by controlling the enable input for output buffers or the disable input for input buffers. The configuration of U 2 through U 7 is established by jumpers W3 through W8, respectively. On the Interlock Status PIA Assembly, integrated circuit U2 is an input and is controlled by the PBO data line of Ul. In a similar manner, U3, U4, U5 and U6 are inputs and are controlled by data lines PB1, PB2, PB3 and PB4, respectively. Buffer U7 is configured as an input and is controlled by PB5 as programmed by jumper W16D. The data lines to buffer U6 are programmed by jumpers W15A, WI5C, WI5E and W15G to be PAO through PA7. The data lines to buffer $\mathrm{U7}$ are programmed by jumpers W15B, W15D, W15F and W15H to be PA0 through PA7. Although buffer U7 is
programmed and controlled in a manner similar to the other buffers, it is not used on the Interlock Status PIA Assembly and is provided only to permit PIA Assembly interchangeability.

Integrated circuits U2 through U6 read the Interlock Status data from the Model IIK or Model IIK/DL Interlock Isolation Assemblies. The relays of each Interlock Isolation Assembly provide a contact closure to a common for each valid interlock circuit. These contact closures are monitored by U 2 through U 6 with U 2 reading the Interlock Status lines corresponding to transmitters 1 through 8 , U4 reading the lines corresponding to transmitters 9 through 16 , U6 reading the lines corresponding to transmitters 17 through 24 , U3 reading the lines corresponding to transmitters 25 through 32 and U 5 reading the lines corresponding to transmitters 33 through 40 .

Resistors R1 through R6 insure that the buffers U2 through U7 start up in a high-impedance mode prior to initialization of Ul and subsequent processor control of the high-impedance mode. Pull-up resistor networks U8 through Ul2 provide bias for the Interlock Status lines.

Connector Jl of the Interlock Status PIA Assembly connects to rear panel connector $J 6$ using a 50 -conductor ribbon cable assembly, W2C.

### 3.5.13 Video Display Unit

The Video Display Unit, reference designation Al, provides the matrix status display and the command entry status display. The matrix status display is either a schematic diagram of the RF paths through the matrix or a tabular listing of the transmitter and antenna connections for up to a 16 row by 16 column matrix. For a matrix larger than 16 rows by 16 columns, the matrix status display is the tabular listing of the transmitter and antenna connections. For both the Local and Remote operational modes, the command entry status is displayed on the bottom line referred to as the data line of the video display.

The Video Display Unit (VDU) is a 9-inch CRT manufactured by Motorola, Inc., Part Number M2000-355. The VDU receives the video signals corresponding to the contents of the video memory, the vertical sync and the horizontal drive from the Video Assembly via a 10-pin card-edge connector AlP1. Although the monitor will operate satisfactorily with only the composite signal, the separate vertical and horizontal syncs result in improved display linearity. Thus, on the signal circuit card jumpers JUl and JU2 are installed in the TTL position to enable TTL level input of the vertical sync and horizontal sync.

Complete specifications, theory of operation and maintenance details for the VDU are provided in the Service Manual for the M2000 Series Video Display Unit included as Appendix A to this Technical Manual.

## INSTALLATION

### 4.1 INSPECTION


#### Abstract

CAUTION The Matrix Control Unit contains parts and assemblies sensitive to damage by Electrostatic Discharge (ESD). Use ESD precautionary procedures when touching, removing or inserting parts and assemblies in the MCU-8.


## CAUTION

The Microprocessor Assembly, the Video Menory Assembly and the batteries should not be removed from their respective sockets. Should any of these components be removed during inspection or be improperly seated as a result of shipment, the data stored in the nonvolatile memories of the Microprocessor Assembly and/or the Video Memory Assembly will be lost. This data must then be reloaded as described in Section 5, Operation. Check the batteries as described in Section 4.7 for proper minimum voltage upon installation and at six month intervals thereafter.
4.1.1 After receiving the MCU-8 system, unpack all components and inspect carefully for any damage that may have occurred in shipment. Remove the top cover of the MCU-8 unit and verify that all circuit board assemblies and the rear panel mounted batteries are properly seated. The diagnostic switches, S5 through S10, located on the chassis behind the CRT assembly should all be in the off position (toggle toward rear panel).
4.1.2 Conduct the initial system tests described in Section 4.7 prior to final installation of the MCU-8 and ancillary equipment.

### 4.2 MECHANICAL

The Model MCU-8 Matrix Control Unit mounts in a standard 19" wide equipment rack and occupies $10-1 / 2^{\prime \prime}$ of vertical panel space. The Matrix Control Unit provides for mounting with customer furnished slides, Jonathan Mfg. Company Part Number ll0QDP22-2, to facilitate access to the equipment for maintenance.

### 4.3 AC POWER CONNECTIONS

The AC power cord connects to the $120 / 220 / 240 \mathrm{VAC}, 50 / 60 \mathrm{~Hz}$ main power.

## CAUTION

Unless otherwise noted by a rear panel label, the unit is supplied wired for 120 VAC operation. The connections to the power transformer must be changed to either the 220 VAC or the 240 VAC circuits as shown in the Power Supply Assembly Schematic Diagram, Figure 8-5, prior to applying 220/240 VAC. The primary power fuse should be changed to 0.5 A Slo-Blo for $220 / 240$ VAC operation.

The AC power cable connects to the $120 / 220 / 240 \mathrm{VAC}, 50 / 60 \mathrm{~Hz}$ main power. The detachable power cord supplied with the MCU-8 is fitted with a standard North American male connector and an IEC female connector. Standard color codes for the individual conductors are brown = line, blue = neutral and green/yellow = ground. Alternate conductor codings are black = line, white $=$ neutral and green $=$ ground.

### 4.4 INDICATOR, INTERLOCK AND ACTUATOR CONTROL CABLE CONNECTIONS

4.4.1 The MCU-8 connects to the Strip Line Switch and to the Actuator Interface Units of the switch with five multiconductor overall shielded cable assemblies. These cable assemblies are normally supplied cut to a customer's specified length and terminated with mating connectors since the connectors are an insulation displacement type. When supplied in this manner, the five cables are wired identically and the fifty pins of each connector are wired completely. Installation consists of connecting the cable assemblies to the MCU-8 and to the SLS-4M and AIU as described in Sections 4.4.5 through 4.4.9. The MCU-8 provides a No. 6-32 ground stud for connection of the cable shields on these cable assemblies. The assembly corments in Section 4.4.4, the pin assignment tabulations of Figures 4-1 through 4-5 and the wire color code tabulation of Figure 4-6 are provided for reference.
4.4.2 When installation requirements preclude factory assembly of these cables, they are supplied with one connector installed and the cable cut to the specified length. The end with the connector installed connects to the MCU-8 since the cable shield is terminated with a pigtail for connection to the MCU-8 ground stud. The other end of the cable is prepared for assembly to the insulation displacement connector supplied loose. For field installation of the connector, the Type. Sl-1 Palm Grip Hand Tool by Amp, Inc., Part Number $229764-2$ is recormended. Installation consists of completing each cable assembly by installing the loose connector with reference to the comments in Section 4.4.4 and connecting each cable assembly to the MCU-8 and to the SLS-4M and AIU as described in Sections 4.4.5 through 4.4.9.
4.4.3 When the interconnecting cable assemblies are provided and installed by the customer, insulation displacement connectors, Amp Part Number 229974-1, and twenty-five pair overall shielded cable, Belden Part Number 9525, are recommended. An alternate cable may be used with these connectors provided it consists of Number 24 AWG stranded wire with an individual conductor outer diameter including insulation of 0.045 inches or less. The overall shield drain wire should be terminated with a pigtail and connected to the MCU-8 ground stud. Installation consists of assembling the
cables with reference to the comments in Section 4.4.4 and connecting the cable assemblies to the MCU-8 and to the SLS-4M and AIU as described in Sections 4.4.5 through 4.4.9.
4.4.4 The MCU-8 and the SLS-4M/AIU are wired so that the two ends of the interconnecting cable connect to identically numbered pins. Figures 4-1 through 4-5 tabulate the functions of the connector pins utilized in these interconnecting cables and Figure $4-6$ provides a wire color code based on Belden Cable, Part Number 9525, for each connector pin. For matrices smaller than the 40 row and 40 column configuration provided by these cables, only the Row Select, Column Select, Row Status, Column Status and TX Interlock Status pins corresponding to the actual number of rows and columns need be connected. The +12 VDC circuit, the GND circuit, the Matrix Enable circuit and the Power Supply Status circuits must be connected as tabulated in Figures 4-1 through 4-5. The color code tabulation of Figure 4-6 details the wire color and the wire pair color for each connector pin. For example, the color code $2 / 2-6$ for connector pin number 1 defines the red wire of the red-blue pair.

### 4.4.5 Row Select (Address) Cable

The Row Select control cable which provides row actuator control functions connects to connector J2 of the MCU-8 and connector J3 of the Row Driver AIU. Figure 4-1 tabulates the function of the connector pins utilized in this cable.

### 4.4.6 Column Select (Address) Cable

The Column Select control cable which provides column actuator control functions connects to connector J3 of the MCU-8 and connector J3 of the Column Driver AIU. Figure 4-2 tabulates the function of the connector pins utilized in this cable.

### 4.4.7 Row Status Cable

The Row Status control cable which provides row indicator status functions connects to connector J4 of the MCU-8 and connector Jl of the SLS-4M. Figure 4-3 tabulates the function of the connector pins utilized in this cable.

### 4.4.8 Column Status Cable

The Column Status control cable which provides column indicator status functions connects to connector J5 of the MCU-8 and connector J2 of the SLS-4M. Figure 4-4 tabulates the function of the connector pins utilized in this cable.

### 4.4.9 Transmitter Interlock Status Cable

The Transmitter Interlock Status control cable which provides transmitter interlock status functions connects to connector J6 of the MCU-8 and connector J6 of the SLS-4M. Figure 4-5 tabulates the function of the connector pins utilized in this cable.

| Pin No. | Function | Pin <br> No. | Function |
| :---: | :---: | :---: | :---: |
| 1 | Row A Select | 26 | Row AA Select |
| 2 | Row B Select | 27 | Row BB Select |
| 3 | Row C Select | 28 | Row CC Select |
| 4 | Row D Select | 29 | Row DD Select |
| 5 | Row E Select | 30 | Row EE Select |
| 6 | Row F Select | 31 | Row FF Select |
| 7 | Row G Select | 32 | Row GG Select |
| 8 | Row H Select | 33 | Row HH Select |
| 9 | Row J Select | 34 | Row JJ Select |
| 10 | Row K Select | 35 | Row KK Select |
| 11 | Row L Select | 36 | Row LL Select |
| 12 | Row M Select | 37 | Row MM Select |
| 13 | Row N Select | 38 | Row nn Select |
| 14 | Row P Select | 39 | Row PP Select |
| 15 | Row Q Select | 40 | Row QQ Select |
| 16 | Row R Select | 41 | Row RR Select |
| 17 | Row S Select | 42 |  |
| 18 | Row T Select | 43 |  |
| 19 | Row U Select | 44 |  |
| 20 | Row V Select | 45 |  |
| 21 | Row W Select | 46 |  |
| 22 | Row X Select | 47 | Phase One MX Enable |
| 23 | Row Y Select | 48 | Phase Two MX Enable |
| 24 | Row Z Select | 49 |  |
| 25 | GND | 50 | +12 VDC |
| FIGURE 4-1 |  |  |  |


| Pin |  | Pin |  |
| :---: | :---: | :---: | :---: |
| No. | Function | No. | Function |
| 1 | Col 1 Select | 26 | Col 25 Select |
| 2 | Col 2 Select | 27 | Col 26 Select |
| 3 | Col 3 Select | 28 | Col 27 Select |
| 4 | Col 4 Select | 29 | Col 28 Select |
| 5 | Col 5 Select | 30 | Col 29 Select |
| 6 | Col 6 Select | 31 | Col 30 Select |
| 7 | Col 7 Select | 32 | Col 31 Select |
| 8 | Col 8 Select | 33 | Col 32 Select |
| 9 | Col 9 Select | 34 | Col 33 Select |
| 10 | Col 10 Select | 35 | Col 34 Select |
| 11 | Col 11 Select | 36 | Col 35 Select |
| 12 | Col 12 Select | 37 | Col 36 Select |
| 13 | Col 13 Select | 38 | Col 37 Select |
| 14 | Col 14 Select | 39 | Col 38 Select |
| 15 | Col 15 Select | 40 | Col 39 Select |
| 16 | Col 16 Select | 41 | Col 40 Select |
| 17 | Col 17 Select | 42 | +50 Reg. P. S. Stat |
| 18 | Col 18 Select | 43 |  |
| 19 | Col 19 Select | 44 |  |
| 20 | Col 20 Select | 45 |  |
| 21 | Col 21 Select | 46 |  |
| 22 | Col 22 Select | 47 |  |
| 23 | Col 23 Select | 48 |  |
| 24 | Col 24 Select | 49 |  |
| 25 | GND | 50 | +12 VDC |
| FIGURE 4-2 |  |  |  |
| MCU-8 CONNECTOR J3 TABULATION |  |  |  |


| Pin |  |  |  |
| :---: | :---: | :---: | :---: |
| No. | Function | No. | Function |
| 1 | Row A Status | 26 | Row AA Status |
| 2 | Row B Status | 27 | Row BB Status |
| 3 | Row C Status | 28 | Row CC Status |
| 4 | Row D Status | 29 | Row DD Status |
| 5 | Row E Status | 30 | Row EE Status |
| 6 | Row F Status | 31 | Row FF Status |
| 7 | Row G Status | 32 | Row GG Status |
| 8 | Row H Status | 33 | Row HH Status |
| 9 | Row J Status | 34 | Row JJ Status |
| 10 | Row K Status | 35 | Row KK Status |
| 11 | Row L Status | 36 | Row LL Status |
| 12 | Row M Status | 37 | Row MM Status |
| 13 | Row N Status | 38 | Row NN Status |
| 14 | Row P Status | 39 | Row PP Status |
| 15 | Row 2 Status | 40 | Row QQ Status |
| 16 | Row R Status | 41 | Row RR Status |
| 17 | Row S Status | 42 |  |
| 18 | Row T Status | 43 |  |
| 19 | Row U Status | 44 |  |
| 20 | Row V Status | 45 |  |
| 21 | Row W Status | 46 |  |
| 22 | Row X Status | 47 |  |
| 23 | Row Y Status | 48 |  |
| 24 | Row Z Status | 49 |  |
| 25 | GND | 50 | +12 VDC |
|  |  | E 4-3 |  |


|  |  |  |  |
| :---: | :---: | :---: | :---: |
| No. | Function | No. | Function |
| 1 | Col 1 Status | 26 | Col 25 Status |
| 2 | Col 2 Status | 27 | Col 26 Status |
| 3 | Col 3 Status | 28 | Col 27 Status |
| 4 | Col 4 Status | 29 | Col 28 Status |
| 5 | Col 5 Status | 30 | Col 29 Status |
| 6 | Col 6 Status | 31 | Col 30 Status |
| 7 | Col 7 Status | 32 | Col 31 Status |
| 8 | Col 8 Status | 33 | Col 32 Status |
| 9 | Col 9 Status | 34 | Col 33 Status |
| 10 | Col 10 Status | 35 | Col 34 Status |
| 11 | Col 11 Status | 36 | Col 35 Status |
| 12 | Col 12 Status | 37 | Col 36 Status |
| 13 | Col 13 Status | 38 | Col 37 Status |
| 14 | Col 14 Status | 39 | Col 38 Status |
| 15 | Col 15 Status | 40 | Col 39 Status |
| 16 | Col 16 Status | 41 | Col 40 Status |
| 17 | Col 17 Status | 42 |  |
| 18 | Col 18 Status | 43 |  |
| 19 | Col 19 Status | 44 |  |
| 20 | Col 20 Status | 45 |  |
| 21 | Col 21 Status | 46 |  |
| 22 | Col 22 Status | 47 |  |
| 23 | Col 23 Status | 48 |  |
| 24 | Col 24 Status | 49 |  |
| 25 | GND | 50 | +12 VDC |
|  |  | E 4-4 |  |



| $\begin{aligned} & \text { Connector } \\ & \text { Pin No. } \\ & \hline \end{aligned}$ | Wire Color $\qquad$ | Connector Pin No. | Wire Color $\qquad$ |
| :---: | :---: | :---: | :---: |
| 1 | 2/2-6 | 26 | 6/2-6 |
| 2 | 0/0-6 | 27 | 0/0-5 |
| 3 | 6/0-6 | 28 | 5/0-5 |
| 4 | 1/1-2 | 29 | 0/0-2 |
| 5 | 2/1-2 | 30 | 2/0-2 |
| 6 | 9/5-9 | 31 | 6/3-6 |
| 7 | 5/5-9 | 32 | 3/3-6 |
| 8 | 2/2-3 | 33 | 4/2-4 |
| 9 | 3/2-3 | 34 | 2/2-4 |
| 10 | 0/0-1 | 35 | 6/1-6 |
| 11 | 1/0-1 | 36 | 1/1-6 |
| 12 | 5/5-6 | 37 | 0/0-9 |
| 13 | 6/5-6 | 38 | 9/0-9 |
| 14 | 0/0-4 | 39 | 4/4-6 |
| 15 | 4/0-4 | 40 | 6/4-6 |
| 16 | 0/0-3 | 41 | 5/2-5 |
| 17 | 3/0-3 | 42 | 2/2-5 |
| 18 | 4/4-5 | 43 | 9/4-9 |
| 19 | 5/4-5 | 44 | 4/4-9 |
| 20 | 9/6-9 | 45 | 9/3-9 |
| 21 | 6/6-9 | 46 | 3/3-9 |
| 22 | 3/3-5 | 47 | 9/2-9 |
| 23 | 5/3-5 | 48 | 2/2-9 |
| 24 | 1/1-5 | 49 | 9/1-9 |
| 25 | 5/l-5 | 50 | 1/1-9 |

FIGURE 4-6
INTERFACE CABLE ASSEMBLY COLOR CODE

The MCU-8 Matrix Control Unit interfaces a standard data modem or the serial data bus of a customer's control system using connector Jl. This connector mates with a standard RS-232-C male connector (Part Number DB-25P, factory supplied). The following pins are used for serial data transmission and reception:

| $\frac{\text { Pin }}{1}$ | Function |
| :--- | :--- |
| 1 | Protective Ground (Connected to MCU-8 Chassis) |
| 2 | Transmitted Data (Data from MCU-8) |
| 3 | Received Data (Data to MCU-8) |
| 7 | Signal Ground |

Pin 8 of the MCU-8 connector, Jl, Received Line Signal Detector, is internally wired to +5 VDC for factory testing and should not be used by the customer.
4.6 MCU-8 CUSTOM FEATURE PROGRAMMING

CAUTION
The MCU-8 main power must be turned off before removing or installing any printed circuit assemblies.

## CAUTION

The Matrix Control Unit contains parts and assemblies sensitive to damage by Electrostatic Discharge (ESD). Use ESD precautionary procedures when touching, removing, or inserting parts and assemblies in the MCU-8.

## NOTE

All of the custom programming features are read by the MCU-8 microprocessor during the initialization program after a power-up or program reset. Thus, to effect any new programming features, the MCU-8 main power must be turned off and then turned on or the program Reset switch S5 momentarily operated. Any programming changes made with main power applied and without resetting the unit will not be implemented until the main power is recycled or the unit is reset.
4.6.1 The Serial Interface Assembly, Part Number D33-290-1, reference designation A6, provides for customer programing of the following features:
(1) $50 / 60 \mathrm{~Hz}$ Line Frequency for Video Sync
(2) MCU-8 Peripheral Address
(3) Serial Data Baud Rate
(4) Serial Data Parity Specification
(5) Serial Data Stop Bit Specification
(6) Active/Tristate Serial Output Circuit

The Serial Interface Assembly is the plug-in printed circuit assembly located directly behind the front panel mounted Keyboard Assembly. The ribbon cables connected to the Serial Interface Assembly provide sufficient slack so that the assembly may be unplugged from the Mother Board Assembly and installed on a 6-inch card extender without disconnecting the ribbon cables.

### 4.6.2 $\quad 50 / 60 \mathrm{~Hz}$ Line Frequency

The timing of the vertical sync signals to the video display is determined by jumper 68 on the Serial Interface Assembly. This timing may be changed to maintain synchronization of the video display when operating from either a 50 or 60 Hz line frequency. As supplied, the MCU-8 is configured to synchronize with a 60 Hz line frequency (jumper w8 installed). To maintain synchronization of the video display when operating with a 50 Hz line frequency, remove jumper W8.

### 4.6.3 MCU-8 Peripheral Address

The two digit MCU-8 Peripheral Address is determined by switches Sl and S2 on the Serial Interface Assembly. Switch Sl establishes the least significant digit (LSD) and switch 52 establishes the most significant digit (MSD). The switches provide hexadecimal addresses from "00" to "FF". The switches are set at the factory for an address of "31" (ASCII 1). The MCU-8 address may be modified by rotating the center selector of either S 1 or S 2 as required to select the new address digits.

### 4.6.4 Serial Data Baud Rate

The serial data baud rate is determined by switches S3 and S4 on the Serial Interface Assembly. Switch S3 establishes the receive baud rate and switch S 4 establishes the transmit baud rate. As tabulated below, these switches provide baud rates from 50 to 19200. The switches are set at the factory for a receive and transmit baud rate of 1200 . The baud rate may be modified by rotating the center selector of either S3 or S4 as required to select the new receive or transmit baud rate, respectively.

| S3, S4 <br> Position | Baud Rate |
| :---: | :---: |
|  |  |
| 1 | 50 |
| 2 | 75 |
| 3 | 110 |
| 4 | 134.5 |
| 5 | 150 |
| 6 | 300 |
| 7 | 600 |
|  | 1200 |

(Factory Setting)
F 19200

### 4.6.5 Serial Data Parity Specification

The serial data parity, either odd or even, is determined by jumper w6 on the Serial Interface Assembly. With the jumper installed, the parity is even and with the jumper removed, the parity is odd. As supplied, the MCU-8 is programmed for even parity (jumper $W 6$ installed). To program the MCU-8 for odd parity, remove jumper $W 6$.

### 4.6.6 Serial Data Stop Bit Specification

The number of stop bits per character, either one or two, is determined by jumper $W 7$ on the Serial Interface Assembly. With jumper W7 installed, the number of stop bits per character is one. With jumper W7 removed, the number of stop bits per character is two. As supplied, the MCU-8 is programed for one stop bit per character (jumper W7 installed). To program the MCU-8 for two stop bits per character, remove jumper W7.

### 4.6.7 Active/Tristate Serial Output Circuit

The serial output circuit is configured for operation with either a dedicated line or a party line serial communication circuit using jumper w9 on the Serial Interface Assembly. With jumper $W 9$ installed, the serial output circuit remains active $(-6$ volt marking condition when not transmitting data) as required for a dedicated line communication circuit. With jumper W9 removed, the serial output circuit is normally high-impedance (tristate) and is switched to an active mode only when the MCU-8 transmits serial data as required for a party line communication circuit. As supplied, the MCU-8 is configured for an active serial output circuit (jumper W9 installed). Note that jumper W9 should remain installed unless operation with a party line communication circuit.

### 4.7 INITIAL SYSTEM TESTS

4.7.1 After installation per the above instructions, verify as described in Section 6.1 the back-up battery voltage that protects the nonvolatile memory. A rear panel label indicates the "factory installation" date and provides space for a user date stamp indicating battery voltage verification at installation. If the batteries require replacement, the MCU-8 main power must be on to preserve the contents of the random access memories.
4.7.2 First test the MCU-8 Unit for proper Local mode operation. For these Local mode tests, energize the Interlock Isolation Assembly of the SLS-4M but do not energize the matrix power supply which is controlled by the power switch on the AIU. The MCU-8 display should show the matrix crosspoint
and interlock status (reference Section 5.3.2). Check for proper status indication when circuits are established by manual operation of the crosspoints.
4.7.3 Then turn on the matrix power supply using the AIU power switch and check the motorized crosspoint operation using keypad entered selections per Section 5.3.5. Also check the Local Unit for proper operation of the busy protect, lockout protect, lockout update and lockout display features.
4.7.4 Upon verification of Local mode operation, interface the MCU-8 to the data modem or the serial data bus of the control system and verify the Remote mode operational features. Place the Local/Remote switch in the Remote position and check for display of "RMT" in the upper right-hand corner of the video display. Transmit connect commands, disconnect commands and status cormands to the MCU-8 and verify correct matrix operation and status responses.

### 5.1 GENERAL

The Model MCU-8 Matrix Control Unit provides actuator control and status display of the Strip Line Switch. The motorized crosspoints of the switch are controlled by the MCU-8 using keypad entered commands in the Local mode. In the Remote mode, the Local Unit receives control and status commands over a serial data bus from the control system, establishes the desired matrix switching and transmits a status response. This section describes the front panel components, the operational procedures for both Local and Remote operation, and the control and status word formats for Remote operation.

### 5.2 DESCRIPTION OF FRONT PANEL COMPONENTS

### 5.2.1 Main Power Switch

This switch controls the application of AC power to the unit. The switch is an alternate action, push-on/push-off illuminated control. When AC power is applied, the switch is illuminated.

### 5.2.2 Video Power Switch

This switch controls the application of $D C$ power to the video display. The switch is illuminated when the video display is energized. When local display of the switch status is not required, the video display may be turned off with no effect on the control and interface features of the MCU-8.

### 5.2.3 Brightness Control

This control adjusts the brightness of the video display. Clockwise rotation increases the display brightness. The display brightness should be adjusted to provide a clean and legible display without blooming.

### 5.2.4 Local/Remote Switch

This keylock switch determines the operational mode of the Matrix Control Unit. When placed in the Local position, the MCU-8 assumes control of the Strip Line Switch and does not respond to control commands from the remote control system. In the Local mode, the MCU-8 responds to status commands from the remote control system unless the keypad is active or a matrix enable and confirm sequence is in progress. When placed in the Remote position, the MCU-8 controls the matrix switching as commanded by the remote control system and does not respond to local keypad entered commands. The operational mode of the MCU-8 is indicated in the upper right-hand corner of the video display by "LCL" for the Local mode and "RMT" for the Remote mode.

### 5.3.1 Initiation

5.3.1.1 Local mode operation of the MCU-8 is initiated by placing the Local/Remote switch in the Local position. Check for display of "LCL" in the upper right-hand corner of the video display to verify Local mode operation.
5.3.1.2 The MCU-8 Unit may be used in the Local mode regardless of the connection of a remote control system. When in the Remote mode, the keypad is disabled and messages from the remote control system are serviced. When in the Local mode, status commands from the remote control system are serviced unless the keypad is active or a matrix enable and confirm sequence is in progress.
5.3.2 Video Display
5.3.2.1 The status of the Strip Line Switch is presented as a tabulation of antennas connected to transmitters, listed by transmitter number and as a cross-tabulation of transmitters connected to antennas, listed by antenna number. A valid RF circuit is indicated by the number of the antenna connected to the subject transmitter displayed next to the transmitter number in the transmitter tabulation and by the number of the transmitter connected to the subject antenna displayed next to the antenna number in the antenna tabulation. A valid interlock closure for the associated transmitter is indicated by an asterisk adjacent to the transmitter number, whereas an open interlock circuit is indicated by an "I" adjacent to the transmitter number. The asterisk adjacent to the antenna number confirms that the antenna is in use; that is, connected to a transmitter. The display of an " F " next to the transmitter number or the antenna number indicates a switching fault. The switching fault display indicates a crosspoint in the Turn position in the same row or column as some other crosspoint that is in the Turn position, and thus an invalid switch combination exists. The reverse video lockout code that is displayed next to an antenna number after a transmitter has been selected indicates an antenna that is not available to the specified transmitter. The "locked out" antenna may be not available for a number of reasons, including a manual switching operation being required, incompatible transmitter/antenna power levels, or the antenna or crosspoint being down for maintenance.
5.3.2.2 The subject Model SLS-4M (20 X 21) Strip Line Switch provides antenna grounding capability using the top row, Row A. The MCU-8 automatically grounds all antenna columns by connecting the antenna column to Row A. Upon a power or reset of the MCU-8 or upon operation of a motorized crosspoint, the MCU-8 checks all unused antennas for the ground row connection and automatically grounds the unused antennas if they are not connected to a transmitter. Any antenna grounded to Row A is indicated by a "G" in the antenna tabulation adjacent to the antenna number. If $a$ malfunction occurs and the unused antenna is not grounded to Row A, a ** GROUND ROW FAULT ** message will be displayed below the matrix tabulation. Since Row A on the switch provides the antenna ground function, then the first transmitter input to the switch is Row B. Thus, the TX 01 control and status display functions correspond to Row B of the switch. In
a similar manner, TX 02 functions correspond to ROW C, TX 03 functions correspond to Row D, and so forth through TX 20 functions which correspond to Row $W$ of the switch.

### 5.3.3 Display Mode Selection

Because the subject Model MCU-8 provides only the matrix status tabular summary display, the display mode selection key, the "D" key on the front panel keypad, is not enabled on the subject MCU-8.

### 5.3.4 Matrix Selection

Because the subject Model MCU-8 provides actuator control and status display of a single matrix, the specification of a matrix for a switching operation is not required, thus, the Matrix key of the front panel keypad is not enabled on the subject MCU-8.

### 5.3.5 Transmitter/Antenna Selection

5.3.5.1 A transmitter selection is initiated by depressing the Transmitter key on the keypad. The MCU-8 will acknowledge this by displaying a "T" on the video display bottom line referred to as the data line. The transmitter is entered as a two digit number. For example, to select transmitter number one, enter " 0 ", then " 1 ". To select transmitter number twelve, enter " 1 ", then "2". The MCU-8 will display the specified transmitter number on the data line. The specified transmitter will also be highlighted by a reverse video display of its number on the tabular display. Should the transmitter be connected to an antenna, the display will indicate in brackets the letters "BA" and the antenna number connected to the specified transmitter. "BA" means the selected transmitter is busy or in use with an antenna. The antennas not available to the selected transmitter will be indicated by a reverse video lockout code (reference Section 5.3.7) adjacent to each inaccessible antenna number.

## NOIE

After entering the keypad command entry mode, the unit will automatically "time-out" and revert to the normal mode if another key is not depressed in approximately 15 seconds.
5.3.5.2 The antenna to be connected is then selected by depressing the Antenna button on the keypad followed by the two digit antenna number. The MCU-8 will display an " $A$ " on the data line followed by the antenna number. The specified antenna will also be highlighted by a reverse video display of its number on the tabular display. Should the antenna be presently connected to another transmitter, the display will indicate in brackets the letters "BT" and the transmitter number connected to the specified antenna. "BT" means the selected antenna is busy with a transmitter. This is followed by "BPE" for busy protect enabled. Switching of a busy antenna is prohibited unless the antenna is first cleared or the "Busy Protect Override" feature is implemented as detailed in Section 5.3.5.4.
5.3.5.3 If the specified antenna is not busy or locked out, switching of the specified antenna to the specified transmitter occurs upon operation of the Enable button on the keypad. The MCU-8 displays the phrase "MX EN" on the data line to indicate that the matrix has been enabled. Confirmation of the desired switching is indicated by an update of the tabular presentation and by displaying the word "CONFIRM" on the data line. If switching as specified does not occur, the word "FAULT" is displayed on the data line. If the specified switching does not occur due to a power supply failure, the defective power supply is displayed on the data line as "PSI FLT".
5.3.5.4 If the specified antenna is busy, the antenna must first be cleared or the "Busy Protect Override" option used. An antenna may be cleared by operating the Transmitter button, entering the associated transmitter number, followed by operating the Antenna button and entering the two digit antenna number " 00 ". Operating the Enable button will then clear the busy antenna. Optionally, operating the "C" key will override the busy protect circuit as indicated by the phrase "BPO" on the data line. The specified transmitter and antenna may now be connected by operating the Enable button as previously described.

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This method will result in disconnecting the antenna from the previously assigned transmitter; and thus, may disrupt an existing circuit.
5.3.5.5 If the specified antenna is locked out, switching of the specified antenna to the specified transmitter will not occur. The display will indicate in brackets the letters "LO ST" and the lockout status code defining the reason the antenna is not available to the transmitter (reference Section 5.3.7.2 for lockout status code definitions). The antenna selection must be aborted and a new accessible antenna selected.
5.3.5.6 When entering transmitter and antenna designations from the keypad, the following constraints apply:
(1) A transmitter designation of "00" will not be accepted in the transmitter/antenna selection routines. The transmitter designation of "00" is allowed only in the lockout memory display routine to access the antenna ground row lockout codes.
(2) A transmitter number or an antenna number greater than the actual number of transmitters or antennas will not be accepted.
(3) Once an antenna has been connected to a transmitter, a new antenna may be specified by operating the Antenna button and by entering the new antenna number. The transmitter number does not need to be respecified unless changing the transmitter.
(4) Because two digits are required to specify a transmitter or an antenna, if an error is made on entering the first digit, a second digit must be entered before reoperating the Transmitter or Antenna button to clear the error.
(5) Recognition of changing the Local/Remote switch from the Local to Remote will not occur if the switch is changed after the Transmitter or Antenna button has been operated and before the selection is completed. If such change occurs, complete the transmitter or antenna selection and then depress either the Transmitter or Antenna button. Recognition of the Local/Remote mode is verified by display of "LCL" or "RMT" in the upper right-hand corner of the display.
(6) If a keypad selection sequence is interrupted and approximately 15 seconds elapse between key depressions, the MCU-8 clears the data line on the video display, clears all files associated with the current transmitter and antenna selection, and reverts to normal operation. This "time-out" feature ensures the continued processing of matrix status updates and remote status requests in the event that the keypad selection is inadvertently interrupted.

### 5.3.6 Automatic Antenna Grounding Feature

As described in Section 5.3.2.2, the MCU-8 grounds all unused antenna columns by connecting the antenna to the antenna ground row, Row A. During the switching of a selected transmitter and antenna crosspoint, the grounded antenna is first cleared and then connected to the specified transmitter. If an antenna is cleared as the result of connecting another antenna to a transmitter, the MCU-8 automatically grounds the cleared antenna by connecting it to Row A.

### 5.3.7 Lockout Memory Operation

5.3.7.1 The operational status of all crosspoints on the Strip Line Switch is stored by the MCU-8 in a special memory termed the lockout memory. Each crosspoint is defined by its operational status, i.e., motorized, manual, not available, not equipped, and is represented by a single digit code in the lockout memory. The MCU-8 uses this memory to determine if an antenna is accessible by a specified transmitter and displays inaccessible antennas with the solid block format reverse video character previously described.
5.3.7.2 While in the Local mode, the contents of the lockout memory for a particular transmitter may be displayed by operating the "F" key. A summary of the lockout code definitions appears on the line above the data line. After specifying a transmitter, the lockout codes for all crosspoints not motorized or operational for that transmitter will appear adjacent to their associated antenna number. The lockout code definitions are as follows:

| Code | Abbreviation | Definitions |
| :---: | :---: | :---: |
| 0 | MTZ | Motorized Crosspoint |
| 1 | MNL | Manual Crosspoint |
| 2 | LCK | Locked Crosspoint (Crosspoint locked in Thru position to prevent connection of high power transmitter and low power antenna) |
| 3 | NAV | Crosspoint Not Available (Customer definable, may be used to inđicate antenna down for maintenance, etc.) |
| 4 | NEQ | Crosspoint Not Equipped (A blank crosspoint provided for expansion) |

Because the "F" key operates as a toggle switch, depressing the "F" key with the lockout memory displayed will revert the display to the previous display mode.
5.3.7.3 Should the operational configuration of the matrix change such as by converting a manual crosspoint to a motorized crosspoint, the lockout code associated with a crosspoint may be changed using the keypad in much the same manner as connecting a transmitter to an antenna. First, depress the "F" key to access the lockout memory display. Operate the Transmitter key and enter the two character transmitter number. The lockout code will appear adjacent to each inaccessible antenna number. Operate the Antenna key and enter the two digit antenna number. At this point, the data line displays the standard transmitter and antenna designation and the lockout code in brackets with the letters "LO ST" for the specified crosspoint. To change the code, depress the " E " key and enter the number from 0 to 4 corresponding to the desired lockout condition. The lockout memory display updates immediately. Codes for additional crosspoints are entered by specifying a new antenna number if the same transmitter is used or by specifying new transmitter and antenna numbers if a different transmitter is required.
5.3.7.4 The lockout memory data is stored in the random access memory of the MCU-8. This memory is nonvolatile as long as the Video Memory Assembly is installed in the Mother Board Assembly. Should this assembly be removed, the back-up batteries are disconnected and the memory contents are lost. Since the memory will power-up with random numbers not corresponding to valid codes, the lockout memory must be reloaded either from the keypad or by using the reload feature described in Section 5.3 .9 before the MCU-8 can control the Strip Line Switch. The lockout memory is programmed at the factory and protected by batteries during shipment and installation. It is recommended that the lockout data be recorded by the customer and saved for reference purposes.
5.3.7.5 Access the lockout memory assignments for the antenna ground row in the lockout memory display routine by depressing the Transmitter key on the keypad and entering transmitter number " 00 ". The data line will display "GND" in place of the transmitter number and the lockout codes will appear adjacent to each manual antenna ground row crosspoint. Operate the Antenna key and enter the two digit antenna number. At this point the data line displays GND, the antenna number, and the lockout code in brackets with the letters "LO ST" for the specified crosspoint. To change the code, depress the "E" key and enter the number from 0 to 4 corresponding to the desired lockout condition. The MCU-8 program checks the lockout code of the antenna ground row crosspoints during the automatic antenna grounding program sequence. A lockout code of " 0 " or " 1 " instructs the MCU-8 to operate the crosspoint to ground the antenna and to display the ** GROUND ROW FAULT ** message if not successful. A lockout code of "2", "3" or "4" instructs the MCU-8 to not operate the crosspoint, thereby not grounding the antenna. The lockout code of "2", "3" or "4" also prevents the display of the ** GROUND ROW FAULT ** message. The lockout code "0" or "l" should be used for all antenna ports which require grounding when not connected to an antenna. The lockout codes "2", "3" or "4" may be used for switch outputs which do not require grounding such as a dummy load output or trunk output.
5.3.7.6 Reload the lockout memory to the original factory set lockout status by using diagnostic switch S 8 as described in Section 5.3.9.
5.3.7.7 The lockout protect feature may be defeated in its entirety by using diagnostic switch 57 as described in Section 5.3.9.

### 5.3.8 Multiple Turn Faults

5.3.8.1 The matrix display shows an "F" fault indicator when any crosspoint is set in the Turn position but is not providing an effective RF circuit because another Turn crosspoint is nearer to either the input or output connector. The multiple turn fault condition is indicated by the "F" fault indicator to the right of the transmitter number and interlock indicator corresponding to the faulty circuit. The "F" fault indicator also is displayed to the right of the antenna number corresponding to the faulty circuit if the antenna is not in use with another transmitter. This fault display warns the operator that one or more crosspoints did not properly clear to the Thru position when a selection was made, or a manual only crosspoint was left in the Turn position. A circuit may be established via such a fault crosspoint if the Turn crosspoint nearer the input or output connector is cleared. If the switch is equipped for automatic antenna grounding, multiple grounded antennas do not create multiple turn faults. Note that the " $F$ " fault indicator will be displayed if a crosspoint is in the Turn position and the associated antenna ground crosspoint is also in the Turn position instead of the required Thru position. The ** GROUND ROW FAULT ** message is displayed when an antenna ground crosspoint does not correctly operate to the Turn position.
5.3.8.2 When this type of fault occurs on a motorized module, a defective actuator, actuator connector or wiring harness is indicated. Until repair can be made, the faulty crosspoint should be manually set to the Thru position and the associated antenna locked out from the associated transmitter.

### 5.3.9 Special Function Switches

Six switches (S5-S10) are located on the chassis behind the CRT assembly (top cover removal provides access). These switches are normally off, i.e., toggle lever set toward the rear panel. The active or on position is established by switching the toggle lever toward the front panel. The functions of the switches for the Local Unit are as follows:

S5 - Performs a reset of the microprocessor which restarts the program from the beginning. A reset is provided automatically each time power is turned on. This switch is momentary action.

S6 - Performs a non-maskable interrupt which vectors to a subroutine to provide a video alignment pattern on the screen (all characters "+"). After adjustment of the CRT, controls return to normal by operating reset switch S 5 or depressing any button on the keypad. This switch is momentary action.

S7 - When on, the Lockout Protect feature is overridden and it is possible to operate any motorized crosspoint of the matrix. All lockout functions are disabled including display updating and clearing of lockout status. This switch is provided for use in case of failure of the nonvolatile memory on the video Memory Assembly. This switch is alternate action.

S8 - When on (with S7 off) provides for reloading the lockout status to the initial status programmed at the factory. To reload the lockout status, depress the "F" key (display lockout status), hold switch S 8 on and depress the "D" button. Then release switch S 8 to return it to the off position. This switch is momentary action.

S9 - Not assigned.
S10 - When on, the complete status response is displayed for diagnostic purposes (reference Section 5.6). An abbreviated version of the complete status message is displayed when switch is in off position. This switch is alternate action.

### 5.3.10 Shutdown Procedure

To shut down the MCU-8, depress the main power switch. Turning the MCU-8 off will not change any transmitter/antenna connections on the Strip Line Switch. With the MCU-8 shut down, the SLS-4 must be operated manually. For instructions on how to operate the switch manually, refer to the technical manual for the Model SLS-4 Strip Line Switch. When the MCU-8 is turned off, the remote control system cannot perform transmitter and antenna switching for the matrix and matrix status information will not be received.

### 5.3.11 Emergency Operating Instructions

To shut down the MCU-8 in an emergency, depress the main power switch. Shutting down the MCU-8 will not change any transmitter/antenna connections on the Strip Line Switch. With the MCU-8 shut down, the SLS-4 must be operated manually. For instructions on how to operate the switch manually, refer to the technical manual for the Model SLS-4 Strip Line Switch. When the MCU-8 is turned off, the remote control system cannot perform transmitter and antenna switching for the matrix and matrix status information will not be received.

### 5.4 REMOTE OPERATION

### 5.4.1 Initiation

Initiate remote mode operation of the MCU-8 system by placing the Local/Remote switch in the Remote position. Check for display of "RMT" in the upper right-hand corner of the video display to verify Remote mode operation. Switching from Local to Remote while specifying a transmitter to antenna connection from the keypad or after updating the lock-out memory will require operation of one of the major function keys, i.e., Transmitter or Antenna, before recognition of the Remote mode switch position occurs.

### 5.4.2 Remote Control

5.4.2.1 Prior to operating in the Remote mode, review the custom programming of the MCU-8 peripheral address, serial data baud rate, parity specification and stop bit specification in Section 4.6.
5.4.2.2 Remote operation involves the transmission of the actuator switching commands and matrix status commands to the MCU-8 by the customer's remote control system. The format of these commands is detailed in the following section. The MCU-8, operating in the Remote mode, will perform transmitter and antenna switching as specified in the control command and will respond to status commands with a message detailing the antenna connected to the specified transmitter, interlock status and power supply status. The MCU-8 operating in the Local mode will respond only to status commands and will not honor control commands.
5.4.2.3 As with local operation of the MCU-8, several constraints apply for remote operation:
(1) Transmitter numbers must be greater than zero and not exceed the maximum number of transmitters.
(2) Antenna numbers must not exceed the maximum number of antennas.
(3) All serial interface features as specified in Section 4.6 must be correct. Further, the number of data bits per character must be seven and the number of start bits must be one.
(4) Connect commands for transmitter and antenna connections will be recognized only if the lock-out code for that crosspoint is the valid motorized code unless the lockout protect feature is defeated using switch S7.
(5) After transmitting a connect or disconnect command to the MOU-8, approximately 1.2 seconds must elapse before a status request is transmitted to the MCU-8. This delay is required for the MCU-8 to initiate the switching command and for the actual switching of the selected crosspoint and antenna grounding to occur.
(6) After receiving a status command, a delay of approximately 300 msec. occurs before a status response is transmitted by the MCU-8.
5.4.2.5 The received connect, disconnect and status commands are displayed on the third line from the bottom line of the MCU-8 video display. The transmitted response to a status command is displayed to the right of the received command. With switch Slo off, an abbreviated version of the transmitted complete status response command is displayed to the right of the complete status conmand. With switch Sl0 on, the transmitted complete status response is displayed to the right of the complete status command using as many lines as necessary to display the full status response. Section 5.6 details the characteristics of the displayed messages.

### 5.5 CONTROL AND STATUS WORD FORMATS

The control and status words received and transmitted by the MCU-8 Unit follow the format detailed below. All characters are ASCII characters. Although shown below with spaces between characters for clarity, all messages are transmitted without intervening spaces.
A. Connect Command (Remote Control System to MCU-8) :

CR LF ADRS C T1 T2 Al A2 X
B. Disconnect Command (Remote Control System to MCU-8):

CR LF ADRS D Tl T2 X
C. Status Command (Remote Control System to MCU-8) :

CR LF ADRS S Tl T2 X
D. Status Response (MCU-8 to Remote Control System):

CR LF ADRS S Tl T2 Al A2 F M I PS ETB
E. Complete Status Command (Remote Control System to MCU-8):

CR LF ADRS S A L L X
F. Complete Status Response (MCU-8 to Remote Control System)

CR LF ADRS $S \mathrm{Tl}_{1} \mathrm{Tl}_{2}$ A1 A2 $\mathrm{I} 1 \mathrm{~T}_{2} \mathrm{I}_{\mathrm{T}} 2_{2} \mathrm{Al}$ A2 I 2
$T 31{ }^{T} 32$ A1 A2 $13 \mathrm{~T}_{1} \mathrm{~T}_{2}$ A1 A2 I 4
T 51 T 52 Al A2 $\mathrm{I} 5 \mathrm{~T} 61 \mathrm{~T} 6_{2}$ A1 A2 I6
$\mathrm{T} 71 \mathrm{~T}_{2}$ A1 A2 17 T 81 T 82 Al A2 I8
$\mathrm{T9} \mathrm{~T}_{1} \mathrm{~T} 92$ A1 A2 $\mathrm{I} 9 \mathrm{~T} 10_{1} \mathrm{~T} 10_{2}$ Al A2 Il0
$\mathrm{Tll}_{1} \mathrm{Tll}_{2}$ A1 A2 $\mathrm{Ill} \mathrm{Tl2} \mathrm{I}_{1} \mathrm{~T} 12_{2}$ A1 A2 I12
$\mathrm{Tl3} 1 \mathrm{Tl}_{2}$ A1 A2 $\mathrm{Il} 3 \mathrm{Tl4} 1 \mathrm{Tl4}_{2}$ Al A2 Il4
$\mathrm{Tl5} \mathrm{Tl}_{2}$ Al A2 $\mathrm{Il5} \mathrm{Tl} 6_{1} \mathrm{Tl} 6_{2}$ Al A2 Il6
$\mathrm{Tl7}_{1} \mathrm{Tl7}_{2}$ Al A2 $\mathrm{Il7} \mathrm{Tl} 8_{1} \mathrm{~T} 188_{2} \mathrm{Al}$ A2 Il 8
T191 T192 Al A2 $119 \mathrm{~T}_{2} 0_{1} \mathrm{~T} 20_{2}$ Al A2 I 20
F M PS ETB
The characters are defined as follows:
$C R=$ ASCII Carriage Return
$\mathrm{LF}=$ ASCII Line Feed
ADRS $=$ MCU-8 Address (Switch Selectable); Any ASCII character except CR, X or ETB (Factory set to ASCII 1)

C $=$ Command Sequence Designator for Connect Message
D = Cormand Sequence Designator for Disconnect Message
S $=$ Cormand Sequence Designator for Status Message
ALL $=$ ASCII Character String Meaning All Transmitters
$\mathrm{Tl}=$ Most Significant Digit of Transmitter Number
T2 = Least Significant Digit of Transmitter Number
Al $=$ Most Significant Digit of Antenna Number
A2 $=$ Least Significant Digit of Antenna Number
$\mathrm{Tl}_{1}=$ Most Significant Digit of Transmitters 1 through 20, thru respectively
$\mathrm{T} 20_{1}$
$\mathrm{Tl}_{2}=$ Least Significant Digit of Transmitter 1 through 20, thru respectively
$\mathrm{T}_{2} \mathrm{O}_{2}$
$\mathrm{F}=$ Fault Digit
$0=$ No Fault
1 = Summary Fault
3 = Connection Fault
5 = Automatic Grounding Fault
M $=$ Mode Digit
$0=$ Local Mode
$1=$ Remote Mode
I = Transmitter Interlock Status Digit
$0=$ Open Interlock
1 = Valid Interlock
Il = Transmitters 1 through 20 Interlock Status Digit, thru respectively

0 = Open Interlock
1 = Valid Interlock
PS = Matrix Power Supply Status Digit. For SLS-4M:
0 = Supply Fault
1 = Supply Normal
$\mathrm{X}=\mathrm{ASCII} \mathrm{X}$ to End Command Message
ETB $=$ ASCII End of Transmission Block to End Status Response
The Fault Digits are defined as follows:
$0=$ No Fault: The transmitter and antenna connection last requested was obtained.
$1=$ Summary Fault: This Summary Fault is set when an error occurs in the message transmitted to the MCU-8. If a Summary Fault occurs, the connect or disconnect command causing the fault is not executed. The following errors will set the Summary Fault:
(A) Connect or Disconnect Command Specification of $\mathrm{T} 1, \mathrm{~T} 2$ $=00$ or Connect Command with A1, $\mathrm{A} 2=00$.
(B) Connect or Disconnect Command Specification of T1, T2 greater than the maximum number of transmitters or A1, A2 greater than the maximum number of antennas.
(C) Connect Command for a crosspoint with a lockout code other than motorized unless switch $\mathrm{S7}$ is set to defeat Lockout Protection.
(D) Connect or Disconnect Command received when Local MCU-8 Unit is in Local mode.
(E) Parity, Framing or Receiver Overrun Error.
$3=$ Connection Fault: The transmitter and antenna connection requested was not obtained and Summary Fault did not occur.
$5=$ Automatic Grounding Fault: The control unit was unable to ground an unused antenna.

### 5.6 MESSAGE DISPLAY FORMAT

5.6.1 As noted in paragraph 5.4.2.5, the connect, disconnect and status commands, and the status responses are shown on the video display. The Video Assembly character generator provides standard characters for the 96 printable ASCII characters (letters, numbers, etc.). The character generator provides special characters for the 32 control characters of the ASCII code set. All ASCII characters are defined by seven bits, bits 0 through 6 . Figure 5-1, Character Generator Modified ASCII Codes, details the displayed character as a function of the character code, bits 0 through 3, the LSD, and bits 4 through 6, the MSD. The special characters for the 32 ASCII control characters are shown in the figure for an MSD of 0 or 1 . All characters in the subject control and status word formats are printable ASCII characters except the carriage return (CR), line feed (LF) and End of Transmission Block (ETB). The carriage return which is the first character of all transmissions has a hex value of "OD" and as shown in Figure 5-1, is displayed on the MCU-8 as " $\xi$ ". The line feed character, the second character of all transmissions, has a hex value of " 0 A " and is displayed as " $\equiv$ ". The end of transmission block character at the end of the transmitted status response has a hex value of "17" and is displayed as " $\dagger$ ". The following paragraphs detail the presentation on the video display of the connect, disconnect and status commands and the status response. Typical command messages and status response messages specifying TX 01 and ANT 01 operations are presented as illustrative examples. Refer to Section 5.5 for the definitions of the message characters. Although shown below with spaces between characters for clarity, all messages are transmitted without intervening spaces.

The connect command transmitted by the remote control system to the MCU-8 with an address of 1 to connect TX 01 to ANT 01 is displayed on the MCU-8 as follows:

$$
" \xi \equiv 1 \subset 0101 \mathrm{X} "
$$

### 5.6.3 Disconnect Command Format

The disconnect command transmitted by the remote control system to the MCU-8 with an address of 1 to disconnect the antenna connected to TX 01 is displayed on the MCU-8 as follows:
$" \xi \equiv 1 \mathrm{D} 01 \mathrm{X} "$
5.6.4 Status Command Format

The status command transmitted by the remote control system to the MCU-8 with an address of 1 to determine the status of TX 01 is displayed on the MCU-8 as follows:
$" \xi \equiv 1 \mathrm{SOLX}$

### 5.6.5 Status Response Format

The status response transmitted by the MCU-8 to the remote control system with an MCU-8 address of 1, TX 01 connected to ANT 01, no connect or summary faults, MCU-8 in the Remote mode, valid interlock closure for TX 01 and normal matrix power supply is displayed on the MCU-8 as follows:
" $\xi \equiv 1 \mathrm{~S} 01010111$ - "
5.6.6 Complete Status Command Format

The complete status command transmitted by the remote control system to the MOU-8 with an address of 1 to determine the status of all transmitters is displayed on the MCU-8 as follows:
" $\xi \equiv 1$ SALLX"

### 5.6.7 Complete Status Response Format

The complete status response transmitted by the MCU-8 to the remote control system with an MCU-8 address of $1, T X 01,02,03$ and 04 not connected to any antennas, TX 05 through TX 18 connected to ANT 05 to ANT 18, respectively, TX 19 and TX 20 not connected to any antennas, valid interlock closures for TX 05 through $T X 18$, no connect or summary faults, MCU-8 in the Remote mode, and normal matrix power supply status is displayed on the MCU-8 as follows. Although this message is displayed without intervening spaces, it is presented below with the same character spacing as shown in Section 5.5 for clarity.

Switch Sl0 on:

$$
\begin{array}{llllllllllll} 
\\
\xi & \equiv 1 & \mathrm{~S} & 1 & 0 & 0 & 0 & 0 & 2 & 0 & 0 & 0 \\
& 0 & 3 & 0 & 0 & 0 & 0 & 4 & 0 & 0 & 0 \\
& 0 & 5 & 0 & 5 & 1 & 0 & 6 & 0 & 6 & 1 \\
& 0 & 7 & 0 & 7 & 1 & 0 & 8 & 0 & 8 & 1 \\
& 0 & 9 & 0 & 9 & 1 & 1 & 0 & 1 & 0 & 1 \\
& 1 & 1 & 1 & 1 & 1 & 1 & 2 & 1 & 2 & 1 \\
& 1 & 3 & 1 & 3 & 1 & 1 & 4 & 1 & 4 & 1 \\
& 1 & 5 & 1 & 5 & 1 & 1 & 6 & 1 & 6 & 1 \\
& 1 & 7 & 1 & 7 & 1 & 1 & 8 & 1 & 8 & 1 \\
& 1 & 9 & 0 & 0 & 0 & 2 & 0 & 0 & 0 & 0
\end{array}
$$

With switch Sl0 set to the off position, an abbreviated version of the message is displayed. All characters from $\mathrm{Tl}_{1}$ through I 20 are not displayed and are replaced with two dashes. The remaining characters in the message are displayed as follows. Note that the entire status response is transmitted and only the message display is modified by switch Slo.
" $\xi \equiv 1 \mathrm{~S}-011$ -

LSD (BITS 0 THROUGH 3)


FIGURE 5-1
CHARACTER GENERATOR MODIFIED ASCII CODES

## SECTION 6

MAINTENANCE

### 6.1 PREVENTIVE MAINTENANCE

The enclosed construction of the MCU-8 Matrix Control Unit makes routine cleaning unnecessary. The highly reliable integrated circuitry does not require a program of preventive maintenance. At six month intervals, check the back-up batteries BT1, BT2 and BT3 for the nonvolatile memory. The test point, TP , shown in Figure 8-2, Component Locations Rear View, provides access to the battery voltage without having to extract the MCU-8 unit from the rack and remove the top cover. If the battery voltage is less than 3.75 volts, replace the batteries. Access the batteries by removing the small panel mounted on the rear panel. The MCU-8 main power must remain on while the batteries are removed and replaced to preserve the contents of the random access memories.

### 6.2 CORRECTIVE MAINTENANCE

6.2.1 The MCU-8 has been designed for easy troubleshooting following a straightforward approach made possible by the clearly defined functions of the plug-in printed circuit board assemblies. The following troubleshooting instructions are directed toward isolating the fault to a particular printed circuit assembly. Do not try to trace the fault to a particular component on an assembly due to the complex nature of the assemblies and the complex equipment required to monitor the dynamic waveforms of the components that interface the microprocessor. Once the fault is isolated to a particular assembly, replace the suspect assembly with a spare assembly from stock and return the defective assembly to the factory for repair.

## CAUTION

Prior to replacing any printed circuit assembly with a spare assembly, compare all programmable jumpers on the two assemblies to verify that identical jumpers are installed. Refer to the Lists of Material in Section 7 of this manual which detail for each assembly the designation, connection and function of the programmable jumpers. Incorrect installation of a programmable jumper on a replacement assembly may render the replacement assembly inoperative and may damage additional circuits due to address or data bus conflicts.

## CAUTION

When replacing the video display unit, verify that jumpers JUl and JU2 are in the TTL position (not in the composite position) on the signal circuit card (reference Appendix A, Service Manual for Video Display Unit).

Turn off the MCU-8 main power before removing or installing any printed circuit assemblies in the MCU-8 in order to prevent damage to the integrated circuits.

## CAUTION

The Matrix Control Unit contains parts and assemblies sensitive to damage by Electrostatic Discharge (ESD). Use ESD precautionary procedures when touching, removing, or inserting parts and assemblies in the MCU-8.
6.2.2 The initial step in troubleshooting is to isolate obvious faults. First, operate the microprocessor reset switch, S5, to restart the program at the beginning. This will ensure that the MCU-8 is operating under microprocessor control. Check all printed circuit assemblies for correct installation in their sockets and check all ribbon cable assemblies for secure installation. Check the cables between the MCU-8 and the Actuator Interface Unit and the serial data circuit port for secure installation.
6.2.3 Check the power supply for correct operating voltages. With reference to Figure 8-5, Power Supply Schematic Diagram, check the +5 VDC supply, the -5 VDC supply, the +12 VDC logic supply, the -12 VDC supply and the +12 VDC video supply. The 5 volt supplies should be within 0.25 volts of their nominal value and the 12 volt supplies should be within 0.6 volts of their nominal value. If the +5 VDC supply is at zero volts, momentarily cycle the AC power to reset the crowbar SCR, A3R7. Also check the power supply fuse A3Fl which may have blown due to a sustained crowbar of the +5 VDC supply by A3CR7. If the +12 VDC video supply is inoperative, check rear panel fuse $F 2$ which may have blown due to a crowbar of the video supply by overvoltage protector VR3. Replace the Power Supply Assembly if the -5, the +12 logic or the -12 supply is inoperative. Replace regulator VRl if the +5 VDC logic supply is malfunctioning and replace regulator VR2 if the +12 VDC video supply is malfunctioning.
6.2.4 If the preceding checks do not indicate any obvious problems, use the failure mode indications to troubleshoot the problem. As noted, the functions of each assembly are such that a defective assembly generally will exhibit unique failure indications permitting rapid troubleshooting to the assembly level. The following sections and troubleshooting tables detail expected failure indications versus defective assemblies.

### 6.3 TROUBLESHOOTING PROCEDURES

6.3.1 An abnomal matrix status display on the video display unit may indicate the failure of an MCU-8 assembly. Table 6-1 provides troubleshooting information based on the video display indication. For each abnormal video display indication, the table lists one or more assemblies as possible causes and suggests tests to verify the faulty assemblies. This troubleshooting information assumes that the actual matrix status is valid and the Interlock Isolation Assembly is operating. The external video monitor recomended in certain tests should accept standard composite video with a $15,750 \mathrm{~Hz}$ horizontal frequency and $50 / 60 \mathrm{~Hz}$ vertical frequency. The service manual included as Appendix A to this technical manual provides
maintenance information for the internal video display unit. Although not listed in the following table, consider the Microprocessor Assembly as a possible cause for all failure indications. If the suggested tests do not isolate the failure, replace the Microprocessor Assembly.
6.3.2 Certain failure modes of the MCU-8 assemblies may not be indicated by an abnormal status display but may be indicated by the loss of a major unit function. For instance, the MCU-8 may function normally in the local mode but not respond to serial data commands. Table 6-2 provides troubleshooting information based on the loss of a function not related to the video display. For each failure mode, the table lists one or more assemblies as possible causes and suggests tests to verify the faulty assembly. Although not listed in the following table, consider the Microprocessor Assembly as a possible cause for all failure indications. If the suggested tests do not isolate the failure, replace the Microprocessor Assembly.

### 6.4 REPLACING AN ASSEMBLY

## CAUTION

Before replacing any printed circuit assembly with a spare assembly, compare all programable jumpers on the two assemblies to verify that identical jumpers are installed. Refer to the Lists of Material in Section 7 of this manual which detail the designation, connection and function of the programmable jumpers on each assembly. Incorrect installation of a programmable jumper on a replacement assembly may render the replacement assembly inoperative and may damage other circuits due to address or data bus conflicts.

Turn off the MCU-8 main power before removing or installing any printed circuit assemblies in the MCU-8 in order to prevent damage to the integrated circuits.

The Matrix Control Unit contains parts and assemblies sensitive to damage to Electrostatic Discharge (ESD). Use precautionary procedures when touching, removing or inserting parts and assemblies in the MCU-8.

To replace a printed circuit assembly, first turn off the MCU-8 main power. Then remove the MCU-8 top cover panel. All of the assemblies are installed in the connectors of the Mother Board Assembly. To remove an assembly, gently pull it out of its connector socket. Then remove any ribbon cables connected to the assembly. Compare the settings of the programable jumpers on the replacement assembly with the jumper settings on the defective assembly. All settings must be identical. Then connect the ribbon cables to the replacement assembly and insert the assembly into the empty socket on the Mother Board Assembly. Make certain the printed circuit assembly is firmly seated. Then turn on the MCU-8 main power and verify that replacing the assembly corrected the problem. Reinstall the MCU-8 top cover panel, and return the defective assembly to Delta Electronics for repair.

TABLE 6-1

## VIDEO DISPLAY INDICATION TROUBLESHOOTING CHART

| Video Display <br> Indication | Possible Cause | Test |
| :--- | :--- | :--- |
| No Display | l2 vDC Video <br> Power Supply | Check VR2, VR3 and F2. |
|  | Video Display Unit | Connect external monitor, <br> Correct display on external |
| monitor indicates defective |  |  |
| internal display. Replace |  |  |
| display. |  |  |

TABLE 6-1
VIDEO DISPLAY INDICATION TROUBLESHOOTING CHART
(CONTINUED)

| Video Display Indication | Possible Cause | Test |
| :---: | :---: | :---: |
| Heading Format Correct, Multiple " F " is Displayed | Defective | Disconnect cables and check |
|  | MCU-8/AIU | if faults clear. |
|  | Cables |  |
|  | Row Status | Replace assembly. |
|  | PIA Assembly |  |
|  | Col Status | Replace assembly. |
|  | PIA Assembly |  |
| Incorrect Text or Random Data Displayed | Video Memory | Replace assembly. |
|  | Assembly |  |
|  | Video Assembly | Replace assembly. |
| Invalid Data in | Video Memory | Reload with switch S8, defeat |
| Lockout Memory | Assembly | with switch $S 7$ or replace assembly. |
| Loss of Lockout Memory Data When AC Power Off | Back-up Batteries | Test for 3.75 V minimum and |
|  |  | replace if necessary. |
|  | Open CR1 Diode | Test and replace diode if |
|  | on Video Memory Assembly | necessary. |
|  | Video Memory | Replace assembly. |
|  | Assembly |  |
| Received Message Display Incorrect | Data Format | Review programming of baud |
|  | Incorrect | rate, number of stop bits and parity. |
|  | Serial Interface Assembly | Replace assembly. |

TABLE 6-2

## EUNCTION LOSS INDICATION TROUBLESHOOTING CHART

| Function Loss Indication | Possible Cause | Test |
| :---: | :---: | :---: |
| Actuators Associated with a Specific Row Not Operating | Row Address <br> PIA Assembly | Replace assembly. |
| Actuators Associated with a Specific Col Not Operating | Col Address <br> PIA Assembly | Replace assembly. |
| Keypad Assembly Inoperative | Local/Remote Switch Failed In Remote Position | Check video display for "LCL" and "RMT" indication as switch is toggled. |
|  | Keypad Assembly <br> Serial Interface <br> Assembly | Replace assembly. <br> Replace assembly. |
| Remote Control Inoperative | Data Format Incorrect | Review programming of baud rate, number of stop bits, parity and MCU-8 address. |
|  | Local/Remote Switch Failed in Local Mode | Check video display for "LCL" and "RMT" indication as switch is toggled. |
|  | Serial Interface Assembly | Replace assembly. |

### 6.5 VIDEO DISPLAY UNIT REPLACEMENT/ALIGNMENT

6.5.1 Should the failure mode be isolated to the internal video display unit, replace the unit by disconnecting card-edge connector AlPl from the rear of the VDU and removing the four screws securing the unit to the chassis. Remove the filter from the defective monitor and install it on the new monitor. Verify that the TTL input jumpers JU1 and JU2 on the signal circuit card (reference Appendix A) are in the TTL position. Secure the new VDU to the chassis and connect card-edge connector AlPl to the signal circuit card.
6.5.2 To access the video alignment pattern, enable the NMI by toggling switch S6 (top cover removal provides access, see Figure 8-3). This provides a full CRT display of "+"s. Center and size the display according to the instructions provided in the video display unit technical manual (Appendix A). When the alignment is correct, momentarily operate the reset switch S 5 or depress any key on the Keypad Assembly to return to nomal operation.

### 6.6 SYSTEM TESTS

6.6.1 After completing the corrective maintenance, perform the following system tests to verify the MCU-8 is in operating condition. There are no accuracy verification procedures.
6.6.2 Reinstall the MCU-8 per the instructions in section 4. If no transmitter/antenna connections exist on the Strip line Switch, perform the initial system tests described in section 4.7. If transmitter/antenna connections exist on the switch, then check that the matrix status display correctly shows the matrix crosspoint and interlock status. Manually establish transmitter/antenna connections and check that the MCU-8 updates the matrix status display to show the connections. Then check the motorized crosspoint operation by entering the transmitter and antenna selections on the keypad. Also check the busy protect, lockout protect, lockout update and lockout display features. Verify that all remote control functions operate correctly.

## LIST OF MATERIAL

### 7.1 INTRODUCTION

7.1.1 Maintenance parts in the MCU-8 are identified by reference designations. These designations are used on the photographs, schematic diagrams, and Lists of Material to identify the components. The component reference designation is also marked adjacent to the component on the printed circuit assemblies. The letter(s) in the reference designation identifies the class of item such as a resistor, integrated circuit, or transistor or identifies a subassembly such as a printed circuit assembly. The number differentiates between parts or subassemblies of the same class.
7.1.2 Reference designations for the parts of a subassembly consist of the part's standard reference designation preceded by the reference designation for the subassembly. For example, reference designation A2R1 identifies resistor number 1 on subassembly number 2. When all of the prefixes are identical on a schematic diagram or printed circuit board, they may be omitted for brevity and a note to that effect is placed on the drawing or circuit board.
7.1.3 The MCU-8 Matrix Control Unit may incorporate two or more printed circuit assemblies that are identical except for the peripheral address of the assembly when the MCU-8 controls a Model SLS Strip Line Switch with more than sixteen rows and/or columns, when the ricU-8 controls multiple Model SLS Strip Line Switches or when the Remote Model MCU-8 Unit controls multiple Local Model MCU-8 Units. Assemblies that differ nnly in peripheral address are differentiated by suffixing a letter ( $A, B$, etc.) to the reference designation and to the part number. Since the multiple assemblies are essentially identical, a single List of Material and Schematic Diagram applicable to the primary assembly are provided and the different peripheral address programming connections for the secondary assemblies are detailed as required in the programable jumper installation tabulation section of the subject List of Material.
7.1.4 The Lists of Material for the MCU-8 Matrix Control Unit and for the maintenance significant assemblies are presented as detailed below. The maintenance parts list for the Video Display Unit is provided in the Service Manual included as Appendix A to this Technical Manual. Maintenance parts lists for ancillary equipments such as data modems and remote displays are provided by the equipments' technical manuals which are appended to this manual as required.

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| Assy, PIA, Intlk Status | 7.15 | $7-45$ |



| 7. | LIST OF MATERIAL, FINAL ASSEMBLY, MATRIX CONTROL UNIT, D13-62-97, REV. A |
| :--- | :--- | :--- | :--- |


| $\begin{aligned} & \stackrel{0}{6} \\ & \stackrel{\rightharpoonup}{\mathrm{~F}} \\ & \hline \end{aligned}$ | Reference Designation | Description | Manufacturer | Manufacturer Part No. |
| :---: | :---: | :---: | :---: | :---: |
| Po | Cl | Cap, Fxd, Elctlt, 5500 UF, 40V | Sprague | 36D552G040AC2A |
|  | C2 | Same as Cl |  |  |
|  | C3 | Cap, Fxd, Tant, 4.7 UF, 35V | Sprague | 196D475X9035JAl |
|  | C4 | Cap, Fxd, Elctlt, 100 UF, 50 V | Sprague | TE-1309 |
|  | C5 | Same as C3 |  |  |
|  | C6 | Same as C4 |  |  |
|  | C7 | Cap, Fxd, Cer, 0.01 UF, 25V | Sprague | HY520 |
|  | F1 | Fuse, Type 3AG, 0.5A, Slo-Blo | Littelfuse | 313.500 |
|  | F2 | Fuse, Type 3AG, 1.5A, Slo-Blo | Littelfuse | 31301.5 |
|  | FL1 | Filter, Line | Corcom | $3 E D 1$ |
|  | J1 | Conn, Rcpt, 25 Pin, Female, Part of Cable Assy W4 |  |  |
|  | J2 | Conn, Rcpt, 50 Pin, Female, Part of Cable Assy W2A |  |  |
|  | J3 | Conn, Rcpt, 50 Pin, Female, Part of Cable Assy W3A |  |  |
|  | J4 | Conn, Rcpt, 50 Pin, Female, Part of Cable Assy W2B |  |  |



| $\stackrel{\circ}{\text { E }}$ | Reference Designation | Description | Manufacturer | Manufacturer Part No. |
| :---: | :---: | :---: | :---: | :---: |
| $\bigcirc$ | S5 | Switch, Toggle, Mom Actn | Alco | MTA-106F |
|  | S6 | Same as S5 |  |  |
|  | S7 | Switch, Toggle, Altn Actn | JB'T | JMT-123 |
|  | S8 | Same as S5 |  |  |
|  | S9 | Same as S7 |  |  |
|  | S10 | Same as S7 |  |  |
|  | T1 | Xfmr, Power | Signal | 9710 |
|  | TB1 | Terminal Block | Kulka | 599-2004-3 |
|  | VR1 | IC, VR, Fxd, Pos 5V, 5A | Fairchild | UA 78H05KC |
|  | VR2 | IC, VR, Exd, Pos 12V, 5A | Fairchild | UA78H12KC |
|  | VR3 | IC, Overvoltage Protector, 12 VDC, 6A | Lambda | L-6-OV-12 |
|  | W1 | Cable, Power | Belden | 17600 |
|  | W2A | Cable Assy, 50 Pin EIA to 50 Pin Transition | Delta | D53-28-27 |
|  | W2B | Same as W2A |  |  |
|  | W2C | Same as W2A |  |  |
| $\stackrel{1}{1}$ | W3A | Same as W2A |  |  |

7.3 4 LIST OF MATERIAL, FINAL ASSEMBLY, MATRIX CONTROL UNIT, D13-62-97, REV. A CONTINUED
7.4 LIST OE MATERIAL, POWER SUPPLY ASSY, D33-275-1, REV. X

| Reference Designation | Description | Manufacturer | Manufacturer Part No. |
| :---: | :---: | :---: | :---: |
| C1 | Cap, Fxd, Elctlt, 5 UF, 25V | Sprague | TE-1202 |
| C2, C3 | Same as Cl |  |  |
| C4 | Cap, Fxd, Elctlt, 500 UF, 50V | Sprague | 39D507G050GL4 |
| C5, C6 | Same as C4 |  |  |
| C7 | Cap, Fxd, Polyest, 1.0 UF, 63V | Roederstein | MKT 1822510065 |
| C8 | Same as C7 |  |  |
| C9 | Cap, Fxd, Tant, 4.7 UF, 35V | Sprague | 196D475X9035JAl |
| Cl0 | Same as C9 |  |  |
| CRI | Bridge Rectifier, 100 PIV, 4A | Motorola | MDA 970-2 |
| CR2 | Same as CR1 |  |  |
| CR 3 | Diode, Sil, Rect, 100 PRV, 3A | Motorola | MR851 |
| CR4 | Same as CR3 |  |  |
| CR5 | Diode, Ger |  | 1N34A |
| CR6 | Diode, Zener, 5.6 V |  | 1N5232 |
| CR7 | Silicon Controlled Rectifier |  | 2N6400 |
| El | Fuse, Type 3AG, 2A, Slo-Blo | Littelfuse | 313002 |


|  | 7.4 LIST OF MATERIAL, POWER SUPPLY ASSY, D33-275-1, REV. X CONTINUED |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Reference Designation | Description | Manufacturer | Manufacturer Part No. |
|  | J2 | Conn, Hdr, 8 Posn, 0.150 Spacing | Berg Electronics | 65566-408 |
|  | R1 | Res, Exd, WW, 0.68 Ohm, 10\%, 6.5W |  | RW767VR68 |
|  | R2 | Unassigned |  |  |
|  | R3 | Res, Fxd, Film, 22 Ohm, 5\%, 2W |  | RL 42S 220 J |
|  | R4 | Res, Fxd, WW, 0.33 Ohm, $10 \%$, 6.5 W |  | RW67VR33 |
|  | R5 | Same as Rl |  |  |
|  | R6 | Res, Exd, Film, lK Ohm, 5\%, 1/4W |  | RL07S102J |
|  | R7 | Res, Fxd, Film, 7.5K Ohm, 5\%, 1/4W |  | RL07S752J |
|  | R8 | Res, Var, Trme, 10K Ohm | Beckman | 93PR-10K |
|  | R9 | Res, Fxd, Film, 43 Ohm, 5\%, 1/4W |  | RL07S430J |
|  | R10 | Res, Fxd, WW, 22 Ohm, 5\%, 5W | Ohmite | 4569 |
|  | R11 | Res, Fxd, Film, 150K Ohm, $5 \%$, $1 / 4 W$ |  | RL.07S 154J |





| $\bigcirc$ | 7.6 LI | MATERIAL, MICROPROCESSOR SUBASSY, | 3-387-1 |  |
| :---: | :---: | :---: | :---: | :---: |
| No | Reference Designation | Description | Manufacturer | Manufacturer Part No. |
|  | C1 | Cap, Fixed, Tant, $4.7 \mathrm{uF}, 35 \mathrm{~V}$ | Sprague | 199D475X9035CAl |
|  | C2 | Cap, Fixed, Ceramic, 0.1 uF, 50V | Sprague | 1C20Z5U104M050B |
|  | C3 | Same as Cl |  |  |
|  | C4 thru | Same as C2 |  |  |
|  | C7 |  |  |  |
|  | C8 | Cap, Fixed, Elctlt, 10 uF, 16V | Sprague | TE-1155 |
|  | C9 | Same as C8 |  |  |
|  | Cl0 | Cap, Fixed, Mica, 500 pF , 5\%, 500V | Arco | DM15-501J |
|  | C11 | Same as C2 |  |  |
|  | CRI | Diode, Germanium |  | 1N34A |
|  | CR2 | Diode, Silicon |  | 1N4148 |
|  | CR3 | Same as CR2 |  |  |
|  | R1 | Res, Exd, Film, 4.7K Ohm, 5\%, 1/4W |  | RL07S 472J |
|  | R2 | Res, Fxd, Film, IK Ohm, 5\%, 1/4W |  | RL07S 102J |
|  | $\begin{aligned} & \text { R3 thru } \\ & \text { R6 } \end{aligned}$ | Same as R2 |  |  |
| $\stackrel{\checkmark}{\stackrel{1}{\bullet}}$ | Ul | IC, Mipres, 1 MHz | Rockwell | R6502 |
|  | U2 | IC, Miprcs, Supervisory Ckt | Maxim | MAX690CPA |



| 0 | Reference Designation | Description | Manufacturer | Manufacturer Part No. |
| :---: | :---: | :---: | :---: | :---: |
|  | Cl | Cap, Fxd, Cer, 0.047 UF, 25V | Sprague | HY535 |
|  | C2 | Cap, Fxd, Cer, 0.47 UF, 25V | Sprague | HY780 |
|  | C2 | Cap, Exd, Cer, 0.47 UF, 12V (Alternate) | Centralab | UK12-247 |
|  | C3 | Cap, Fxd, Tant, 4.7 UF, 35V | Sprague | 196D475X9035JAl |
|  | C4 | Cap, Fxd, Cer, 0.01 UF, 25V | Sprague | HY520 |
|  | J2 | Conn, Hdr, 6 Posn, 0.150 Spacing | Berg <br> Electronics | 65566-406 |
|  | Q1 | Transistor, NPN |  | 2N3904 |
|  | R1 | Res, Fxd, Film, 5.1K Ohm, 5\%, 1/4W |  | RL07S512J |
|  | R2 | Res, Fxd, Film, 1K Ohm, $5 \%, 1 / 4 \mathrm{~W}$ |  | RL07S 102 J |
|  | R3 | Same as R2 |  |  |
|  | Sl | Switch, PB | Mechanical <br> Enterprises | T5C-M-NO |
|  | $\begin{aligned} & \text { S2 thru } \\ & \text { S20 } \end{aligned}$ | Same as S1 |  |  |
|  | SIMP1 | Button, PB Switch, "7" | Mechanical <br> Enterprises | K0033-G |


7.7 LIST OF MATERIAL, KEYPAD ASSY, D33-247-2, REV. R CONTINUED

| Reference Designation | Description | Manufacturer | Manufacturer Part No. |
| :---: | :---: | :---: | :---: |
| S14MP1 | Button, PB Switch, "D" | Mechanical <br> Enterprises | K0004-G |
| S15MP1 | Button, PB Switch, "ANTENNA" | Delta | D05-91-7 |
| S16MP1 | Button, PB Switch, "A" | Mechanical Enterprises | K0001-G |
| S17MP1 | Button, PB Switch, "0" | Mechanical <br> Enterprises | K0015-G |
| S18MP1 | Button, PB Switch, "B" | Mechanical <br> Enterprises | K0002-G |
| S19MP1 | Button, PB Switch, "C" | Mechanical <br> Enterprises | KC003-G |
| S20MPl | Button, PB Switch, "ENABLE" | Delta | D05-91-8 |
| U1 | IC, Int, Keyboard Encoder | National | MM74C923 |
| U2 | IC, LSTTL, Triple 3-Input Nand Gate |  | 74LS10N |
| U3 | IC, BCMOS, Hex Tristate Buffer | Motorola | MC14503BCP |
| W1 | Jumper, Wire, \#24 AWG, $\mathrm{w} /$ Teflion Insul |  |  |
| W2 | Same as Wl |  |  |



PROGRAMMABLE JUMPER INSTALLATION

| Jumper |  |  |
| :---: | :---: | :---: |
| Des. | Connection | Function |
| W1 | --- | Keys C, D, E and F Enable |
| W2 | N/U |  |



${\underset{1}{0}}_{0}^{0} 7.8$ LIST OF MATERIAL, SERIAL INTEREACE ASSY, D33-290-1, REV. G CONTINUED

## PROGRAMMABLE JUMPER INSTALLATION

| Jumper |  |  |
| :---: | :---: | :---: |
| Des. | Connection | Function |
| W1 (PRI) | 1-W | Address Block \$6000-\$7FEF |
| W1 (SEC) | 1-V | Address Block \$4000-\$5FFF |
| W2 (PRI) | 1-K | ACIA Address XlXX |
| W2 (SEC) | 1-L | ACIA Address X2XX |
| W3 (PRI) | 1-L | Aux PIA Address X2XX |
| W3 (SEC) | 1-M | Aux PIA Address X4XX |
| W4 (PRI) | 1-M | Kybd Address X4XX |
| W4 (SEC) | $\mathrm{N} / \mathrm{U}$ |  |
| W5 (PRI) | 1-4 | ACIA IRQ |
| W5 (SEC) | 1-4 | ACIA IRQ |
| W6 THRU W13 | --- | Custom Feature Programming |




| $\bigcirc$ | Reference Designation | Description | Manufacturer | Manufacturer Part No. |
| :---: | :---: | :---: | :---: | :---: |
|  | U7 | IC, LSTTL, Triple 3-Inp Nand Gate |  | 74LSION |
|  | U8 | IC, LSTTL, Quad 2-Inp EOR Gate |  | 74LS86N |
|  | U9 | IC, TTL, Quad 2-Inp Nand Gate |  | 7400N |
|  | 010 | Same as U9 |  |  |
|  | U11 | IC, TTL, Dual Retrig Monstb Mvib |  | 74LS123N |
|  | W1 | Jumper, Wire, \#22 AWG, w /Tefion Insul |  |  |
|  | W2 thru W8 | Same as Wl |  |  |
|  | Y1 | $\begin{aligned} & \text { Crystal, HC-18/N } \\ & 10.0000 \mathrm{MHz} \end{aligned}$ |  |  |


| 7.9 | LIST OF MATERIAL, VIDEO ASSY, D33-271-2, REV. P CONTINUED <br> PROGRAMMABLE JUMPER INSTALLATION |  |
| :---: | :---: | :---: |
| Jumper Des. | Connection | Function |
| W1 | N/U |  |
| w2 | 2-3 | Cursor Inactive |
| w3 | 1-J | CRTC Address XX8X |
| W4 | 1-K | CRTC Address XIXX |
| W5 | 1-V | Address Block \$4000-5FFF |
| W6 | 1 TO 2 | Vert Sync |
| W7 | N/ |  |
| W8 | $\mathrm{N} / \mathrm{U}$ |  |


| $$ | 7.10 LIST OF MATERIAL, VIDEO MEMORY ASSY, D33-408-1, REV. A |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Reference Designation | Description | Manufacturer | Manufacturer Part No. |
|  | Cl | Cap, Fxd, Tant, 4.7 UF, 35V | Sprague | 199D475×9035CA1 |
|  | C2 | Same as Cl |  |  |
|  | C3 | Cap, Fxd, Tant, 0.1 UF, 35V | Sprague | 199D104X9035AA1 |
|  | C4 | Cap, Fxd, Ceramic, 0.1 UF, 50V | Sprague <br> Kemet | 1Cl0Z5U104M050B C315Cl04M5U5CA |
|  | C5 | Same as C4 |  |  |
|  | C6 | Same as C4 |  |  |
|  | C7 | Same as Cl |  |  |
|  | CRl | Diode, Germanium |  | 1N34A |
|  | CR2 | Diode, Silicon |  | 1N4148 |
|  | CR3 | Same as CRl |  |  |
|  | UI | IC, LSTTL, Data Selector |  | SN74LS157N |
|  | U2 thru | Same as Ul |  |  |
|  | U4 |  |  |  |
|  | U5 | IC, $8 \mathrm{~K} \times 8$ CMOS Static RAM | Hitachi Sony | $\begin{aligned} & \text { HM6264LP-12 } \\ & \text { CXK5864PN-12L } \end{aligned}$ |
|  | U6 | IC, LSTIL, Quad 2-Input Nand Gate |  | SN74LS00N |
|  | U7 | Same as U6 |  |  | LIST OF MATERIAL, VIDEO MEMORY ASSY, D33-408-1, REV. A CONTINUED


| Reference Designation | Description | Manufacturer | Manufacturer Part No. |
| :---: | :---: | :---: | :---: |
| U8 | IC, Int, Quad Bus Xcvr, Non-Inv | Signetics | 8 T 28 |
| U9 | Same as U8 |  |  |
| Ul0 | Res, SIP Ntwk, 10 Com, 10K Ohm | CTS <br> Beckman | $\begin{aligned} & \text { 750-101-R10K } \\ & 785-1-\mathrm{RlOK} \end{aligned}$ |
| VR1 | IC, VR, Fxd, Pos 5V, 0.1A | Motorola | MC78L05CP |
| W1 | Wire, Tinned Copper Bus, \#24 AWG | QQ-W-343 | Type S |

PROGRAMMABLE JUMPER INSTALLATION

Jumper
Des.

Wl

Connection

1-U

Function

Address Block \$2000-\$3FFF









|  | 7.13 <br> Reference Designation | LIST Of MATERIAL, ROW Status pia assembly, D33-299-3, REV. F through g |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Description | Manufacturer | Part No. |
|  | Cl | Cap, Fxd, Tant, 4.7 UF, 35V | Sprague | 196D475X9035JA1 |
|  | C2 | Same as Cl |  |  |
|  | J1 | Conn, Har, Male, 50 Posn | T\&B/Ansley | 609-5027 |
|  | J2 | Conn, Har, 6 Posn, 0.150 Spacing | Berg <br> Electronics | 65566-406 |
|  | Rl | Res, Fxd, Film, 1K Ohm, 5\%, 1/4W |  | RL07S102J |
|  | R2 thru R6 | Same as R1 |  |  |
|  | Ul | IC, Prphl Intfc Adptr (PIA) | Motorola MOS Tech | $\begin{aligned} & \text { MC6820P } \\ & \text { MPS6520 } \end{aligned}$ |
|  | U2 | IC, BCMOS, 8-Bit Bidir CMOS/TTL | RCA | CD40116BE |
|  | U3 thru | Same as U2 |  |  |
|  | U8 thru U13 | Unassigned |  |  |
|  | W1 | Jumper, Wire, \#22 AWG, w/Teflon Insul |  |  |
|  | W2 | Same as Wl |  |  |
| $\stackrel{\underset{\sim}{\omega}}{ }$ | W3 | Jumper, Prgm | Berg Elec. | 65474-001 |
|  | W4 thru W17F | Same as W3 |  |  |










| Jumper Designation | Connection | Function |
| :---: | :---: | :---: |
| W1 | 1-E | PIA ADDRESS XXIX |
| W2 | 1-V | ADDRESS BLOCK \$4000-\$5FFF |
| W3 | D TOP, ETOG | U2 INPUT |
| W4 | D TOP, E TO G | U3 INPUT |
| W5 | D TO P, ETOG | U4 INPUT |
| W6 | D TO P, E TO G | U5 InPut |
| W7 | D TO P, ETO G | U6 Input |
| W8 | D TO P, E TOG | U7 INPUT |
| W9 | TO + | U8 PULLUP |
| W10 | TO + | U9 PULLUP |
| W11 | TO + | U10 PULLUP |
| W12 | TO + | U11 PULLUP |
| W13 | TO + | U12 PULLUP |
| W14 | TO + | U13 PULLUP |
| W15A | С то 1 | PA4 TO U6 |
| W15B | C TO 1 | PA4 TO U7 |
| W15C | с то 1 | PA5 TO U6 |
| W15D | С то 1 | PA5 TO U7 |


| Jumper <br> Designation | Connection | Function |
| :--- | :--- | :--- |
| W15E | C TO 1 | PA6 TO U6 |
| W15F | C TO 1 | PA6 TO U7 |
| W15G | C TO 1 | PA7 TO U6 |
| W15H | C TO 1 | PA7 TO U7 |
| W16A | C TO 1 | PB4 TO W7-P |
| W16B | N/U |  |
| W16C | N/U | PB5 TO W8-P |
| W16D | C TO 1 | R1 PULLUP |
| W17A | TO + | R2 PULLUP |
| W17B | TO + | R3 PULLUP |
| W17C | TO + | R4 PULLUP |
| W17D | TO + | R5 PULLUP |
| W17E | TO + | R6 PULLUP |

## SECTION 8

## ILLUSTRATIONS AND CIRCUIT DIAGRAMS



| FIGURE 8-I |
| :---: |
| COMPONENT LOCATIONS |
| FRONT VIEW |



* J2 THRU J11 SUPPLIED AS REQUIRED DEPENDING ON NUMBER AND CONFIGURATION OF MATRICES, FOR A SINGLE MATRIX WITH 16 ROWS/16 COLS OR LESS, ONLY J2 AND J3 ARE REQD, FOR A SINGLE MATRIX WITH MORE THAN 16 ROWS/16 COLS AND LESS THAN 4Ø ROWS/4Ø COLS, J2 THRU J6 ARE REQUIRED.
** J1 (STANDARD) AND J13 (OPTIONAL) SUPPLIED AS REQUIRED DEPENDING ON REMOTE CONTROL SYSTEM INTERFACE REQUIREMENT .

FIGURE 8-2
COMPONENT LOCATIONS REAR VIEW


| FIGURE $8-3$ |
| :---: |
| COMPONENT LOCATIONS |
| TOP VIEW |






* COMPONENT DESCRIPTIONS:

CI $0.01 \mu$ F, $25 V$ EFF REV h thru L
$0.047 \mu$ F, 25V EFF REV M
FIGURE 8-7
$20.1 \mu \mathrm{~F}, 16 \mathrm{~V}$ EFF REV H THRU $L$
$0.47 \mu \mathrm{~F}, 25 \mathrm{~V}$ EFF REV M
$0.47 \mu \mathrm{~F}, 12 \mathrm{~V}$ ALT EFF REV $P$








# Unfortunately, this is a scan of a photocopy of a photocopy and so parts of it may not be readable. 

APPENDIX A<br>SERVICE MANUAL FOR<br>M2000 SERIES<br>VIDEO DISPLAY UNIT

REPRINTED WITH PERMISSION OF
MOTOROLA, INC. DISPLAY SYSTEMS

## DISPLAY MANUAL SUPPLEMENT

INSTRUCTION MANUAL AFFECTED:
Service Manual VP?
Motwola Part No 68P25253A23

## PURPOS:

Provide upteded service information for the revised Signal Circuit Card, which is used in the M1000/M2000 Series CRT Whelsy bontors.

## DESCRIPTIOL:

This supperment contains updeted circuit card layouts, schematic diagrams, and a replacement service parts Fst. They are arolicable to Redel M1000/M2000 Series CRT display monitors using the revised Signal Circuit Card, fort no. 84025985E02. (This pet n. is located on the bottom or foil side of the circuit card.) For Signal Circuit Cards with curs m. geD25,ggev2 and earlier), refer to the basic service manual (VP16), part no. 68P25253A23.

The Defecton Crati Cas nat affected. As a result, circuit card layouts in the basic service manual (VP16) are whtaphicolle.


Signal Circuit Card - Applicable to Models M1000-100, 155 and M2000 Series


Schematic Diagram for Models M1000-100, 155 and M2000 Series



 minciacuit ground

1. chass.s secane

- wire wowo : Eammats.
 $\frac{48}{\operatorname{conncc}+14}$






ST EDGE CONNECTOR SOCKET



$\square$

## M1000/2000 SERIES SERVICE PARTS LIST

This service parts list represents components for the basic M1000/2000 CRT display models. For replacement of components that differ in unique CRT display models, order by the unique model number, schematic designator and description.

When a component requires replacement, it is recommended that only Motorola part numbers be used. This is necessary to ensure optimum performance and reliability from selected components with specific operating characteristics. When a part number is not listed, however, an equivalent may be substituted.

| REF . NO. | PART NO. | DESCRIPTION |
| :---: | :---: | :---: |
| CAPACITORS |  |  |
| Cl | 23S00187A26 | 22, 25V; Lytic |
| C2 | $21500180 \mathrm{C64}$ | 33PF 10\%, N750, 100V; Cer Disc |
| C3 | 8 S 10191898 | .01 108, 250N; Poly |
| C4 | 23R29914A77 | 22, 35V; Lytic |
| C5 | 23S00187A 26 | 22, 25V; Lytic |
| C6 | 21500180853 | 470PF 108, X5F, 500V; Cer Disc |
| C7 | 8S10212A91 | 0.22 108, 250 V |
| C8 | 21500180 C 52 | 18PF 5\%, NPO, 500V; Cer Disc |
| C9 | 23S10255A06 | 100, 16V : Lytic |
| C10 |  | (Not Used) |
| C11 |  | (Not Used) |
| C12 | 21500180807 | . 001 10\%, Z5F, 500V; Cer Disc |
| C13 | 8S10191B96 | 4700PF, 10\%, 400v; Poly |
| C14 |  | (Not Used) |
| C15 | $8 \mathrm{~S} 10191 \mathrm{B91}$ | . 047 10\%, 250V; Poly |
| C16 | 23S 10229A32 | 1.0 20\%, 16V; Lytic |
| C17 | 21 R 29964 A 06 | 2200PF 2\%, NPO, 100 V |
| C18 | 8R10191B88 | . 027 10\%, 400v; Poly |
| C19 | 8R29959840 | 0.1 10\%, 200v; Poly |
| C20 | 8R29956A 39 | .047 5\%, 200v; Poly My lar |
| C21 | 8R29959840 | 0.1 10\%, 200V; Poly |
| C22 | 21500180093 | 6.8PF +0.5, NPO 500N; Cer Disc |
| C23 | $8 S 10191897$ | 6800PF 10\%, 400V; Poly |
| C24 | 21500180C84 | .0027 10\%, 25F, 50V; Cer Disc |
| C25 | 8510191898 | .01 10\%, 250V; Poly (M1000-100,155M2000-100,155) |
| C25 | 8510191891 | . 047 10\%, 250V; Poly (M1000-190) |
| C26 | 8S 10191889 | . 022 10\$, 250V; Poly |
| C27,28 | 23S10218A31 | 5.0 10\%, 15V; Lytic |
| C 29 | 8 S 10191898 | . 01 10\%, 250V; Poly |
| C30 | 8510191416 | . 01 10\%, 400V; Poly |
| C31 | 23S10255A29 | 470, 16V; Lytic |
| C32 | 8S 10191807 | . 047 108, 400v; Poly |
| C33 | 23S 10255A 74 | 22, 160V; Lytic |
| C34 | 8S 10191807 | . 047 10\%, 400v; Poly |
| C35 | 8 S 10212820 | 0.47 10\%, 400 V |
| C36 | $21500180 C 41$ | . 0027 108, 25F, 500v; Cer Disc |
| C37 | 8510191453 | 0.22 10\%, 160V; Poly |
| C38 | $23 S 10255883$ | 1800, $85^{\circ} \mathrm{C}, 20 \mathrm{~V}$; Lytic |
| C39 |  | (Not Used) |
| C40 | 21500180007 | 15PF, 10\%, N150, 500\%; Cer Disc |
| C41 | 21500180889 | 180PF 108, 100V; Cer Disc |
| C42 | 21R00180C82 | 33PF 10\%, N150, 500V; Cer Disc |
| 643 |  | (Not Used) |
| C44 | $8 \mathrm{S10169871}$ | . 033 108, 400v; Mylar (M2000) |
| C45 | 8 S 10212052 | 0.1 108, l00V; Mtiz Poly |
| C46,47 | 23R29914A73 | 4.7. 35 V ; Lytic |


| REF. NO. | PART NO. | DESCRIPTION |
| :---: | :---: | :---: |
| CAPACITORS (CONT.) |  |  |
| C48 | 8S 10191890 | . 033 108, 250V; Poly |
| C49 | 23510255826 | 4.7, 63V; Ly+ic |
| C50 | 21 129964A05 | 0.1 +80-20\%, 25U, 100V; Car Disc |
| C51 |  | (Not Used) |
| C52 | 21500180890 | .01, 208, 25u, 100v; Cer Disc |
| C53 | $21 R 29964 A 05$ | 0.1 +80-20\%, Z5U, 100V; Cer Disc |
| C54 | 21500180851 | . 001 10\%, X5F, 500V; Cer Disc |
| DIODES |  |  |
| D1 | $48 \mathrm{PO} 02054 \mathrm{A00}$ | Diode, Fast Recovery; 2054 |
| D2 | 485191405 | Rectifier, Silicon 91a05 |
| D3-06 | 48802054A00 | Diode, Fast Recovery; 2054 |
| D7-09 | 485191405 | Rectifier, Silicon 9la05 |
| D10 | 435134921 | Rectifier, Silicon 800V DID |
| D11 | 182 134978 | Rectifier, Silicon Dik |
| 012 | 48 R 137608 | Diode, Silicon; H.V. (Nil000) |
| 012 | 438137622 | Diode, Silicon; H.V. (M2000) |
| D13,14 | *8802054A00 | Diode, Fast Recovery; 2054 |
| INTEGRATED CIRCUITS |  |  |
| 10.1 | E1R6332A00 | IC, Timer; 555 |
| COILS \& CHOKES |  |  |
| 4 | 24025603A03 | Coil, Width (M1000) |
| 4 | \%025603A04 | Coil, Width (M2000) |
| 12 | 23025221409 | Choke, Vert. Out |
| 13, ${ }^{\text {a }}$ | 24025290402 | Yoke, Deflection (M1000) |
| LSA/B | 24068531403 | Yoke, Deflection (M2000) |
| TRANSISTORS |  |  |
| Q1 | 429134997 | Ist Video Ampl. A3k |
| 2 | 46र157127 | 2nd Video Ampl. P2S |
| 03 | A A3137172 | 3rd Video Ampl. A6J |
| Q4 | $45 \times 137093$ | Video Output A5F (M1000-100,155/M2000) |
| 84 | 43803026A00 | Video Output 3026 (M1000-190) |
| 93 | 483: 37171 | Sync Sep. A6H |
| 36 | 481137127 | Sync Ampl. P2S |
| Q: | 46233007A00 | Horiz. Driver 3007 (M1000-100,155/M2000) |
| \% | $48 \mathrm{~F} / 37169$ | Horiz. Driver A6G (M1000-190) |
| q | 406035a00 | Horiz. Output 3035 |
| c |  | Blanking Ampl. A6J |
| 810 |  | Vert. Osc. AbJ |
| O! | $48 \mathrm{P}: 34997$ | Vert. Driver A3K |
| Q2 | 48R137598 | Vert. Output B2Y |
| RESISTORS/CONTROLS |  |  |
| Unlass otherwise noted, all Abbr: FCF = Fixed Carbo. Film |  |  |
| velues are in ohms, 1/4 watt, $\quad \mathrm{FCC}=\mathrm{Fixed}$ Carber Composition |  |  |
| 5. Preistors not listed are FMF = Fixed Meta: Film |  |  |
| ct the fixed carbon film type, WW = wirewound |  |  |
| 1/4 ar $/ 12$ watt, 5 , as noted <br> MOF = Metal Oxide F <br> on the monatic.) |  |  |
| 88 | 18025245A02 | Control, Contrast ik |
| 814 | $18025245 A 02$ | Control, Video Bias F . |
| 818 | IPR10731A03 | WW; 1.5K, 7W |
| Ps | YOD25245A06 | Control, Horiz. Hoid ZX |
| 5 ES | 6 6 10621 D 17 | FMF; 18.2 K 18, 1/8w |




MODEL M2000 (9"-CRT)

| TABLE 1 |  |  |  |
| :---: | :---: | :---: | :---: |
| MODEL SIGNAL INPUT * CRT SIZE \& PHOSPHOR  <br> M1000-100 TTL $5^{\prime \prime}$ P4 <br> M1000-155 COMPOSITE $5^{\prime \prime}$ P4 <br> M1000-190 DIRECT DRIVE $5^{\prime \prime}$ P4 <br> M2000-100 TTL $9^{\prime \prime}$ P4 <br> M2000-155 COMPOSITE $9^{\prime \prime}$ P4 <br> M2000-355 COMPOSITE $9^{\prime \prime}$ P31 <br> *All CRT's are without anti-reflective faceplates.    |  |  |  |

## GENERAL INFORMATION

The models described herein are fully transistorized (except CRT) and applicable for displaying alphanumeric characters. All models will accept TTL or composite video inputs depending on jumper positioning. The exception is Model M1000-190 which is designed for direct drive applications only.

NOTE: The Model M2000-100 (TTL) is supplied factory wired as a model M2000-155 (composite video) version. See schematic diagram for jumper locations.

The CRT'S employed are of the magnetic deflection type with integral implosion protection. An operating voltage of 12 volts DC @ 650 mA (typical) is required from an external power supply for the M1000 models. The M2000 models require an external 12 volts $D C$ @ 900 mA (typical).

## Service Manual VP16

## M1000 and M2000 SERIES

(See Table 1)

MODEL M1000 (5' - CRT)

## CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVIC. ING PROCEDURES AND PRECAUTIONS.

Input and output connections for these models are made through a 10-pin edge connector on the signal circuit card. Output connections are provided for an optional remote brightness control, except on the Model M1000-190.

Two plug-in etched circuit cards are utilized, a signal circuit card and a deflection circuit card. Components are mounted on the top of the circuit cards and copper foil on the bottom. Schematic reference numbers are printed on the top and bottom of each circuit card to aid in the location and identification of components for servicing. All standard operating/adjustment controls are mounted in a convenient manner on both circuit cards.

## CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.
2. A GOOD PRACTICE, when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.
3. Extreme care should be used in HANDLING THE PICTURE TUBE as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in.). Do not nick or scratch glass or subiect it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire. When servicing or repairing the monitor, if the cathode ray tube is replaced by a type of tube other than that specified under the Motorola Part Number as original equipment in this Service Manual, then avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger of personal injury from unnecessary exposure to X-ray radiation may result.
4. An ISOLATION TRANSFORMER should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.
5. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.
6. If the HIGH VOLTAGE is adjustable, it should al ways be ADJUSTED to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary $X$-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

## 7. BEFORE RETURNING A SERVICED UNIT, the

 service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER WHEN MAKING THIS TEST.In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.


## Voltmeter Hook-up for Safety Check

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.

The AC voltage indicated by the meter may not exceed $7 \frac{1}{2}$ volts. A reading exceeding $7 \frac{1}{2}$ volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.

The above test should be repeated with the power plug reversed, when applicable.

NEVER RETURN A MONITOR which does not pass the safety test until the fault has been located and corrected.

## ELECTRICAL SPECIFICATIONS *

|  | MODEL M1000 | MODEL M2000 |
| :---: | :---: | :---: |
| PICTURE TUBE (CRT): | 5" measured diagonally ( 127 mm ); 13 sq . in. viewing area ( $84 \mathrm{sq} . \mathrm{cm}$ ); $55^{\circ}$ deflection angle; P4 phosphor standard | $9^{\prime \prime}$ measured diagonally ( 228 mm ): 44 sq. in viewing area ( 284 sq.cm): $90^{\circ}$ deflection angle; integral implosion protection; P4 phosphor standard except P31 phosphor in Model M2000-355. |
| POWER INPUT: | 12 V DC at 650 mA | 12 V DC at 900 mA |
| INPUT SIGNALS: | COMPOSITE VIDEO INPUT: 0.5 V t <br> impeda <br> minate <br>  2.5 V t <br> put (in <br>  $>2 \mathrm{k}$ oh <br> TTL INPUT: 2.5 V t <br> DIRECT DRIVE INPUT: 1190 u <br>  drive <br> dance: <br>  zontal | .5V composite $\mathrm{P} / \mathrm{P}$, sync negative (input 74 ohms terminated, 12 k ohms unteror <br> .OV $P / P$, video drive, sync positive at inimpedance: 75 ohms video termination, vertical and horizontal) <br> .0V $\mathrm{P} / \mathrm{P}$, video drive, negative vertical sync Min., 400 uSec max.), positive horizontal uSec min. to 30 uSec max.). (Input impeohms video termination, $>330$ ohms hori- <br> e, $\mathbf{>} 2 \mathrm{k}$ ohms vertical sync.) |
| RESOLUTION: | 650 lines center, 500 lines corners |  |
| VIDEO RESPONSE: | Within $-3 \mathrm{~dB}, 10 \mathrm{~Hz}$ to 12 MHz |  |
| LINEARITY: | Within 2\% as measured with standard EIA ball chart and dot pattern |  |
| HIGH VOLTAGE: | 9.0 kV at 50 uA beam current, nominal |  |
| HORIZONTAL RETRACE TIME: | 11.0 uSec maximum |  |
| SCANNING FREQUENCY: | Horizontal: $15,750 \mathrm{~Hz} \pm 500 \mathrm{~Hz}$; Vertical: $50 / 60 \mathrm{~Hz}$ |  |
| ENVIRONMENT: | Operating temperature: $0^{\circ} \mathrm{C}$ to $50^{\circ} \mathrm{C}$ <br> Storage temperature: $-40^{\circ} \mathrm{C}$ to $+65^{\circ} \mathrm{C}$ <br> Operating altitude: 10,000 feet maximum ( 3048 meters) <br> Designed to comply with applicable DHEW rules on X-Radiation <br> Designed to enable listing under UL Specification 478 |  |
| TYPICAL DIMENSIONS: | $4.60^{\prime \prime} \mathrm{H}, 5.12^{\prime \prime} \mathrm{W}, 8.68^{\prime \prime} \mathrm{D}$ (without power supply) ( $117 \times 130 \times 220 \mathrm{~mm}$ ) | $\begin{aligned} & 7.25^{\prime \prime} \mathrm{H}, 9.50^{\prime \prime} \mathrm{W}, 9.48^{\prime \prime} \mathrm{D}(184 \times \\ & 241 \times 241 \mathrm{~mm}) \end{aligned}$ |

* Specifications subject to change without notice.


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## SERVICE NOTES

## CIRCUIT TRACING

Component reference numbers are printed on the top and bottom of the plug-in circuit cards to facilitate circuit tracing. In addition, control names and circuit card terminal numbers are also shown and referenced on the schematic diagrams in this manual.
Transistor elements are identified as follows:
E - emitter, B - base, and C - collector.

## COMPONENT REMOVAL

Removing components from an etched circuit card is facilitated by the fact that the circuitry (copper foil) appears on one side of the circuit card only and the component leads are inserted straight through the holes and are not bent or crimiped.
It is recommended that a solder extracting gun be used to aid in component removal. An iron with a temperature controlled heating element would be desirable since it would reduce the possibility of damaging the circuit card foil due to overheating.
The nozzle of the solder extracting gun is inserted directly over the component lead and when sufficiently heated, the solder is drawn away leaving the lead free from the copper foil. This method is particularly suitable in removing multiterminal components.

## POWER TRANSISTOR REPLACEMENT

When replacing the "plug-in" transistor, please observe the following precautions:

1. The transistor heat sink is not "captive", which means that the transistor mounting screws also secure the heat sink. When installing the transistor, the heat sink must be held in its proper location.
2. When replacing the plug-in transistor, silicone grease (Motorola Part No. 11M490487) should be applied evenly to the top of the heat sink and bottom of the transistor.
3. The transistor mounting nuts must be tight before applying power to the monitor. This insures proper cooling and electrical connections. NON-COMPLIANCE WITH THESE INSTRUCTIONS CAN RESULT IN FAILURE OF THE TRANSISTOR AND/OR ITS RELATED COMPONENTS.

- NOTE -

Use caution when tightening transistor mounting nuts. If the screw threads are stripped by excessive pressure, a poor electrical and mechanical connection will be made.

## CRT REPLACEMENT

Use extreme care in handling the CRT as rough handling may cause it to implode due to high vacuum. Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for
protection. In addition, be sure to disconnect the monitor from all external voltage sources.

1. Discharge CRT by shorting 2nd anode to ground; then remove the CRT socket, deflection yoke and 2nd anode lead.
2. Remove CRT from chassis by loosening the one screw that secures the CRT mounting strap or retaining ring.
3. Install new CRT and proceed to horizontal linearity, centering and beam alignment procedures.

## HORIZONTAL OSCILLATOR ADJUSTMENT

- NOTE -

Not applicable to Model M1000-190.
Step 1. Turn on monitor and set up for normal operation.
Step 2. Locate the HORIZ. HOLD control, R35, on the Signal circuit card.
Step 3. Begin rotating R35 CCW until the video display is out of horizontal sync. At this point rotate R35 back CW until the video display just locks in horizontally; then stop. Using tape, mark the left-hand edge of the video display (not the raster edge) of the CRT faceplate.
Step 4. Continue rotating R35 CW until the video display is out of horizontal sync again in the opposite direction. At this point rotate 835 back CCW until the video just locks in horizontally; then stop. Mark the left-hand edge of the video display on the CRT faceplate again.

Step 5. Observe the distance between the two marks on the CRT faceplate. The object is to rotate the HORIZ. HOLD control, R35, until the left-hand edge of the video display is centered between the two marks on the CRT faceplate.

## VIDEO BIAS ADJUSTMENT

$$
\begin{gathered}
- \text { NOTE - } \\
\text { Not applicable to Model M1000-190. }
\end{gathered}
$$

Step 1. With the monitor operating, rotate the CONTRAST CONTROL, R6,for minimum contrast; then disconnect the input signal (s).

Step 2. Connect a voltmeter across R18 (negative probe toward the collector of Q4).

Step 3. Adjust the VIDEO BIAS control, R14, for a $+2.0 \pm .05$ volt indication.

Step 4. Disconnect the voltmeter.
Step 5. Reconnect the input signal(s) and adjust the CONTRAST control, R6, for desired contrast.

## HORIZONTAL LINEARITY ADJUSTMENT

- NOTE-

This adjustment procedure is required only when a CRT and/or deflection yoke have been replaced.

## PROCEDURE

Step 1. Disconnect monitor from power supply.


Figure 1. Partial View of CRT Neck/Deflection Yoke for Horiz. Linearity Adjustment

Step 2. (M20CO ON:Y) Locate the S-SHAPING transformer, $T 3$, on the deflection circuit card; then rotate its slug down to the borom. This action temporarily minimizes the effect of Theneng in the circuit.)
Step 3. (Refer to rigure 1.) Loosen the deflection yoke clamp somy just enough to permit sliding the copper sleeve on the CRT Mers back ant forth.

Step 4. (Reier to Figure 1.) Position the copper sleeve so that only $1 / 8^{\prime \prime} \uparrow 123^{\circ}$, extends out past the rear lip of the deflection vies. hatertion, be sute that the overlap edge of the cuper steve is anged moperly ond not twisted.




Step 5. Tighten the clamp scone carchitly we as not to diturts the yoke position.

Step 6 . Comoct the monhor to se power supply and set up for fratmal cperation.

Step 7. (Refer to Figure 2.) Observe the extreme lefthand edge characters (designated " $A$ " in Figure 2). Its width should be equal to the width of the right-hand edge characters (designated " $B$ " in Figure 2). If character " $A$ " is wider than character " $B$ ", the copper sleeve is extending out too far. If " $A$ " is narrower than " $B$ ", the copper sleeve should be pulled out further. In any event, the copper sleeve may have to be repositioned by trial and error if the 0.125 -inch dimension does not provide desired linearity. Continue until the width of character " $A$ " is equal to the width of character " $B$ ".

- NOTE -

Steps 8-11 are applicable only for the M2000 monitor.
Step 8. With the M2000 monitor turned on and operating normally, observe the width of the center character (designated " $C$ " in Figure 2). It should be narrower than characters " $A$ " and " $B$ ".

Step 9. Connect an oscilloscope (AC coupled) between the blue wire pin (on deflection circuit card) and chassis ground. A parabolic waveform should appear.

Step 10. Begin rotating the slug of T3 upward (away from circuit card) until the amplitude of the waveform is 125 volts $P-P$. This setting will equalize the width of character " $C$ " to that of characters " $A$ " and " $B$ ".
Step 11. Disconnect oscilloscope.

## RASTER CENTERING (Figure 1)

## - NOTE -

For Model M1000-190 refer to video centering. For models without beam alignment magnets, proceed to Step 2. Raster centering is factory set and should not normally require further adjustment.
Step 1. Position the tabs of the beam alignment magnets such that they are horizontally opposing.
Step 2. Adjust vert. size (R52) and horiz. width (L1) such that all edges of the raster are visible.
Step 3. Position raster centering magnets for best centering of raster.
Step 4. Readfuist size to specified dimensions or approx:mately $33 / 4^{\prime \prime}$ wide $\times 25 / 3^{\prime \prime}$ high for M1000 series and $6 \frac{1}{2} 2^{\prime \prime}$ wide $\times 4^{\prime \prime}$ high for M2000 series monitors.

VIDEO CENTERING (For M1000-190 only) (Figure 1)

- NOTE -

For models without beam alignment rings, procesd to Step 2. Video centering is factory set and should not normally require further adjustment.
Step 1. Position the tabs of the beam alignment magnets such that they are horizontaly opposing.
Step 2. Adjust vert. size (R52) and horiz. width (L1) suct that all edges of the video ard visible.


Block Diagram (Model M1000-190 only)


Block Diagram (All Models except M1000-190)

Step 3. Position raster eontering magnets for best centering of video.
Step 4. Readjust size to specfed dimensions or approximately 3 3/4" wide $25 / 8^{\prime \prime}$ high for M1000 series and $6 \frac{1}{2}$ " wide $\times 4^{\prime \prime}$ high ins whene series montors.

## CRT BEAM ALIGMREMT (Thare I)

For optimum charseter guatey in the comers of the video display, a beam aligment maphet may te used on the monitor CRT. If not used disragat the following procedure.

- NGTE -

Adjustmert of the rester centerng rings must precomb the aksustment of the bean alignment megnes.

## PROCEDURE

The beam alignment magnet should be positioned on the neck of the CRT between the deflection yoke and the tube base. The correct location of the rings is approximately over the second grid of the electroin gin ifigure 1 i.
Step 1. Adjust the display brightness for optimum viewing.
Step 2. Adjust the focus voltage for optimum overall focus.
Step 3. Loosen the beam alignment magnet clamping screw just enough to allow the assembly free movement on the CRT neck.
Step 4. While observing the tails on the dots in the corners of the display, rotate the focus rings to minimize the tails.
Step 5. Tighten the clamping screw.

## THEORY OF OPERATOM

## GENERAL

The following cicut derchation is ppliceble to monimers using a composto video ingut signal. For rooniters using TTL inputs, he descrptor is bscicely the sene fowever, the horizonte: and vatide syne puses are coupled trom an
 pers JU 1 and JUZ wht to rabored to the Th posken.
 circuity. The devepmont and procsing of the driving signals is portemst asteraly from the montor and apliod to separath inputs smide tw the Th moceis, Thotote.
 direct orive wersign. Gee ghoch warams.

## VIDEO AMPLIFIER CIRCUIT (Figure 3.)

The video amplifier consists of four stages that include Q1, Q2, Q3 and Q4. The first stage, Q1, functions as an emitter follower. The low output impedance of this first stage permits use of a low resistance CONTRAST control, R6, which furnishes flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the sync separator, Q 5 . Capacitor C 2 provides high frequency roll-off to limit the collector output to the bandwidth required to pass synchronization signals.

Transistors Q2 and Q3 form a direct coupled amplifier with frequency compensation provided by C 40 and C 41 . The output from Q3 is capacitively coupled (C5) to the base of Q4, video output stage. The video bias control, R14, is used to set the quiescent collector current of O 4 . Frequency compensation is provided by R17 and C6. The combined action of clamping diode D1 and capacitor C5 provide DC restoration for the video signal.


Figut 3. Video Amplifier Circuit

Components C7, D2 and R19 provide CRT beam current limiting. Diode D2 is normally forward-biased; therefore, as $\mathrm{Q4}$ conducts, its collector voltage drops. This causes a larger beam current to flow through R19, which in turn causes its voltage drop to rise. If excessive beam current flows, the voltage developed across R19 becomes greater than the collector voltage of O 4 . This action reversebiases D2, which prevents a further increase in beam current. Capacitor C7 helps couple video to the CRT cathode, pin 2, through R20. Resistor R2O is used to isolate 04 from transients that may occur as a result of CRT arcing.

## SYNC SEPARATOR/AMPLIFIER CIRCUIT

 (Reference Figure 4.)The sync separator employs two stages. Transistor 05 is the sync separator and Q 6 is the sync amplifier. The video input to the sync separator is black positive. Capacitor C3 is charged by the peak base current that flows when the positive peak of the input takes $\mathbf{O 5}$ to saturation. This charge depends on the peak to peak input to $\mathbf{Q 5}$ and thus makes the bias for 05 track the amplitude of the input signal. As a result, $\mathbf{Q} 5$ amplifies only the positive peaks of the input signal. The initial bias current through R23 sets the clipping level.


Figure 4. Sync Separator/Amplifier Circuit

## PHASE DETECTOR (AFC)

(Reference Figure 5.)
The phase detector control consists of two diodes (D3 \& D13) in a keyed clamp circuit. Two inputs are required to generate the required output, one from the sync amplifier, Q6, and one from the horizontal output circuit, Q8. The required output must be of the proper polarity and amplitude to correct phase differences between the input horizontal sync pulses and the horizontal time base. The horizontal output ( Q 8 ) collector pulse is integrated into a sawtooth by R28, C13 and R29. During horizontal sync time, both diodes conduct, which shorts C 13 to ground. This effectively clamps the sawtooth on C13 to ground at sync time. If the horizontal time base is in phase with the sync (waveform A), the sync pulse will occur when the sawtooth is passing through its AC axis and the net charge
on C 13 will be zero (waveform B). If the horizontal time base is lagging the sync, the sawtooth on C 13 will be clamped to ground at a point negative from the AC axis. This will result in a positive DC charge on C 13 (waveform C). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag. Likewise, if the horizontal time base is leading the sync, the sawtooth on C 13 will be clamped at a point positive from its AC axis. This results in a net negative charge on C13, which is the required polarity to slow the horizontal oscillator (waveform D).
Passive components R30, R31 and C16 comprise the phase detector filter. The bandpass of this filter is chosen to provide correction of horizontal oscillator phase without ringing or hunting. Optional capacitor C14 (when present) times the phase detector for correct centering of the picture on the raster.


Figure 5. Phase Detector (AFC) Circuit

## HORIZONTAL OSCILLATOR AND DRIVER

(Reference Figure 6.)
The horizontal oscillator consists of integrated circuit IC1, which is essentially a voltage controlled oscillator with variable mark-space ratio (duty cycle) and internal voltage reference. The reference voltage is present at pin 6, while resistors R37 and R38 determine the mark-space ratio. The main oscillator timing capacitor is C 17 , with its charging current derived from three sources: (a) a fixed current from R33, (b) a variable current from R34 and HORIZ. HOLD control R35, (c) and a correcting current from the phase detector (AFC) network through R32. The combination of these three charging currents and C17 determine the horizontal frequency.


Figure 6. Horizontal Circuit

The output from IC1 (pin 1) is a square wave of proper frequency and duration, which is applied to the base of horizontal driver 07 . The output from $\mathrm{Q7}$ is coupled via the horizontal driver transformer T1 (current step-up) to the base of horizontal output device Q8. Components R41 and C19 provide current limiting, while components R40 and C18 provide transformer damping to suppress ringing in the primary of T2 when Q7 goes into cutoff.

## HORIZONTAL OUTPUT

(Reference Figure 6.)
The secondary of T1 provides the required low drive impedance for 08 . Once during each horizontal period, 08 operates as a switch that connects the supply voltage acros: the parallel combination of the horizontal deflection yoke $\{[3-A)$ and the primary of the high voltage transformer, T 2 . The required sawtooth deflection current (through the horizontal yoke) is formed by the L-R time constant of the yoke and primary winding of transformer T2. The horizontal retrace pulse charges C33 through D7 to provide +87 V .

Momertan transients at the collector of 08 , should they occur, afe jimited to the voltage on C33 since D7 will conduct it the collector voltage exceeds this value.

The cimper diode, D10, conducts during the period betwees resace and turn on of O8. Capacitor C20 is the retracs runing capacitor. Coil L1 is a series HORIZ. WIDTE wnitrol. Components C32 and D8 generate a negative valuge necessary to properly bias the CRT. A copper sleeve of the neck of the CRT shapes the horizontal magnetic fed for proper linearity.

Pin 4 of the high voltage transformer, T2, is a boost windirs. which together with components D11 and C34, develops +400 volts for G2 of the CRT. This same +400 volts is aise always present on the high side of FOCUS control fey.

- NOTE -

In the M2000 monitor (only), an S-shaping transformer, T3, and capacitor C44 provide additional shaping of the horizontal deflection yoke current for proper linearity.

## DYNAMIC FOCUS (M2000 ONLY)

(Reference Figure 6.)
Due to the geometry of a CRT, the electron beam travels a greater distance when deflected to a corner as compared to the distance traveled at the center of the CRT screen. As a result of these various distances traveled, optimum focus can be obtained at only one point. An adequate adjustment can be realized by setting the focus while viewing some point midway between the center of the CRT screen and a corner, thus optimizing the overall screen focus. One of the simplest methods for improvement is to modulate the focus voltage at a horizontal sweep rate. Now optimum focus voltage is made variable on the horizontal axis of the CRT, which compensates for the beam travel along this axis.

In the M2000, the secondary of T3 generates a parabolic voltage, which together with a fixed voltage from the FOCUS control R61, is applied to the focus grid of V 1 . This system dynamically changes the value of focus voltage from the CRT screen center to screen edge, which will always provide an optimum amount of voltage for best overall focus.

## VERTICAL OSCILLATOR, DRIVER AND OUTPUT (Reference Figure 7.)

Composite sync pulses from the collector of Q6, Sync Ampl., are applied to the double integrating network of R45, C23, R46 and C24. The horizontal component of the sync signal is removed, leaving only the vertical sync pulses. The vertical sync pulses are coupled to the free running ver-


tical oscillator stage, Q10, by C25 and R47. Transistors Q10 and Q12 are connected as a multivibrator. Transistor Q11 is used as an emitter follower that provides a low impedance drive for the vertical output stage, Q12. The series combination of capacitors C27 and C28 are initially charged to the supply voltage through R53 and the VERT. SIZE control, R52, which generates an exponential ramp of voltage.

When a positive vertical sync pulse is applied to the base of Q10, it begins conducting, which immediately discharges C 27 and C28. This action turns off Q11 and causes a sudden decrease in the collector current of Q12, which also decreases the vertical deflection current through deflection yoke (L3-B) and vertical choke (L2). The resultant rapidly collapsing field in $\mathbf{L} 2$ generates a large voltage spike that is used for vertical retrace. Components R58, C29, R51 and C26 shape this spike to ensure that 010 remains conducting until retrace is carried out to completion. Diode D4 couples the shaped spike to the base of Q10. At this point, Q10 reverts to its non-conducting state and the cycle repeats. The VERT HOLD control, R49, and R48, provide a feedback signal to 010 to maintain oscillation in the event vertical sycn pulses are not present. Diodes D5 and D6 provide the proper voltage drops to operate Q12 class $A$.

Vertical linearity is maintained by applying the ramp voltage generated across R59, through R57 (VERT LIN control) and R54, to the junction of C27 and C28. Since this path is resistive, the waveform will be integrated into a


Figure 8. Blanking Amplifier
parabola by C 27 (Waveform A). This results in a predistortion of the ramp waveform (waveform C). (Waveform 8 illustrates the drive sawtooth without parabola shaping.) Parabolic shaping is necessary to compensate for the nonlinear charging of C27 and C28, and the impedance change occuring in L2 with current. Capacitor C31 serves to remove the DC component of the vertical deflection yoke current. Diode D9 clamps the collector voltage of Q12 to a safe level.

## RETRACE BLANKING (NOT ON M1000-190) <br> (Reference Figure 8.)

Retrace blanking is provided by negative-going horizontal and vertical rate pulses applied to G1 of the CRT. The collector pulse from the horizontal output stage, Q 8 . is developed across R43 through R42 and C22. The collector pulse from the vertical output stage, Q12, is differentiated by C21 to remove the sawtooth portion of the waveform. The remaining pulse appears across R43. The mixed vertical and horizontal pulses on R43 are amplified and inverted by the blanking amplifier, 09, and applied to G1 of the CRT.


Wodel M1000 - Rear Chassis View


Model M2000 - Rear Chassis View


Deflection Circuit Card - Component Side


Deflection Circuit Card - Solder Side


Signal Circuit Card - Component Side (All Models except M1000-190)


Signal Circuit Card - Solder Side (All Models except M1000-190)


M1000 - 100, 155 and M2000 - 100, 155, 355 - Schematic Diagram









1 His...5



St edge connector socket



2.4p



Signal Circuit Card - Component Side (Model M1000-190)


Signal Circuit Card - Solder Side (Model M1000-190)

REPLACEMENT PARTS LIST

| PEF. No. | PART <br> Number | DESCRIPTION | REF. NO. | PART NUMBER | DESCRIPTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GhOUT CABDAESEMBLES: (COMPLETEWITHAL |  |  | C45 | 8S10212052 | 0.1. 100V: Cer. Disc |
|  |  |  | C46 | 23S10229A32 | 1.0. 16V: iytic |
|  | duv 25012 A 05 | Deflection Circuit Card (Cpt.) ( $M$ 1000-100, 155) |  |  |  |
|  | 84025651485 | Deflection Circuit Card (Cpt.) (M1000-190) (M1000-190) | D1 | 48R02054A00 | Diode, Low Power: 2054 |
|  | 54V25014\%30 | Defection Circuit Card (Cpt.) | D2 | 485191405 | Rectifier, Silicon; 91A05 |
|  |  | (2000-155, 355) | D3-D6 | 48R02054A00 | Diode, Low Power; 2054 |
|  | av2603am | Gsym Circuit Card (Cpt.) <br> (Al: models except M1000-190) | D7-D9 | 485191 A05 | Rectifier, Silicon: 91405 |
|  |  |  | D10 | 485134921 | Diode, D1D |
|  | 82V25551n8 | Gignel Circuit Card (Cpt.) ( $\mathrm{m} 1000-190$ ) | D11 | 48R134978 | Rectifier, Silicon: D1K |
|  |  |  | D12 | 485137608 | Diode, D9H (M1000 only) |
|  |  |  | D12 | 48 S 137622 | Diode, D9N (M2000 only) |
| capathors: |  |  | D13 | 48R02054A00 | Diode. Low Power: 2054 |
|  | inat wilus the in microfarads unless o noted |  | D14 | $48 S 137495$ | Diode, IN 139 (M1000-190 only) |
| 0 | $23610 \% 66$ | $22,40 \mathrm{y}: \mathrm{ty} \text { tic }$ | INTEGRATED CIRCUITS: |  |  |
| ¢ | 218490064 | $\begin{aligned} & 33 \text { pr } 10 \mathrm{E}, \mathrm{~N} 750,100 \mathrm{~V} \text {; } \\ & \text { Ger. Oisc. } \end{aligned}$ | IC1 | 51S10778A01 | MC1391P; T3L |
| 0 | 831029598 | . 01 10\%, 250V; Polyester | COILS/CHOKES: |  |  |
| C4. 5 | $\begin{aligned} & 2359 \mathrm{man} 8 \\ & 2159 \operatorname{cose} \end{aligned}$ | 2] 40v: ytic | L1 |  |  |
| Cl |  | A70 \% $10 \%$, X5F; Cer.Disc |  | 24025603A03 | Coil, Horiz. Width (M1000 only) |
| 0 | 6swameat | 02290\%, 250V; Mtiz Poly | 12 | 24025603A04 | Coil, Horiz. Width (M2000 only) |
| + | 218150cs2 | tepr ${ }^{\text {cta }}$, NPO; Cer. Disc | L2 | 25D25221A09 | Choke, Vert. Out |
| ¢ | 23510255400 | 100. 50 v : lytic | L3 A/B | 24025290A02 | Yoke, Deflection (M1000 only) |
| 90 |  | 330 pr 10\%, X5F; Cer.Disc | L3 A/B | 24068531A03 | Yoke, Deflection (M2000 only) |
| Ot |  | 20ef 10\%, X5F; Cer.Disc |  |  |  |
| 02 | 21518085 | a 70 pr $10 \%$, X5F; Cer. Disc | TRANSISTORS: |  |  |
| 10 | 21515004: | .002, 10\%, Z5F; Cer.Disc | Q1 | 48S134997 | 1st Video Ampl.; A3K |
| Ca | 9510191891 | . 41 10\%, 250V; Polyester | Q2 | 485137127 | 2nd Video Ampl.; P2S |
| $0 \cdot 6$ | 2031022943? | 1.0, 16V, Tant. Iytic | Q3 | 485137172 | 3rd Video Ampl.; A6J |
| c\% | 85,020062 | hez 10\%, 400V: Poly Carb | Q4 | 485137093 | Video Output: A5F |
| \%\% | Guteters | ف2\% tos, 400V; Polyester | 04 | 485134919 | Video Output; A1M |
| C13 | 257010102 | $0.140 \%$, 250 V ; Polyester ${ }^{\text {- }}$ |  |  | (M1000-190 only) |
| ca | 83100724046 | .04\% $10 \%$, 200V; Polyester | Q5 | 485137171 | Sync Sep.; A6H |
| ¢ | Esp191602 | $0.110 \%$, 250V; Polyester | 06 | 485137127 | Sync. Ampl.; P2S |
| 02 | 2136009 | csef +2.5 NPO; Cer.Disc | 07 | 485137169 | Horiz. Driver; A6G |
| cas | 85398189 |  | 08 | 485137462 | Horiz. Output; A9Z |
| COF | 2whers | ,02, 00 , Z5F; Cer. Disc | 09 | 485137172 | Blanking Ampl.: A6J |
| C6 | actusters | D: $50 \% .250 \mathrm{~V}$; Polyester | 09 | 485137172 | Vert. Sync; A6J (M1000-190 only) |
| 025 | 85019188 |  |  |  |  |
|  |  | (M10co-190 only) | Q10 | 485137172 | Vert. Osc.; A6J |
| cas | astangess | , ¢e 10\% 250V; Polyester | 011 | 485134997 | Vert. Driver; A3K |
| 627.23 |  | 80, 15v, Tant.lytic | Q12 | $48 S 137598$ | Vert. Output; B2Y |
| ca |  | .5.th\%, 200v: Polyester |  |  |  |
| Cos | sstoyeate | D: 4\%, ¢0VV: Polvester | RESISTO | /CONTROLS: |  |
| \% |  | 4 70 , svamic | Note: | Oniy power or special resistors are listed. Use the description when ordering standard values of fixed carbon resistors up to 2 watts. |  |
| Ca 2 |  | Wi P\%M. AOOV Polyester |  |  |  |  |
| C 33 | $\begin{aligned} & 238+c, 55 A 74 \\ & 831010+609 \end{aligned}$ | 2a, weratys |  |  |  |  |
| C3 |  | 04, 50. 400 V ; Polyester |  |  |  |  |
| cas | Es?0212e20 | क.es hele y | R6 | 18D25245A02 | Control. Contrast 1k |
| C36 | 2tsisocat | .00n $50 \%$, 2 SF, 500 V ; Cer.Disc | R14 | 18D25245A02 | Control. Video Bias 1 k |
| 03 | 6s1060,653 | a.22 10\%, 加\% Polyester | R18 | 17S10731A03 | 1.5k 5\%, 5w; Wire Wound |
| c3 | $\begin{aligned} & 2551095503 \\ & 2: 5,00607 \end{aligned}$ | 1509, 89, etis | R35 | 18C25267801 | Control, Horiz. Hold 22k |
| \% |  | 150m the M150: Cer.Disc | R49 | 18025245A15 | Control, Vert. Hold 100k |
| cos | 2:560062 | dap ave N150: Cer.Disc | R52 | 18025245A20 | Control, Vert. Size 50k |
|  |  | (16\%000-190 only | R57 | 18025245A10 | Control, Vert. Lin. 1.5k |
| 0.4 | 2151868e3 |  cer ane | $\begin{aligned} & \text { R61 } \\ & \text { R63 } \end{aligned}$ | $\begin{aligned} & 18 \mathrm{D} 25245 \mathrm{~A} 12 \\ & 18 \mathrm{D} 25245 \mathrm{AO} \end{aligned}$ | Control, Focus 2 Meg. <br> Control, Brightness 500k |
| Cat | $\begin{aligned} & 215: 30 c 32 \\ & \text { csioseng71 } \end{aligned}$ | 33 F 10\% Ni50; Cer. Disc |  |  |  |
| CA: |  |  | T1 | 25025221A04 | Transformer, Horiz. Driver |

REPLACEMENT PARTS LIST (Continued)

| REF. NO. | PART NUMBER | DESCRIPTION | REF. NO. | PART <br> NUMBER | DESCRIPTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $T 2$ | 24D25291E02 | Transformer, High Voltage (M1000 only) |  | 26C25198A03 | Heat Sink (for Q8) <br> Heat Sink (for Q12) |
| T2 | 24D25291D03 | Transformer, High Voltage (M2000 only) | S3 | 15S10183A87 | Housing, Recept.: 3-contacts (less contacts) |
| T3 | 24C25602B01 | Transformer, S-Shaping (M2000 only) |  | $\begin{aligned} & 39 S 10184 A 72 \\ & \text { 14A25340A01 } \end{aligned}$ | Contact, Recept. (3 req'd.for S3) Insulator, Hi-Voltage Standoff (M2000 only) |
| MISC. ELECTRICAL PARTS: |  |  |  | 59C25465A02 | Magnet, Focus (M2000 only) |
| V1 | 96S10769A01 | 5"- CRT, Type No. 140ANB4 (M1000 only) |  | 2S10054A36 | Nut, Clip-on No.8-18 (M1000 only) |
| V1 | 96R2500A14 | 9"-CRT,Type M24-304W/10TS5497A <br> (M2000-155 only) |  | $\begin{aligned} & \text { 42C25258A01 } \\ & 3 S 138210 \end{aligned}$ | Retainer, CRT (M1000 only) Screw, No. 8-18 $\times 1-1 /{ }^{\prime \prime}$ |
| V1 | 96R02500A23 | 9**-CRT (M2000-355 only) |  |  | (M1000 only) |
| V1 MECH | 96R02500A22 AL PARTS: | $\begin{aligned} & \text { 9"- CRT (M2000-201, } \\ & \text { M2000-255 only) } \end{aligned}$ |  | $\begin{aligned} & \text { 26C25323A01 } \\ & 9 \mathrm{D} 25241 \mathrm{~A} 04 \end{aligned}$ | Shield, Linearity (CRT) <br> Socket, CRT (Incl. leads \& resistors R20, R65, R66 \& R67) |
| MECHANICAL PARTS: |  |  |  | 41825268A03 | Spring, CRT Aquadag (M1000 only) |
|  | 14B25751A01 42D25298A03 | Collar, "C" (CRT Neck) Connector, Anode (M1000 only) |  | 41065987 A 01 | Spring, Special; CRT Aquadag gnd. <br> (M2000 only) |
|  | 42D25298A08 | Connector, Anode (M2000 only) |  | 42D67027A14 | Strap, CRT Mitg.(M2000 only) |
| S1 | 9S10768A01 | Connector, Receptacle; Header |  | 7S10747A02 | Support Guide, Circuit Card |
| P3 | 28S10586A 14 | Conn., Circuit Card; 3-contacts |  |  |  |

