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Colin Hinson

In the village of Blunham, Bedfordshire, UK.

Proposed new No Break Trigger system

designed by

Chief Technician Colin Hinson

and

Sergeant Tony Mellor

After some 6 years of operation it became apparent that the original No Break Trigger system was a cause of many hours of the station being “off the air”. Tony and I therefore decided that we would have a go at designing a semiconductor version of the (then) current valved system.

We designed what you see in this document between us and solved the problems that cropped up between us so that we both knew how the whole thing worked. The printed circuit boards were designed and made by us using copper plated boards from Vero Electronics who also supplied the 19 inch rack assembly.

Having got the “box” working, we obtained permission to connect it as the trigger source for the Type 85 radar, along with its ancilliary equipments (such as IFF etc). To my knowledge this ran for at least 5 years with no problems.

This document is the original scanned version. A modernised version of the document are available on this site.

Colin Hinson, Oct. 2017.

PROPOSED NEW NO-BREAK TRIGGER SYSTEM

SECTION 1 - NEW NBT SYSTEM

General Introduction

1. This paper discusses a design for a No-Break Trigger System which could be utilised at R.F radar stations where a high standard of timing precision and reliability is required. The equipment is capable of working in a wide range of environments and over the temperature range 0.C to 50.C requires no forced air cooling.

NBT System

2. ADRS's are triggered from an NBT equipment developed from early synchronising systems. This equipment has since its introduction been considerably modified in an effort to increase its reliability. However its serviceability still falls short of a working ideal.

3. The new NBT system is introduced in order to improve reliability and serviceability of the trigger system.

General Equipment Description

4. The equipment is mounted on 5 basic types of printed circuit board which are housed in a "Verorack", 19" rack assembly. This rack will mount directly into a 7' Sainsbury cabinet.

5. Power supplies are mounted in the same cabinet and are fed from the A.C. mains supply. Bulk D.C. power supplies are not required.

System Description

6. The equipment contains duplicated crystal oscillators, dividers and trigger output circuits. Each major sub-division of the equipment is mounted on its own printed circuit board. All active auto-changeover components are mounted together on one board, the system may be run manually with all automatic fault detection circuitry disabled on removal.

7. The input to the system is designed to interface with the PRF control system in the Radar Type 84 MTI equipment.

8. The output triggers are compatible with the trigger inputs to all the equipments currently in use at ADRS's.

9. The existing underfloor mounted pulse distribution unit and the wall mounted pulse indicator panel are not required with the proposed system.

SECTION 3 - BRIEF TECHNICAL DESCRIPTION OF SYSTEM

Refer to Annex

Oscillator Board

1. The 4Mhz oscillator is similar to the one used in the present NBT system, this is so that compatibility between the unit and the external PRF control system may be maintained. The 4Mhz nominal crystal frequency is converted to TTL levels and divided by 16 before leaving the board. The 250 kHz output is routed to both divider boards, the switching between main and standby oscillators is accomplished electronically on the divider boards.

2. A 500 Hz square to sine converter is also housed on this board, this accepts a 500 Hz logic level square wave from the in use divider. The 500 Hz sine wave output is routed to the PRF control system.

3. Both the 250 kHz and the 500 Hz signals are checked to ensure correct operation by the fault detection circuit on the board. The output of the fault detector is fed to the control board where it is used to initiate auto changeover in the event of a failure.

4. LEDs indicating "In Use" and "Fault" conditions are mounted on the front panel.

Divider Board

5. The 250 kHz signal from the in use oscillator is divided by a series of bistables down to 250 Hz. Gating circuits accept outputs from individual bistables and generate the six timing pulses.

6. An align facility is provided so that the divider which is not currently in use may be kept exactly in step with the in use divider. This ensures that the output pulses from each board are precisely in line with each other and no timing errors will occur if changeover of divider boards takes place.

7. Each output from the board is monitored and a fault signal is sent to the control board should any output become unserviceable. In addition to the pulse outputs a 500 Hz square wave is sent from the in use board to the oscillator.

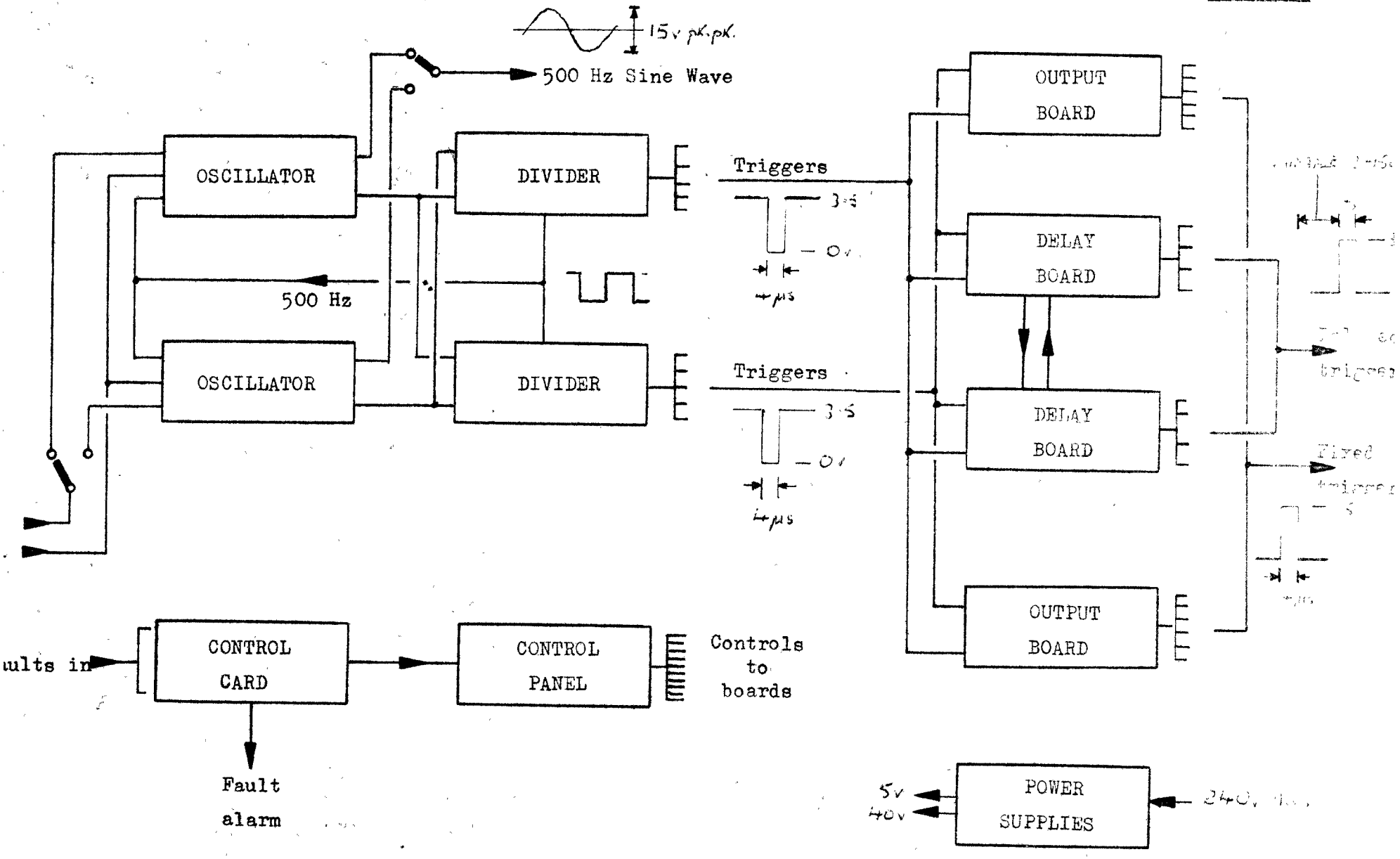
8. The front panel carries "In Use" and "Fault" indicators.

Output Board

9. Two boards are used simultaneously to provide the output triggers, however the output circuit configuration is such that if one driver fails the other will continue to function and no loss of triggers will occur.

10. Both dividers feed the boards, selection of a particular divider is performed by the input gating on the output boards.

11. Each board has 6 outputs of 35 volt, 4us wide positive going pulses. Additional triggers are catered for by providing extra pairs of boards. The front panel carries monitor sockets and trigger presence indicators.


15v pk.pk.
500 Hz Sine Wave
OSCILLATOR
DIVIDER
500 Hz
OSCILLATOR
DIVIDER
Triggers
3·5
0v
4μs
Triggers
3·5
0v
4μs
OUTPUT BOARD
DELAY BOARD
DELAY BOARD
OUTPUT BOARD
ults in
CONTROL CARD
CONTROL PANEL
Controls to boards
Fault alarm
5v
40v
POWER SUPPLIES
240v

SECTION 2 - SYSTEM SPECIFICATION

PRF — Controlled by crystal stabilised oscillator, fine control by T84 MTI system.

$$\text{Basic PRF} = \frac{\text{Crystal frequency (kHz)}}{16.384} \text{ pps.}$$

PULSE WIDTH — 4us.

500 Hz REFERENCE — Subdivision of oscillator frequency.

POWER REQUIREMENTS — 5 volts at 3 amperes ± 5%
40 volts at 1 ampere ± 5%

OUTPUT TIMINGS — Fixed triggers, referenced to "Zero" trigger.

(1) Zero
(2) -8us.
(3) -125us.
(4) -250us.
(5) -750us.

Delayed triggers, delayed by from 2us to 15 0us on any of the fixed triggers.

TRIGGERS AVAILABLE — Each delay board gives 4 outputs and each output board gives 6 outputs. The basic system may be extended in multiples of these figures by adding additional pairs of boards.

TRIGGER OUTPUT — Both the delay and the output boards use the same output circuit configuration. The output is capable of producing 100ns rise time triggers at the remote end of 100 metres of UR70 cable. The rise time is only degraded to 25 0ns when driving 800 meters of low loss cable.

The output is open and short circuit proof.

Delay Board

12. This board accepts the outputs from the dividers and produces delayed triggers 35 volts amplitude and 4us wide.

13. Each pair of delay boards have their delay circuits cross coupled, this ensures that both boards produce outputs at the same time even if one delay has been incorrectly set.

14. The front panel carries monitor sockets, trigger presence indicators and delay controls.

Control Board

15. The control board monitors the outputs of every other board within the system and controls the automatic changeover between boards. The power supplies are monitored but since they operate in parallel no switching is necessary.

16. When any fault is detected an alarm signal is generated and a record of the part of the equipment which failed is kept. This record is in the form of a LED display on the control panel which is kept lit until reset manually.

Power Supplies

17. Supplies of 5 volts and 40 volts are used within the system. Small modular units are used fed from the 240 volt mains supply. Duplicate supplies are paralleled together, this ensures operation without break in the event of supply failure and eliminates the need for switching.

SECTION 4 - DETAILED TECHNICAL DESCRIPTION

Part 1 - Oscillator board

Part 2 - Divider board

Part 3 - Output board

Part 4 - Delay board

Part 5 - Control board and control panel

Part 6 - Rack wiring

SECTION 4 - PART 1 - OSCILLATOR BOARD

General Description

1. The oscillator board provides the highly stable frequency used to feed the divider boards. It also accepts a 500 hz square wave from the in use divider and converts this into a sine wave for use in the T84 signal processing system.

2. The board is powered from the 5 volts and 40 volts supply.

Oscillator

3. The oscillator is of the inverted Hartley type with VT2 source following into VT1, thus providing a high impedance input and a low impedance feedback path to the tap of L3. The main resonant circuit consists of L3, C3 and variable capacitor VC1. The oscillator is stabilized by crystal XL1 and is capable of being swung ±20 kHz about the crystal frequency of 4.000 or 4.078 MHz by VC1. L1, L2, C1, C2 and R1 form the network required to broaden the basic crystal response.

4. A second source follower, VT3, is fed from VT2, this isolates the oscillator from the waveform shaper VT4. Capacitor VC1 is motor driven and is controlled by the P.R.F. controller in the cancellation cabinet of the T84 signal processing. VT4 squares the output from the oscillator and feeds directly into IC3, a four bit binary counter. The 250 KHz output from IC3 is taken from the board and feeds the two divider boards. The 250 KHz output also feeds IC2 which is a retriggerable monostable. The timing cycle of IC2 is set by C8 and R11 to be 5uS. Since the periodic time of the input is 4uS, the monostable will be retriggered before the completion of the timing cycle and therefore the Q output will remain at logical 1 and the $\overline{Q}$ at logical 0. Should the oscillator/4 bit counter fail then the monostable will revert to its stable state within 5uS. The Q will go to logical 0 and be inverted twice by IC1c and IC1b and present a logical 0 at the clear input of IC2. This will hold the Q at logical 0 and therefore the monostable will latch in its stable state. The fault output from the $\overline{Q}$ is fed to the control board fault circuitry. The Q output going to logical 0 grounds the cathode of LED1, the fault indicator causing it to light. The logical 0 output of IC1A is fed from the board to light the Oscillator fault LED on the control panel. The reset line for the monostable comes from the pulse generator on the control board to IC1b. When this line goes to logical 0 it allows the clear line to go to logical 1. If the fault is cleared, the monostable will be retriggered by the 250 KHz and allow the clear to remain at logical 1 when the reset pulse ends and both fault LEDs will go out.

5. If the fault persists, the monostable will not retrigger and the fault output from the $\overline{Q}$ will remain at logical 1.

500Hz Generator

6. A square wave at 500Hz is taken from the in use divider and fed to VT5 via the shaping network R14, R15, C13, and C14. VT5 is arranged as a phase shift oscillator but with insufficient gain to sustain oscillation independantly due to the undecoupled emitter resistor R21. The application of the shaped square

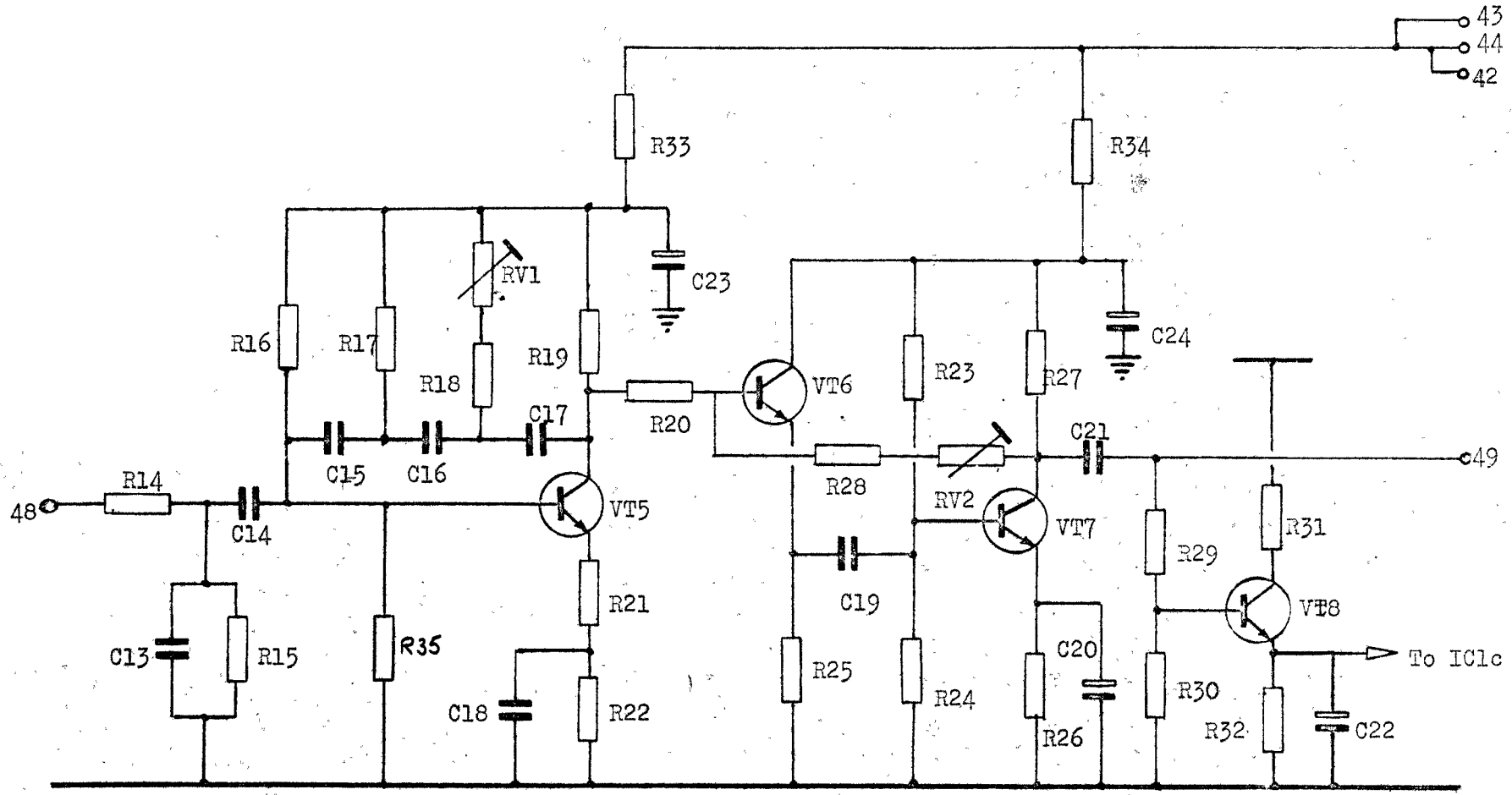
500Hz Generator (Continued)

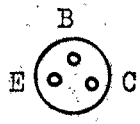
wave to VT5 causes it to oscillate, locked in phase to the 500Hz sub-multiple of the crystal frequency. RV1 sets the gain of VT5 to a maximum over the required range and only requires adjustment when the crystal frequency is changed.

7. The sine wave output of VT5 is buffered by emitter follower VT6 and fed to amplifier VT7. Negative feedback is taken from VT7 collector to VT6 base, the amount of feedback being set by RV2. Thus RV2 adjusts the gain of VT6 and VT7 and so sets the amplitude of the output sine wave.

8. A sample of the output is taken to VT8 through R29. The positive peaks of the sinewave cause VT8 to conduct allowing C22 to charge up through VT8 and R31. C22 is normally charged to approximately 4 volts, holding the input to IC1c at logical 1. If the 500Hz fails, VT8 is cut off and C22 discharges through R32. R32 is sufficiently low in value to pull down the input to IC1c to logical 0 and the monostable will latch as before. The time taken for C22 to discharge through R32 to below the threshold of IC1c introduces a short delay in the time taken for the 500Hz fault circuit to trip. This ensures that in the event of a divider failure causing loss of 500Hz, the divider changeover will operate before the loss of 500Hz is detected.

9. To indicate the in use oscillator card, an in use signal is fed from the oscillator selection switch to IC1d. When the in use signal is at logical 1 the output of IC1d goes to logical 0 causing the in use light LED2 to come on.

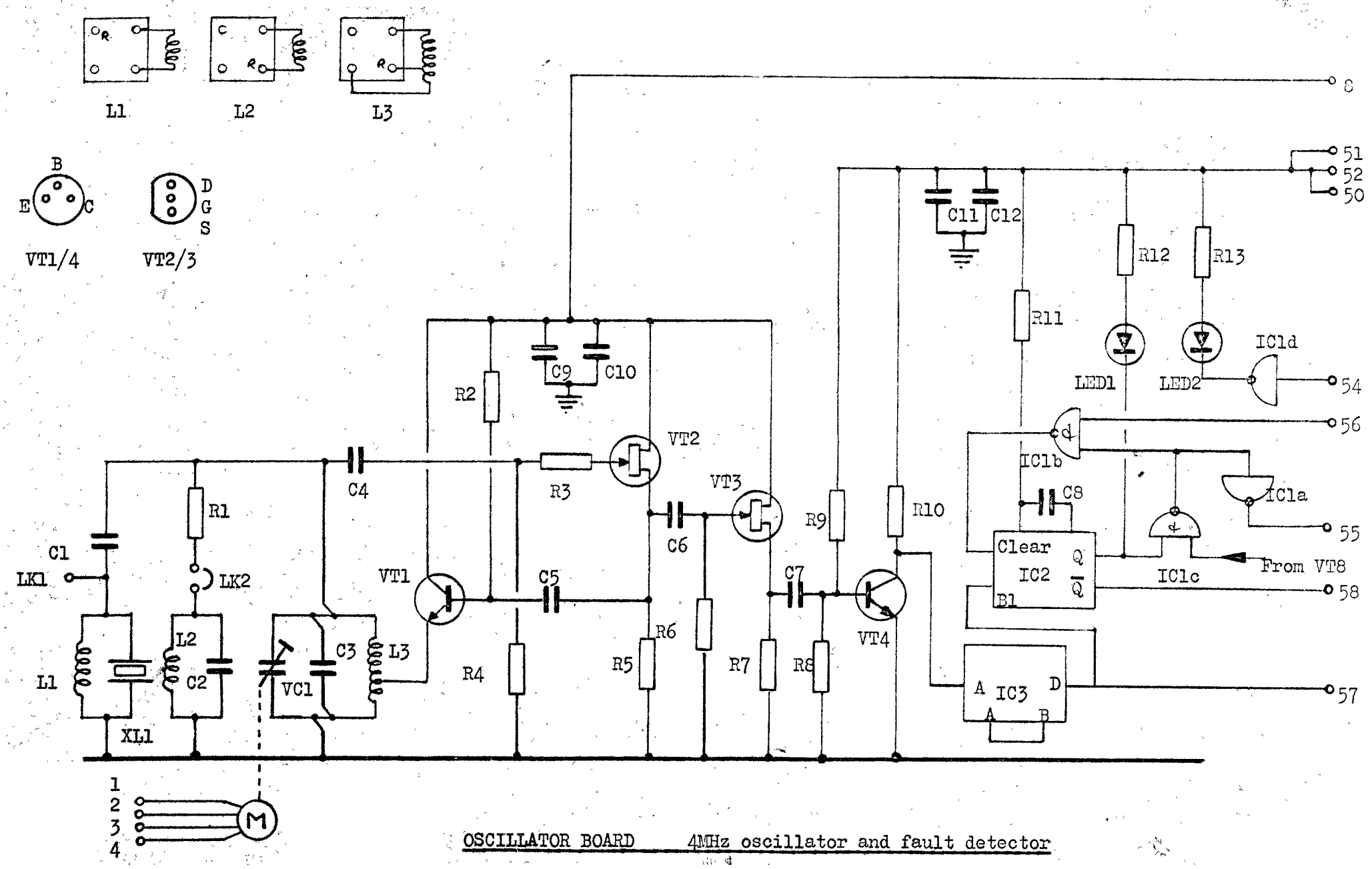




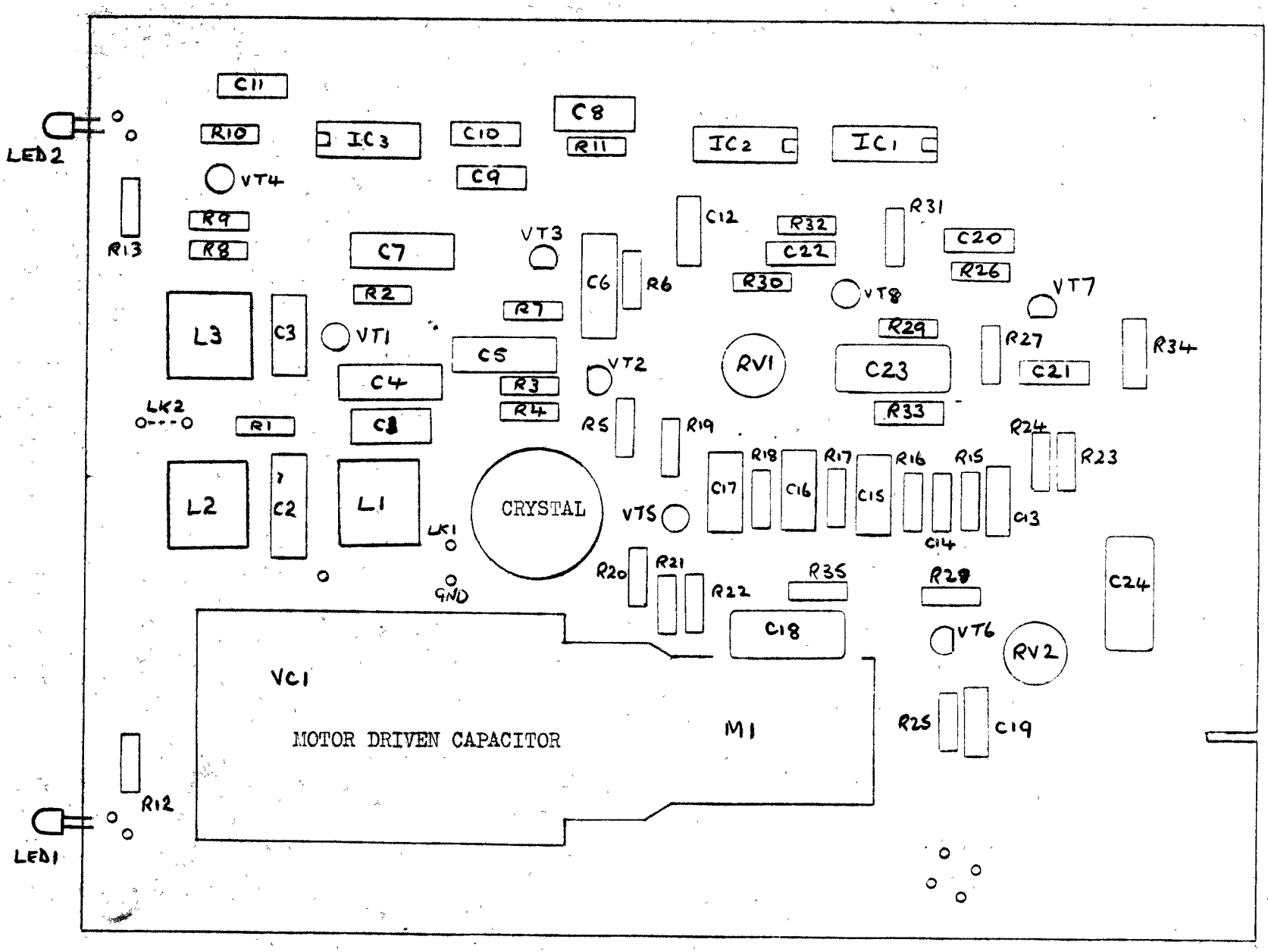
VT5/8

VT6/7

OSCILLATOR BOARD 500Hz convertor



OSCILLATOR BOARD 4MHz oscillator and fault detector



OSCILLATOR BOARD Layout

ANNEX D TO
SECTION 4
PART 1

OSCILLATOR BOARD - LIST OF COMPONENTS

R1	470R	10W	0136108
R2	56k		0136158
R3	390R		0136106
R4	100k		0136164
R5	1k0		0136116
R6	390k		0136057
R7	1k2		0136118
R8	18k		0136146
R9	56k		0136158
R10	1k8		0124709
R11	15k		0136144
R12	270R		
R13	270R		
R14			
R15	6k8		0136136
R16	56k		0136158
R17	15k		0136144
R18	12k		0136142
R19	12k		0136142
R20	100k		0136164
R21	27R		
R22	820R		0136114
R23	10k		0136140
R24	1k8		0124709
R25	4k7		0124739
R26	330R		0136104
R27	1k2		0136118
R28			
R29			
R30	100k		0136164
R31	100R		01
R32	680R		0136114
R33	22k (1W)		
R34	1k5 (1W)		0135750
R35	4k7		0124739
RV1	4k7		
RV2	1M0		

C1	10pF	10C	0126774
C2	1nF		
C3	10pF		0126774
C4	100pF		
C5	12pF		
C6	12pF		
C7	150pF		
C8	1nF		
C9	15uF		0130498
C10	220nF		1953299
C11	220nF		1953299
C12	220nF		1953299
C13	100nF		
C14	100pF		9467456
C15	10nF		9521641
C16	10nF		9521641
C17	10nF		9521641
C18	47uF		0131425
C19	470nF		
C20	15uF		0130498
C21	470nF		
C22	15uF		0130498
C23	56uF		1021722
C24	56uF		1021722
VC1	8-81pF		0161008
L1			9132586
L2			9132581
L3			9132584

VT1	2N916
VT2	2N3819
VT3	2N3819
VT4	2N916
VT5	2N916
VT6	2N3705
VT7	2N3705
VT8	BC107

IC1	SN7493N
IC2	SN74122N
IC3	SN7400N

SECTION 4 PART 2 - DIVIDER BOARD

1. This board accepts 3 250KHz inputs, one from each of the two oscillators and one from an external signal source. One of these inputs is selected for use and then divided down to 250Hz by a ten stage binary counter.

2. 6 pulses each 4uS wide are obtained by gating the binary counter outputs, their timings are (with respect to zero, and assuming a P.R.F. of 250pps), -1000uS, -750uS, -250uS, -125uS, -8uS, and zero. 5 of these pulses are fed to the Output boards and the Delay boards, the -1000uS pulse is used on the control board. The 6 pulses are checked both for presence and correct sequence. An additional check performed on the -1000uS pulse ensures that the P.R.F. of the outputs is of the correct order.

3. The TTL counter has an 'Align' facility, this enables the standby divider to be run in exact synchronism with the in use divider.

Circuit Description

4. The input gating from the Control Panel is used to set bistable IC30c & d. The bistable outputs enable IC15a and allow the oscillator signal through, or enable IC15b allowing the B oscillator through. If SW1a is in the Ext position both IC15a and IC15b are disabled, IC14a is enabled allowing an external signal to be applied to the divider.

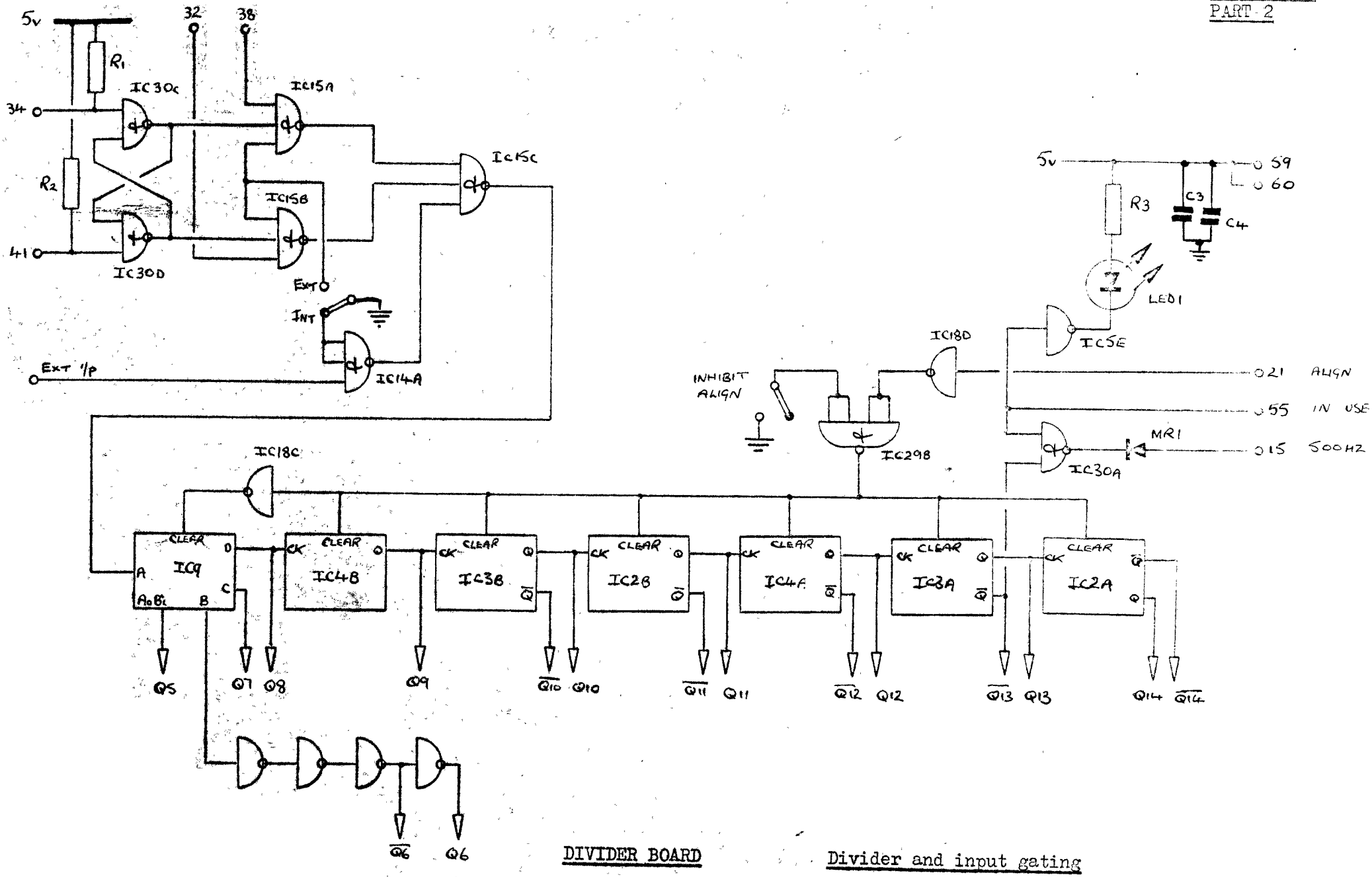
5. The selected input is fed via IC15c to the ripple counter chain which consists of 4 bit binary counter IC9 followed by 6 JK flip flops IC2, 3, and 4. These flip flops are used in the ÷2 mode, with their J inputs connected to their $\bar{Q}$ outputs and K inputs connected to Q outputs to avoid having to connect them to VCC.

6. The align input is applied to all flip flops and inverted by IC18C before being applied to IC9. A logical 0 on this line will clear the flip flops and the logical 1 from IC18c will clear IC9. SW16 inhibits the align when an external signal is used to drive the divider.

Output Gating Circuit

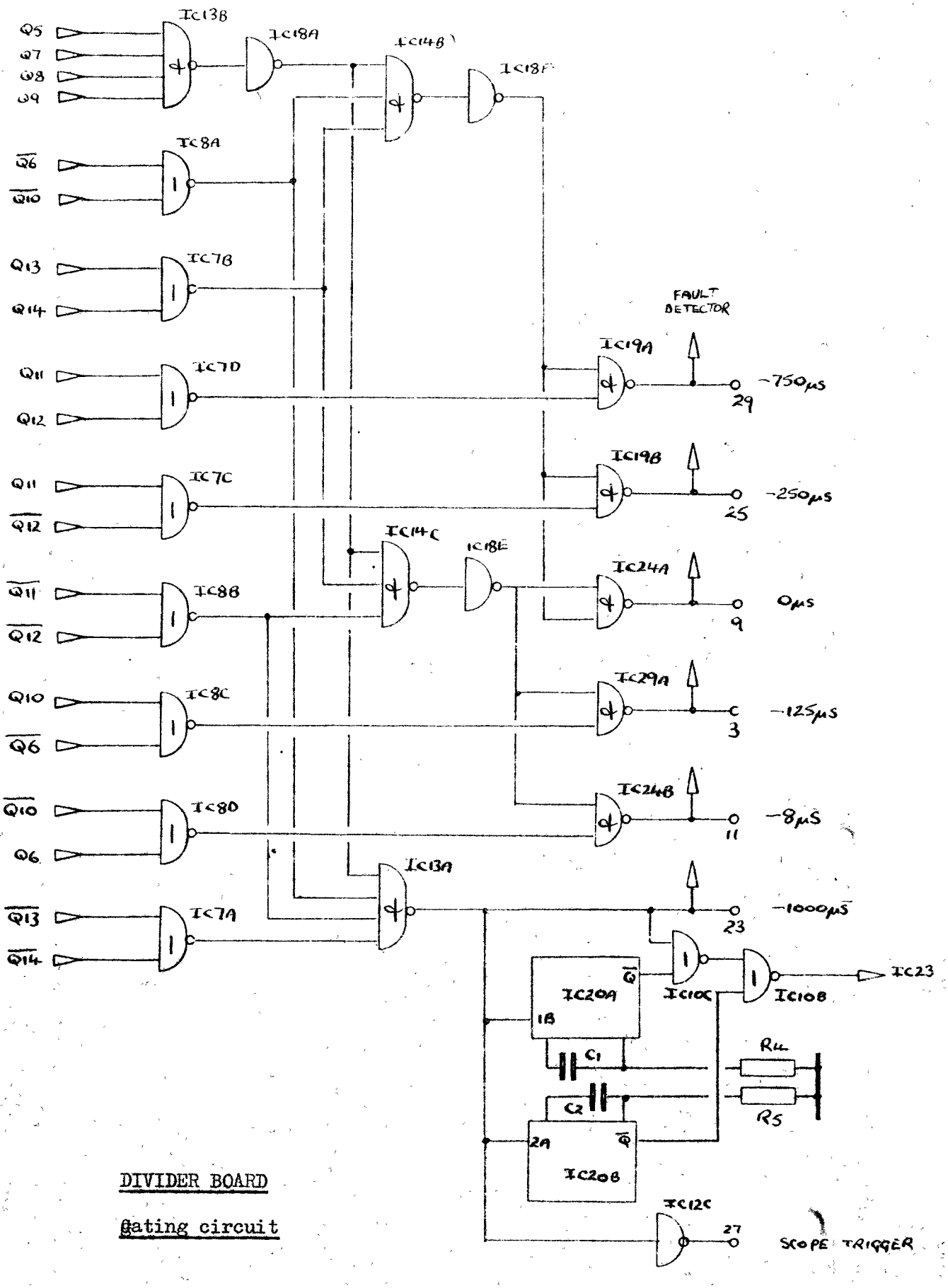
7. The output gating circuit provides the 4uS wide pulses at the required timings. The Q and $\bar{Q}$ outputs of the counter are the inputs to the gating circuit, To minimise the effects of propagation delay through the counter chain Q6 is delayed by passing it through successive stages of inversion in IC5a, b and c. The various triggers are produced in accordance with the truth table below:-

	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14
-1000uS	1	1	1	1	1	1	1	1	1	1
-750uS	1	1	1	1	1	1	0	0	0	0
-250uS	1	1	1	1	1	1	0	1	0	0
-125uS	1	1	1	1	1	0	1	1	0	0
-8uS	1	0	1	1	1	1	1	1	0	0
0uS	1	1	1	1	1	1	1	1	0	0



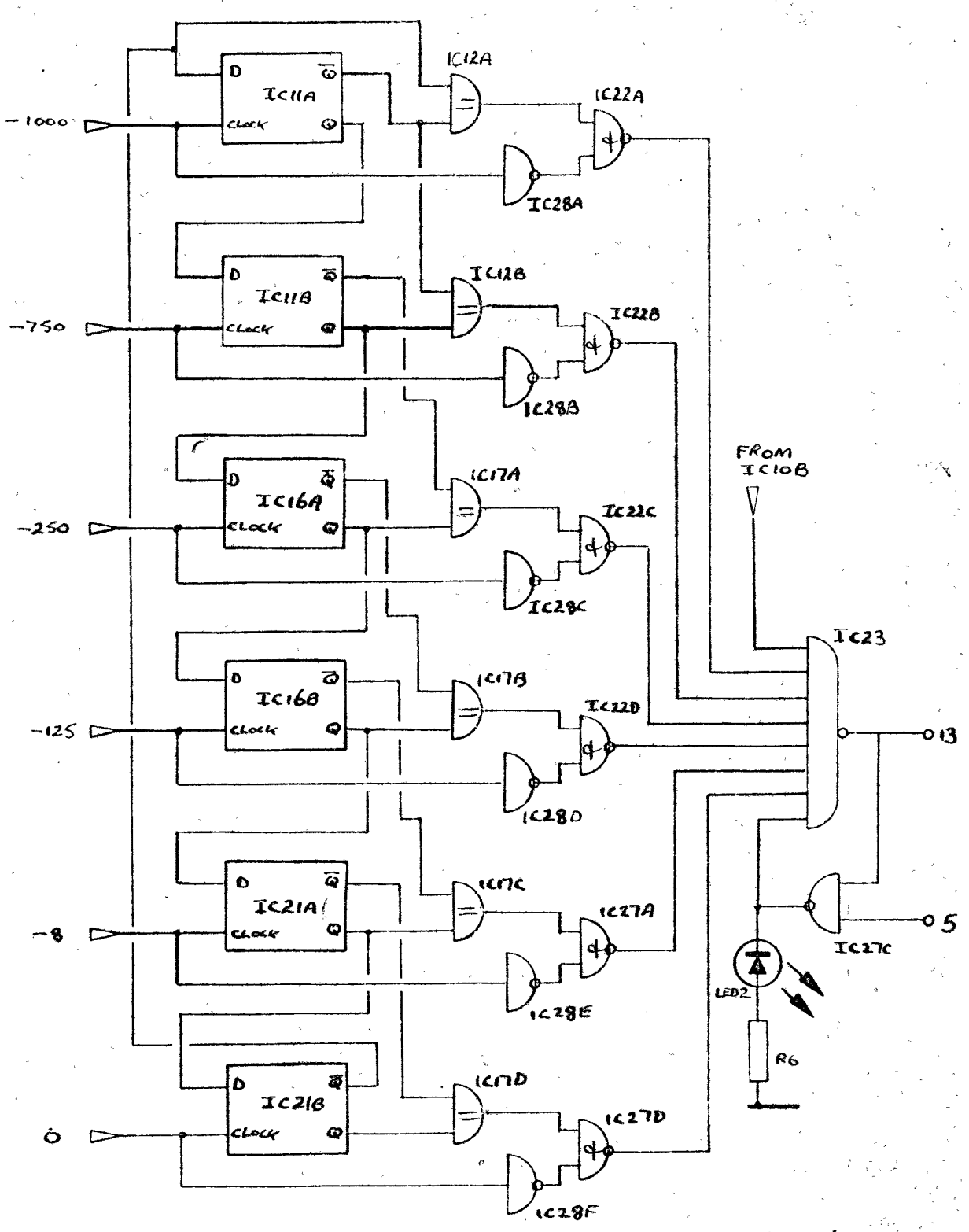
DIVIDER BOARD

Divider and input gating

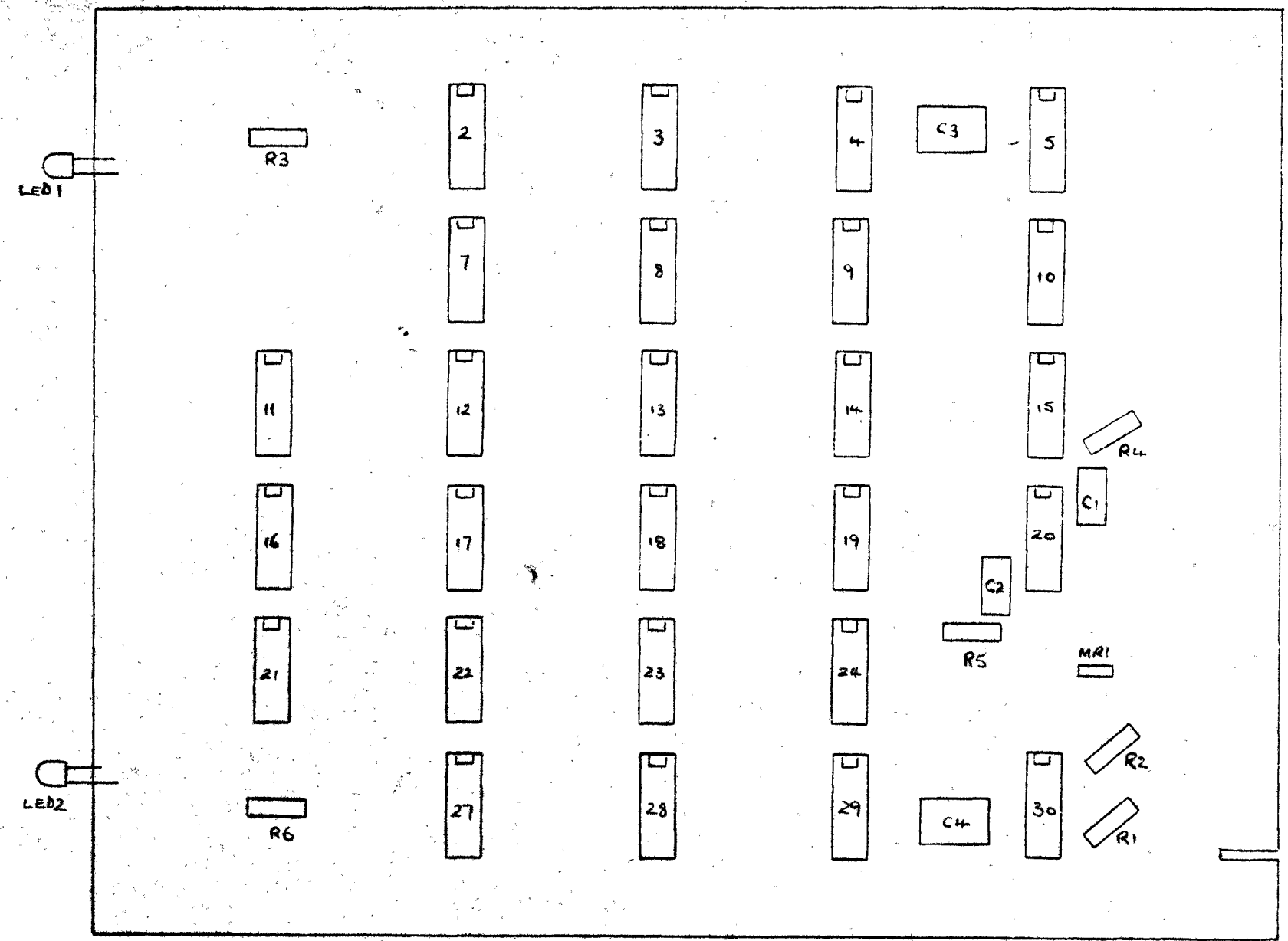


DIVIDER BOARD

Gating circuit



DIVIDER BOARD Fault detector



DIVIDER BOARD Layout

SECTION 4 - PART 3 - OUTPUT BOARD

General Description

1. This board accepts three inputs from each divider board at TTL logic levels. Each board produces six 35 volt, 4uS positive going triggers. The board is powered from the 5 volt and the 4 0 volt power supplies.

Circuit Description

2. Input gating The divider A or B selection is carried out on the output board by IC1 and IC2. IC1c and IC2b form a cross coupled NAND bistable whose state depends on the control signal coming from the selector switch SW on the Control Panel. The purpose of this bistable is to ensure that only one divider is selected at one time. When the bistable is in the 'A' position due to a logical 0 at pin 52, a logical 1 is applied to the gating inputs of IC1a, b and d, allowing the input from divider A to pass through the gates. A logical 0 is applied to the gating inputs of IC2a, c and d thereby inhibiting the inputs from divider B. When a logical 0 is applied to pin 53 the gating is reversed, B inputs being allowed through and A inputs inhibited.

3. The three outputs of the gating circuit are fed out from the board on pins 51, 56 and 58 and externally wired to the six inputs on pins 41 to 46. Each trigger is buffered and inverted by one element of IC3 and fed to the discrete component trigger driver.

Trigger Driver

Note:- Description is given for trigger driver A, see table for other driver component references.

4. The trigger is fed from IC3a through C1 and R7, C2 to the base of VT1. Diode MR1 prevents the output of IC3c being pulled above 5 volts by C1 charging during switch on.

5. VT1 is normally non-conducting and is driven into conduction by the trigger input. When VT1 conducts, the junction of R8 and R9 is pulled up to the 40 volt rail. Base current to turn on VT2 is supplied through R9. C3 and VT2 form a capacitive discharge circuit into the load. C3 is kept charged by current through R12.

6. Isolating diode MR2 enables the outputs from two boards to be paralleled to provide back-up should one driver fail.

7. A portion of the output is tapped from potential divider R10, R11 and fed to the fault detector IC6b.

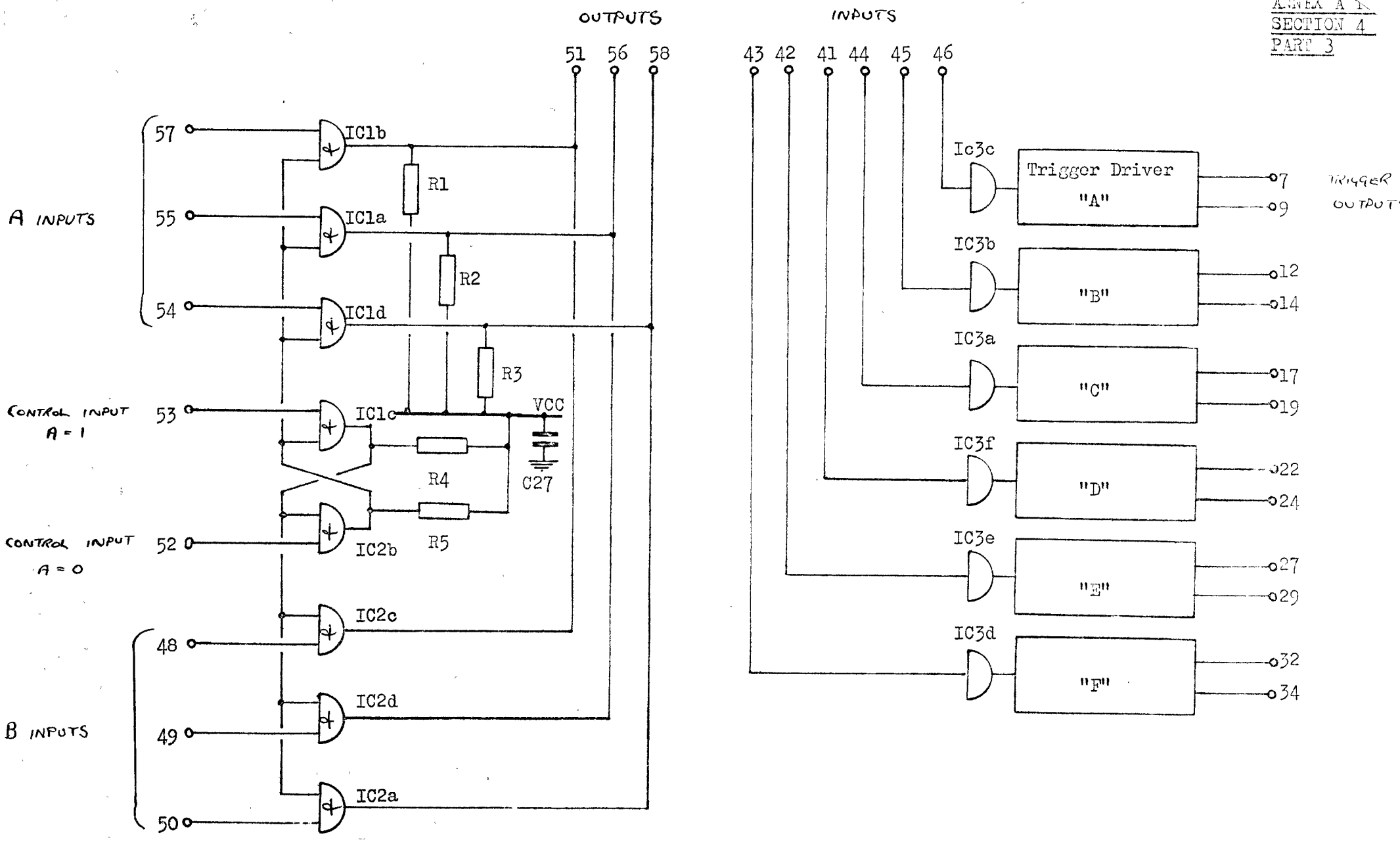
Fault Detector

8. The output trigger sample is fed to the retriggerable monostable multivibrator IC6b which timing period is set by R13 and C4 to be 5mSecs. As the pulse spacing is approximately 4mS the monostable will be retriggered before the completion of its timing cycle. The Q output of IC6b will therefore remain at a logical 1 and the $\overline{Q}$ at logical 0, lighting the trigger presence indicator LED1.

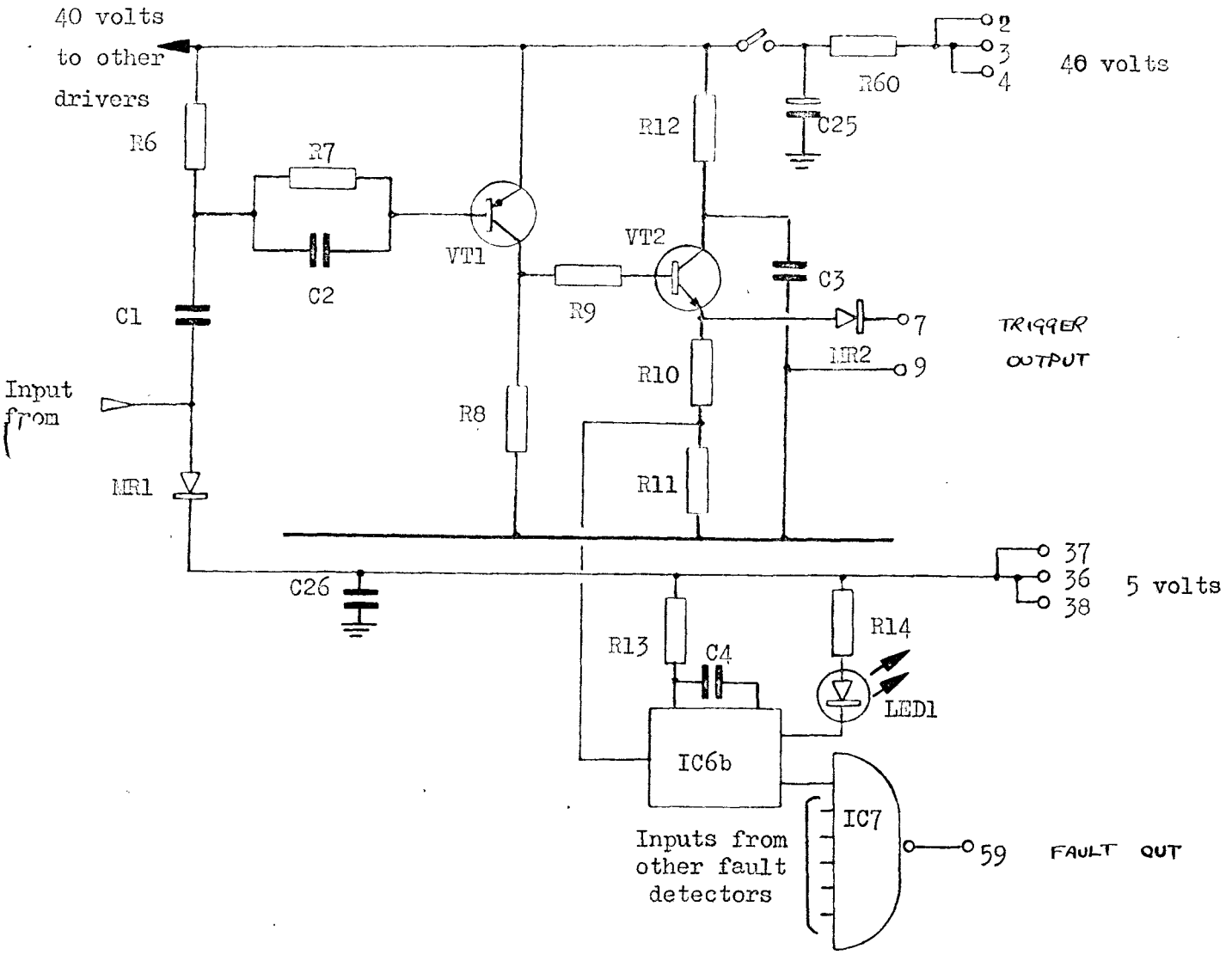
Fault detector (continued)

9. Should any trigger fail, the appropriate LED will extinguish and the Q of the fault detector will go to logical 0. The presence of a logical 0 at any input of IC7 will cause its output to go to logical 1 signalling a fault to the control board circuitry.

10. Since two separate drivers are simultaneously providing each trigger, no change-over need take place if one trigger driver output fails.

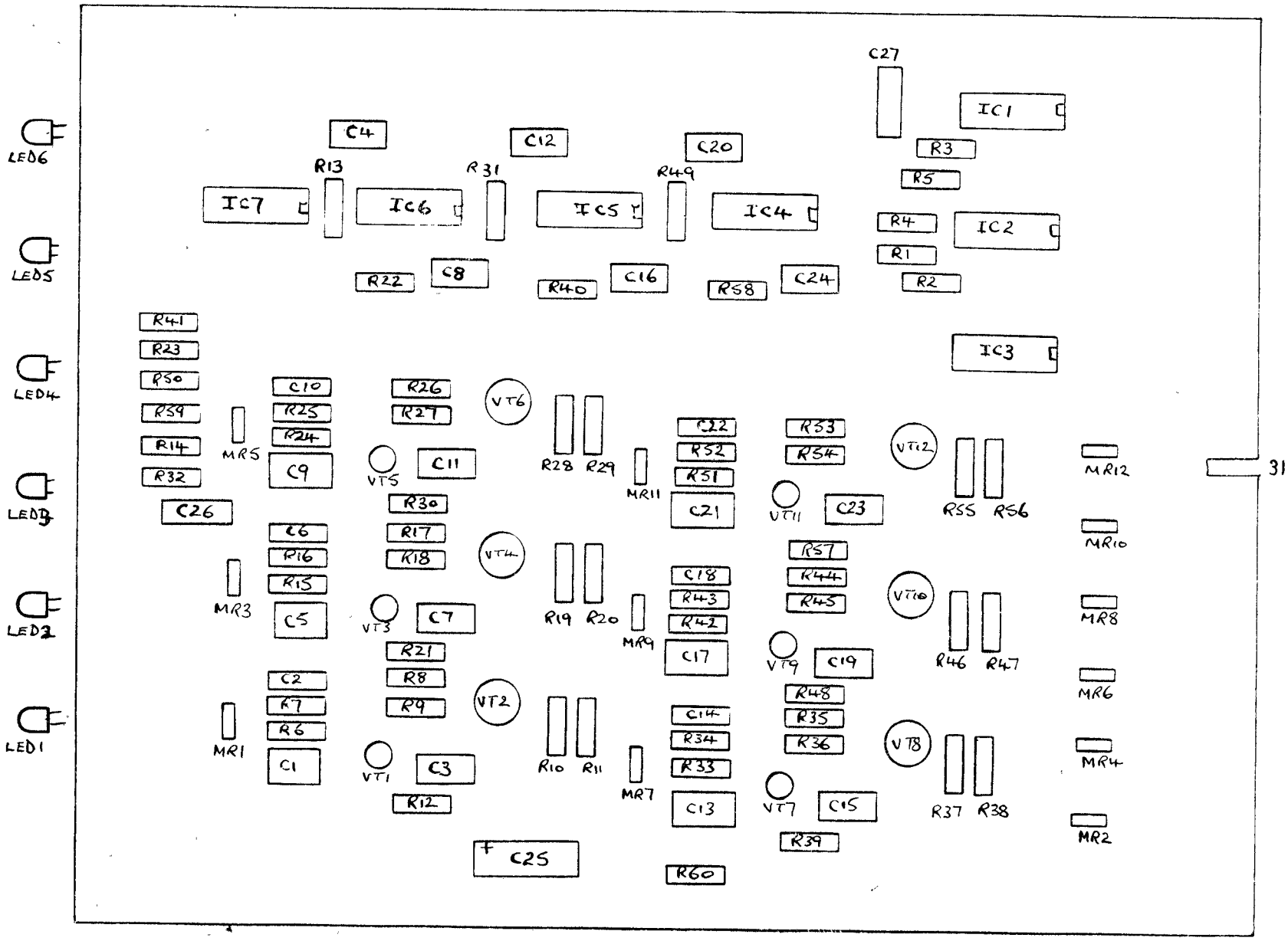


OUTPUT BOARD Input logic diagram



A	B	C	D	E	F	
R6	R15	R24	R33	R42	R51	1k5
R7	R16	R25	R34	R43	R52	1k5
R8	R17	R26	R35	R44	R53	1k5
R9	R18	R27	R36	R45	R54	680R
R10	R19	R28	R37	R46	R55	220R
R11	R20	R29	R38	R47	R56	18R
R12	R21	R30	R39	R48	R57	5k6
R13	R22	R31	R40	R49	R58	33k
R14	R23	R32	R41	R50	R59	270R
C1	C5	C9	C13	C17	C21	4.7nF
C2	C6	C10	C14	C18	C22	100pF
C3	C7	C11	C15	C19	C23	0.47uF
C4	C8	C12	C16	C20	C24	0.47uF
VT1	VT3	VT5	VT7	VT9	VT11	CV 7676
VT2	VT4	VT6	VT8	VT10	VT12	CV 7725
MR1	MR3	MR5	MR7	MR9	MR11	CV7128
MR2	MR4	MR6	MR8	MR10	MR12	CV 7368
LED1	LED2	LED3	LED4	LED5	LED6	TIL 209
I06b	IC6a	IC5b	IC5a	IC4b	IC4a	SN74123N
pin 7	pin 12	pin 17	pin 22	pin 27	pin 32	Output pin
pin 9	pin 14	pin 19	pin 24	pin 29	pin 34	Output ground

OUTPUT BOARD Trigger Driver and Fault circuit



31

OUTPUT BOARD - LAYOUT DIAGRAM

OUTPUT BOARD - LIST OF COMPONENTS

R1	1k5	10W 0136120
R2	1k5	
R3	1k5	
R4	1k5	
R5	1k5	
R6	1k5	
R7	1k5	
R9	680R	10W 136112
R10	220R	10W 136100
R11	18R	
R12	5k6	10W 136134
R13	33k	10W 136152
R14	270R	

C1	4700p	10C 9548817
C2	100p	10C 9467456
C3	0.47uF	polycarbonate 100v.
C4	0.47uF	
C25	10uF	electrolytic 100v.
C26	0.22uF	10C 1953299
C27	0.22uF	

VT1	CV 7676	10CV 0374448
VT2	CV 7725	10CV 0374572
MR1	CV 7128	10CV 0373140
MR2	CV 7128	10CV 0373140

IC1	SN7403	
IC2	SN7403	
IC3	SN7404	10CV 1181748
IC4	SN74123	
IC5	Sn74123	
IC6	SN74123	
IC7	SN7430	10CV

LED1/6	TIL209

SECTION 4 - PART 4 - DELAY BOARD

1. The delay boards are operated in tandem in the same way as the buffer boards. If both delays on paired boards are not set exactly the same it is possible to produce two output triggers on the same line. To prevent this double pulsing an align circuit is used to start the lagging trigger at the same time as the leading edge of the early trigger.

Input Gating

2. The input gating is identical to that used in the buffer board and is not described in detail here.

Delay Circuit (Considering trigger one circuit)

3. The positive edge of the input to IC3A B starts its timing cycle which period is set by C1, C2, R6 and RV1. When the timing cycle is completed the Q output of IC3A returns to logical 0. This falling edge triggers IC3B which starts its timing cycle which is set to 4uS by R7, C3.

4. The 4uS pulse at the $\overline{Q}$ of IC3B is fed to the trigger drive amplifier and fault detector circuit identical to that used on the buffer boards.

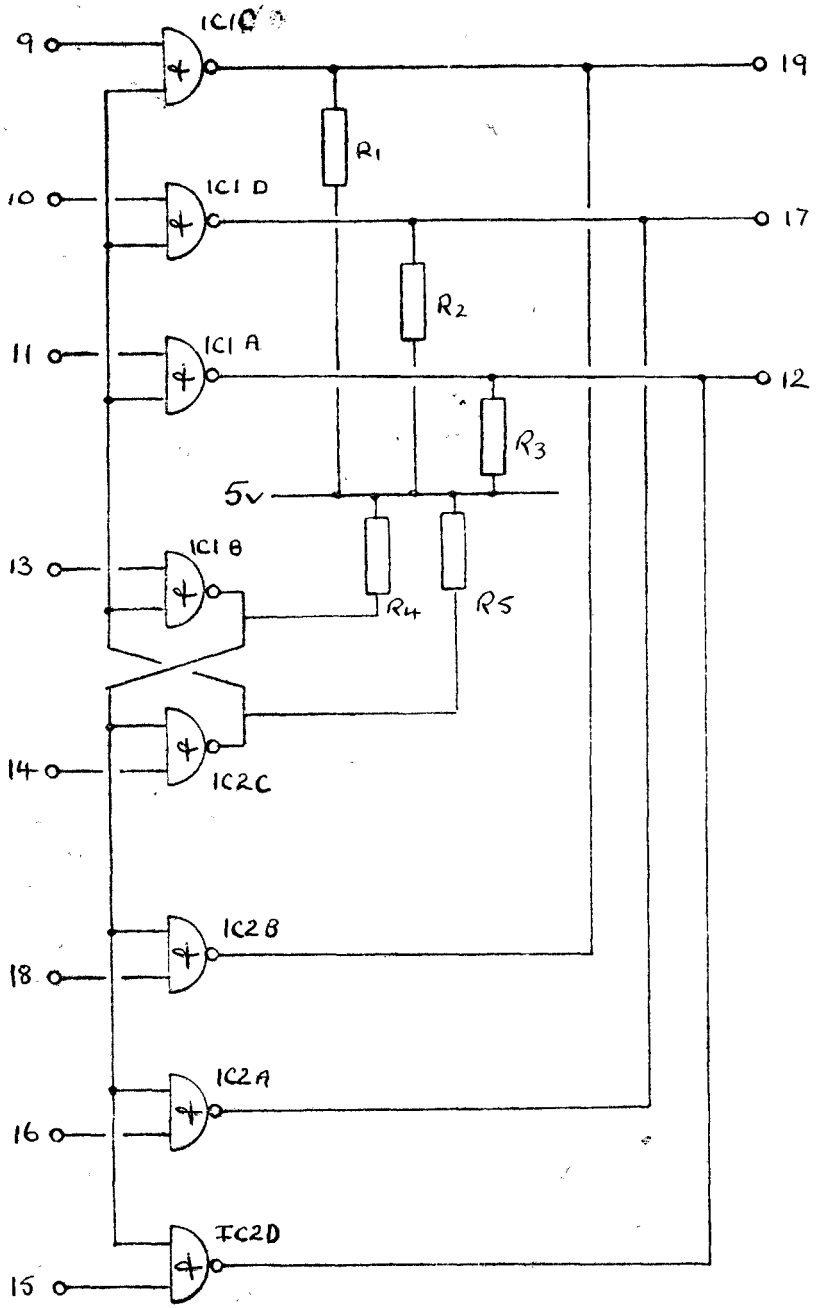
Align Circuit

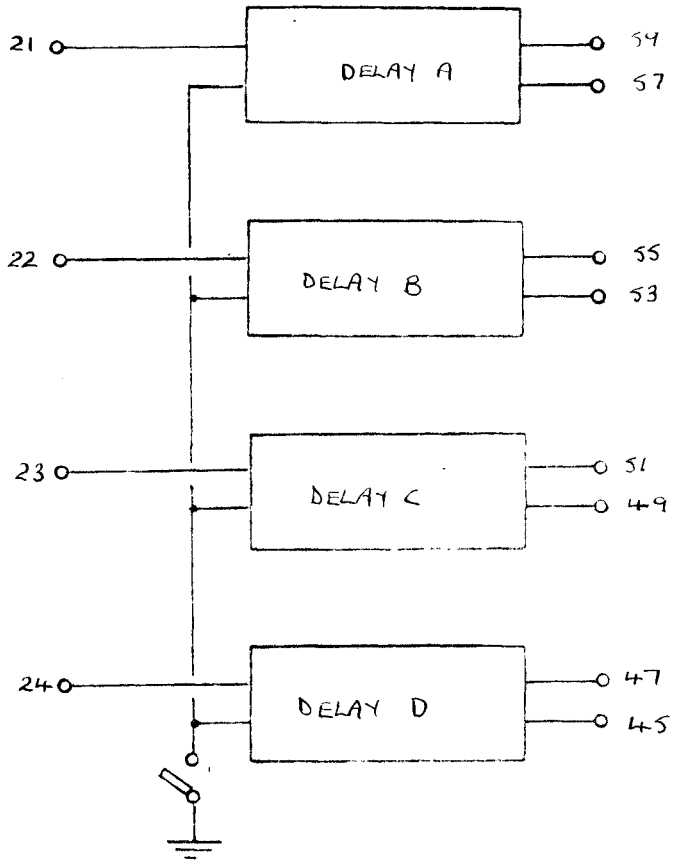
5. The 4uS pulse at IC3B Q is fed to IC9C. This pulse is allowed to pass through IC9C and leave the board only if the trigger is serviceable. If the trigger is not present then IC11B Q will be at logical 0 and the align pulse will be inhibited at IC9C.

6. When the align pulse arrives at board B, it is inverted by IC8F and is passed to IC7C. Providing the align is not inhibited the align pulse is fed to the clear input of IC3A. Consider the circuit action when the delay on board B is set longer than that of board A. The align pulse which starts at the leading edge of the trigger from board A clears IC3A on board B. IC3A Q goes low and initiates the trigger pulse from board B. The align facility is inhibited on one board of the pair when the second is turned off on time control panel.

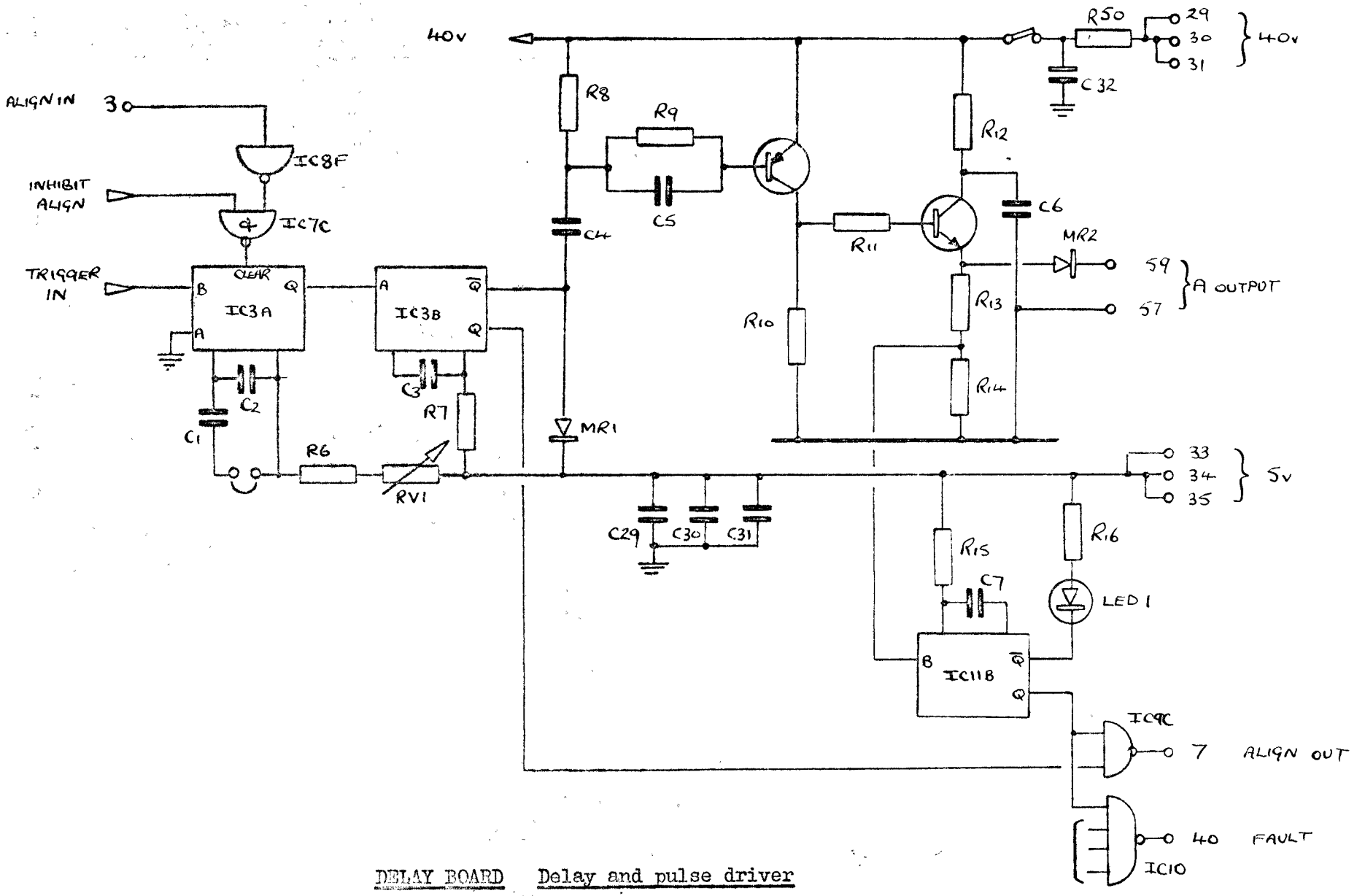
6. The two fixed ranges of each delay are set by a prewired link adjacent to the timing capacitors C1 and C2.

7. The fault outputs from each delay are commoned in IC10 and fed on the control board.

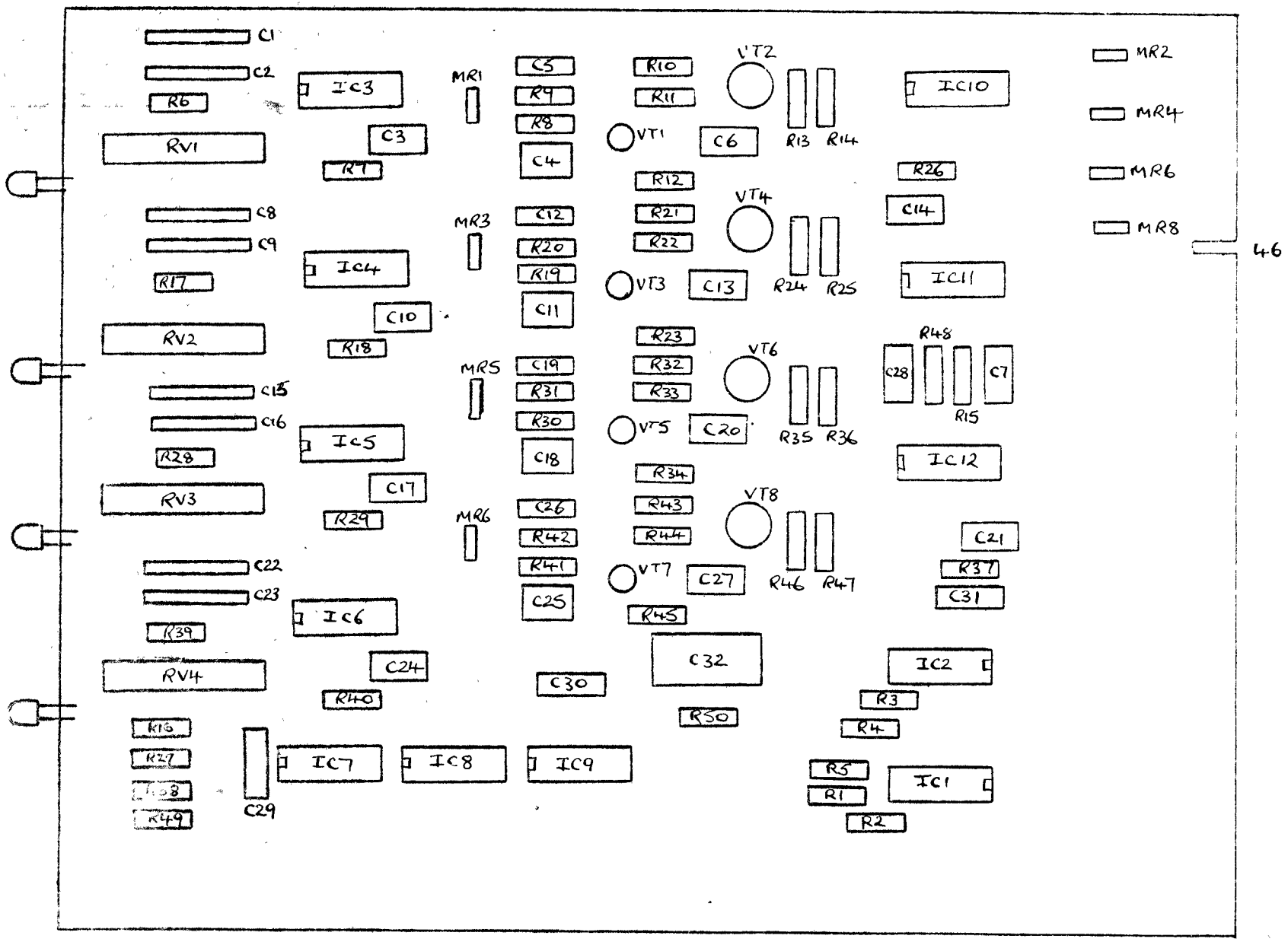




DELAY BOARD INPUT LOGIC DIAGRAM



DELAY BOARD Delay and pulse driver



DELAY BOARD Layout

Component index, Trigger Driver and delay

Circuit	A	B	C	D
	R6	R17	R28	R39
	R7	R18	R29	R40
	R8	R19	R30	R41
	R9	R20	R31	R42
	R10	R21	R32	R43
	R11	R22	R33	R44
	R12	R23	R34	R45
	R13	R24	R35	R46
	R14	R25	R36	R47
	R15	R26	R37	R48
	R16	R27	R38	R49
	RV1	RV2	RV3	RV4
	C1	C8	C15	C22
	C2	C9	C16	C23
	C3	C10	C17	C24
	C4	C11	C18	C25
	C5	C12	C19	C26
	C6	C13	C20	C27
	C7	C14	C21	C28
	MR1	MR3	MR5	MR7
	MR2	MR4	MR6	MR8
	IC7c	IC7b	IC7a	IC7d
	IC3	IC4	IC5	IC6
	IC8f	IC8a	IC8b	IC8e
	IC9c	IC9b	IC9a	IC9d
	IC11b	IC11a	IC12b	IC12a
	LED1	LED2	LED3	LED4

ANNEX E TO
SECTION 4
PART 4

DELAY BOARD - LIST OF COMPONENTS

R1	1k5	10W 0136120
R2	1k5	
R3	1k5	
R4	1k5	
R5	1k5	
R6	4k7	10W 0124739
R7	18k	10W 0136146
R8	1k5	
R9	1k5	
R10	1k5	
R11	680R	10W 0136112
R12	5k6	10W 0136134
R13	220R	10W 0136100
R14	18R	
R15	33k	10W 0136152
R16	270R	
R50	220R	10W 0136100
RV1	50k	10W 9567027
VT1	CV7676	10CV 0374448
VT2	CV7725	10CV 0374572
MR1	CV7128	10CV 0373140
MR2	CV7128	10CV 0373140
LED1/6	TIL209	

C1	0.01uF	
C2		
C3	680pF	
C4	4700pF	10C 9548817
C5	100pF	10C 9567456
C6	0.47uF	100v polycarbonate
C7	0.47uF	
C29	0.22uF	10C 1953299
C30	0.22uF	
C31	0.22uF	
C32	10uF	100v electrolytic
IC1	SN7403	
IC2	SN7403	
IC3	SN74123	
IC4	SN74123	
IC5	SN74123	
IC6	SN74123	
IC7	SN7400	10AD 5204489
IC8	SN7404	10CV 1181748
IC9	SN7400	10AD 5204489
IC10	SN7420	
IC11	SN74123	
IC12	SN74123	

SECTION 4 - PART 5 - CONTROL BOARD

General Description

1. The Control board contains the logic required to decide which part of the trigger system is serviceable, and in the case of the dividers and oscillators ensures that the in use boards are serviceable. Should an output board not be serviceable, the control board will indicate this, but do nothing about it.

2. This board also contains the logic required to align the dividers, and the pulse generator required to reset its own fault latches and those of the dividers and oscillators.

3. The conditions set by the control board may be manually over-ridden by the switches on the control panel.

Circuit Description

4. Oscillator Control The fault lines from Oscillators A and B are fed into the Board on pins 55 and 57 respectively to IC15a. These lines are at logical 0 for no fault and logical 1 for fault. When an oscillator fault occurs IC15a output goes to logical 0 and sets the fault latch formed by IC19a and b which in turn lights the oscillator fault LED and via IC17 the overall fault LED (and rings the bell).

5. The fault input lines also feed IC5e and IC5f which invert the logic to give a logical 0 as a fault. The output of IC5e is fed to IC5c and the K input of IC3a. The K input of IC3a going to logical 0 ensures that when IC3a is clocked, its Q will go to logical 0 and its $\overline{Q}$ to logical 1 (this selects B oscillator as in use). The output of IC5c going to logical 1 causes the input to IC4c to go to a logical 1 for a time dependant upon C2 and R2. If IC4c's other input is at logical 1 at this time (i.e. oscillator A in use) its output will go to logical 0 for about 1uS. This pulse is fed via IC4b to the clock input of IC3a which causes IC3a Q to go to logical 1 which selects B Oscillator as in use, as mentioned above. Should the B oscillator already have been in use when the A went faulty then IC4c will be inhibited (IC3a $\overline{Q}$ at logical 0) and the only effect will be to operate the fault latch. In the case where one oscillator is faulty and the other goes faulty, both the J and K inputs to IC3a will be at logical 0 when it is clocked and so no change-over will take place. The 2 outputs of IC3a are fed via open collector inverters and the control panel switches to control the input gating on the divider boards. Open collector inverters are used in this position to allow the control lines to be grounded by a manual control switch on the control panel. The circuit action for the B oscillator going faulty is similar to that described above for the A side.

Divider control

6. The control circuit for the dividers is identical to that for the oscillators and the above description applies. The only exception is that the output has more drive capacity (three inverters in parallel) to allow it to feed a large number of output and delay boards. The pull up resistors are mounted on the control panel.

Alignment Control

7. If the standby divider is not in step with the In use divider, the -1000uS pulse from the in use divider is used to bring into alignment the standby divider. IC15b and c, IC13c and IC14a and d form the gating circuit which extracts the -1000uS pulse from the in use divider and feeds it as an align pulse to the standby divider should the two dividers not be in step. Should 2 consecutive align pulses occur, bistable IC28a and b is set by the second of these align pulses. The output of IC28b presents a fault signal to the overall fault detector IC17.

Fault Reset

8. The operation of SW3 is fed as a clean signal to pulse generator circuit C5, R5 via the de-bouncer IC20a and b. The exponential signal is transformed into a square wave by IC18a and fed as a 10uS reset signal to the fault latches throughout the system.

Output Fault Circuit

9. Should a fault occur in any one of the output circuits, a logical 1 will be present at one of the inputs of IC25 or IC30. The logical 1 signal at the combined output of IC25 and IC30 is inverted twice by IC29 c and e and leaves the board to light the output fault LED. When a fault occurs the output fault latch IC28c and d will be set by the pulse from the pulse generator c6 R6 and IC29a. In order to avoid the masking of important faults by minor (output) faults, provision is made to allow the output fault latch to be reset even though the output fault still persists, however in this situation the output fault LED will remain lit when the overall fault LED is extinguished.

Overall Fault

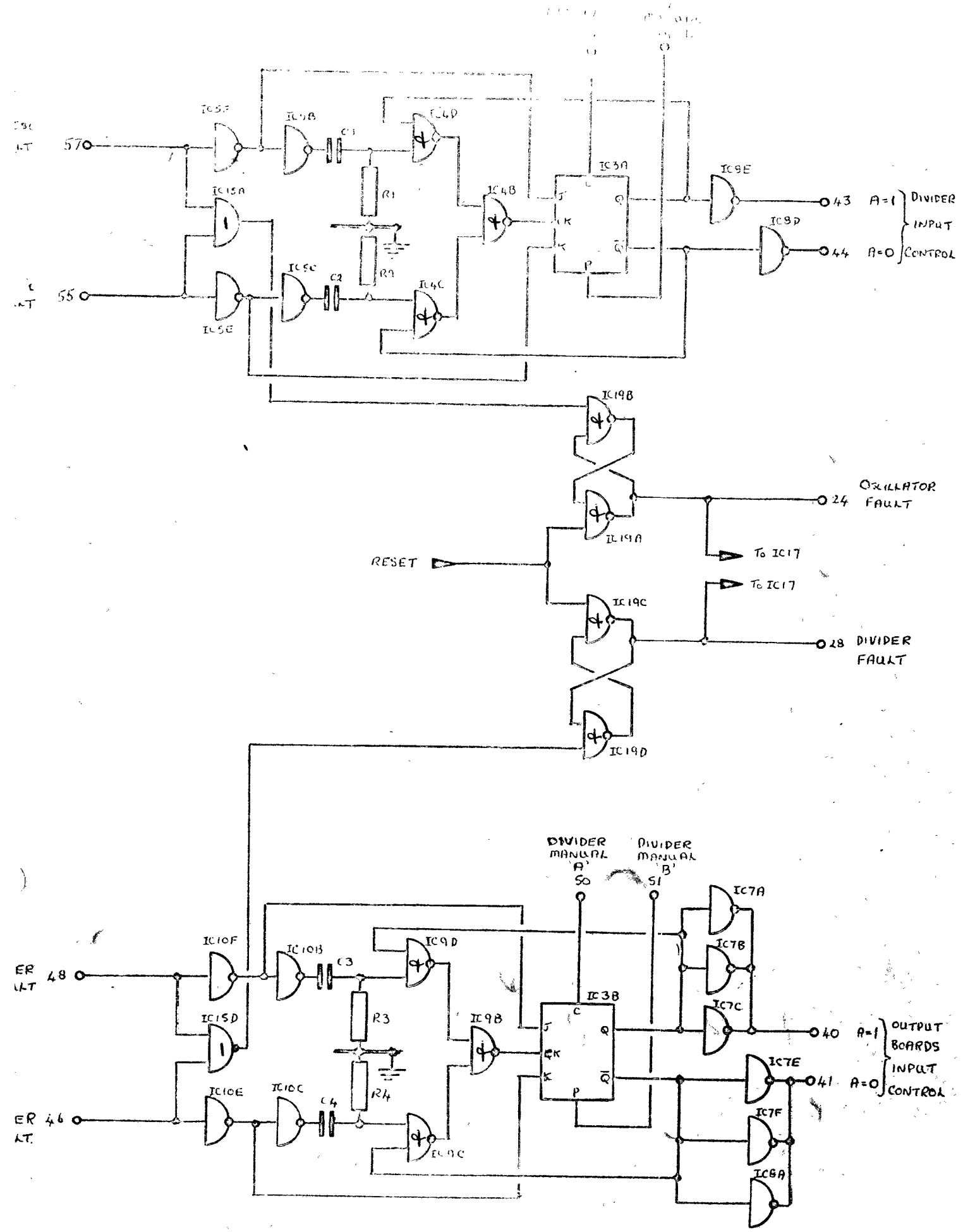
10. The outputs from the individual fault latches are fed to IC17 where they are commoned to provide an overall fault signal. This is inverted by IC13b and fed from the board to light the overall fault LED.

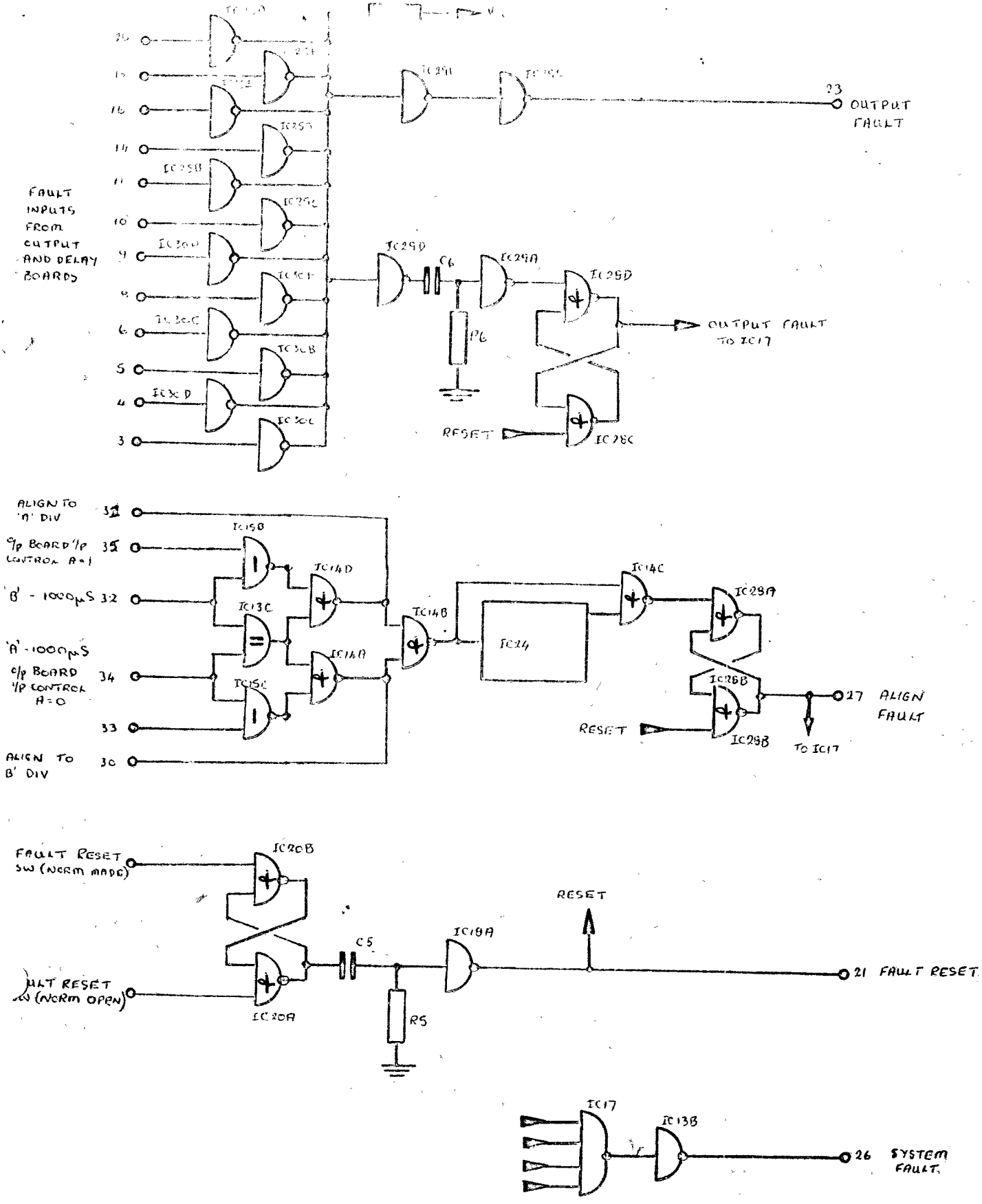
CONTROL BOARD FAULT LOGIC ACTION

Osc. or Div A	Osc. or Div B	
'S'	'S'	Select either for use.
Fault	'S'	Select B for use and operate fault latch
'S'	Fault	Select A for use and operate fault latch
Fault	Fault	Operate fault latch

ALIGN

Divider A	Divider B	
In use	aligned	Do nothing
In use	Mis-aligned	Apply a pulse timed at -1000uS to the align input of Divider B
Aligned	In use	Do nothing
Mis-aligned	In use	Apply a pulse time at -1000uS to the align input of Divider A
More than one successive pulse applied to either align input.		Operate alignment fault latch and light the fault LED
Output fault		Operate overall fault latch with pulse and light output fault LED.


IC5F
IC15A
IC5E
IC5C
IC4C
IC4B
IC4D
IC1B
C1
C2
R1
R2
IC3A
IC9E
IC9D
57
55
43
44
A=1 DIVIDER INPUT
A=0 CONTROL
IC19B
IC19A
IC19C
IC19D
RESET
24 OSCILLATOR FAULT
To IC17
To IC17
28 DIVIDER FAULT
DIVIDER MANUAL 'A' S0
DIVIDER MANUAL 'B' S1
IC10F
IC15D
IC10E
IC10B
IC10C
IC9B
IC9C
IC9D
C3
C4
R3
R4
IC3B
IC7A
IC7B
IC7C
IC7E
IC7F
IC8A
48
46
40
41
A=1 OUTPUT BOARDS INPUT
A=0 CONTROL


FAULT INPUTS FROM OUTPUT AND DELAY BOARDS
IC30D
IC30A
IC30C
IC30B
IC30D
IC30E
IC29D
C6
R6
IC29A
IC29D
OUTPUT FAULT TO IC17
RESET
IC28C
23 OUTPUT FAULT
ALIGN TO 'A' DIV
31
I/P BOARD I/P CONTROL A=1
35
'B' - 1000μS
32
'A' - 1000μS
O/P BOARD I/P CONTROL A=0
34
33
ALIGN TO 'B' DIV
30
IC15B
IC14D
IC13C
IC14A
IC15C
IC14B
IC24
IC14C
IC28A
IC28B
IC28B
27 ALIGN FAULT
TO IC17
RESET
FAULT RESET SW (NORM MADE)
FAULT RESET SW (NORM OPEN)
IC20B
IC20A
C5
R5
IC18A
RESET
21 FAULT RESET
IC17
IC13B
26 SYSTEM FAULT

SECTION 4 - PART 6 - RACK WIRING INTERCONNECTIONS

Osc A	Osc B	Cont Bd	Cont Pan.	Div A	Div B	O/P A	O/P B	Del A	Del B	Signal Description
		3z							40a	Delay B fault
		4z						40a		Delay A fault
		5z					59a			Output B fault
		6z				59a				Output A fault
		8z								)
		9z								) Spare fault input
		10z								)
		11z								) lines to Control Board
		14z								)
		16z								) Grounded when not used
		18z								)
		20z								)
56z	56z	21a		5z	5z					Fault latch reset pulse
		22z	a							" " " Switch (Norm made)
		23a	z							O/P fault Led. drive
		24a	z							Oscillator fault LED drive
		26a	z							Overall fault LED drive
		27a	z							Alignment fault LED drive
		28a	z							Divider fault LED drive
		29z	a							Fault reset switch(Norm. broken)
		30a			21z					Divider B align pulse
		31a		21z						Divider A align pulse
		32z			23a					Divider B -1000uS pulse
		33z	a		55z	52z	52z	13z	13z	Buffer i/p control (Sw'd) A=0
		34z		23a						Divider A -1000uS pulse
		35z	a	55z		55z	53z	14z	14z	Buffer i/p control (Sw'd) A=1
		40a	z							Buffer i/p control (Unsw) A=1
		41a	z							Buffer i/p control (Unsw) A=0
		43a	z							Divider i/p control (Unsw) A=1
		44a	z							Divider i/p control (Unsw) A=0
		46z		13a						Divider A fault
		48z			13a					Divider B fault
		50z	a							Divider Manual A
		51z	a							Divider Manual B
58a		55z								Oscillator A fault
		56z	a							Oscillator Manual A
	58a	57z								Oscillator B fault
		58z	a							Oscillator Manual B
	54z		a	34z	34z					Divider i/p control (Sw'd) A=0
54z			a	41z	41z					Divider i/p control (Sw'd) A=1
	57a			32z	32z					250KHz - Oscillator B
57a				38z	38z					250KHz - Oscillator A
				29a						-750uS - A)
					29a					-750uS - B)
				25a						-250uS - A)
					25a					-250uS - B)
				3a						-125uS - A) Inverted pulse o/p's
					3a					-125uS - B)
				11a						-8uS - A) at TTL logic level.
					11a					-8uS - B) To be wired as req'd.
				9a						0uS - A)
					9a					0uS - B) to O/P & delay boards
			z	27a						Scope trigger (-1000uS)
			z		27a					Scope trigger (-1000uS)
			a					38		Inhibit align A delay
			a						38	Inhibit align B delay

Rack Wiring Interconnections (Continued)

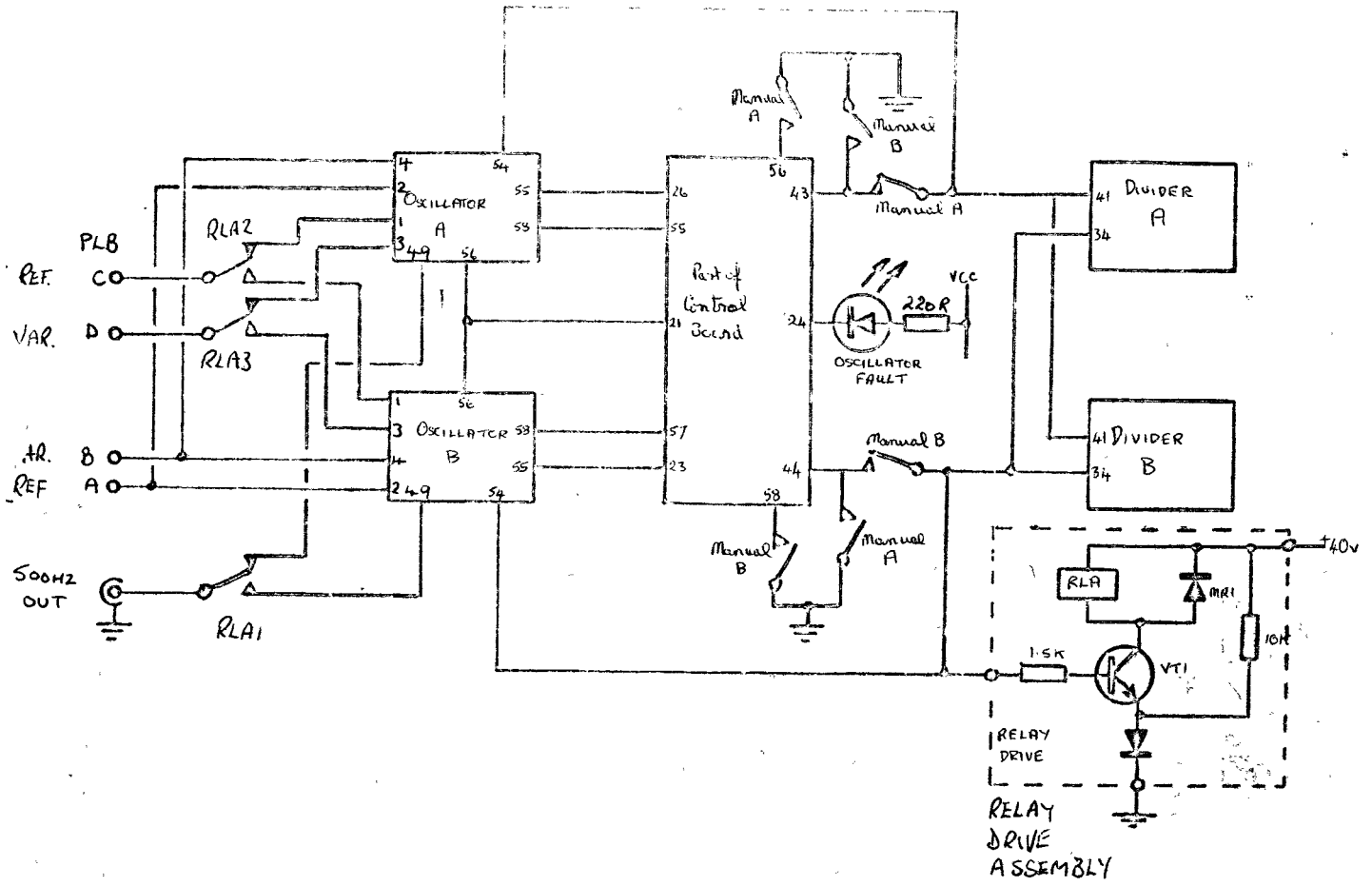
Osc A	Osc B	Cont Bd.	Cont Pan.	Div A	Div B	O/P A	O/P B	Del A	Del B	Signal Description
49a			z							500Hz (to RLA)
	49a		z							500Hz (to RLA)
48z	48z			15a	15a					TTL 500Hz - parallel source
								1z	5a	Delay output align for trigger No
								2z	6a	Delay output align for trigger No
								3z	7a	Delay output align for trigger No
								4z	8a	Delay output align for trigger No
								5a	1z	Delay output align for trigger No
								6a	2z	Delay output align for trigger No
								7a	3z	Delay output align for trigger No
								8a	4z	Delay output align for trigger No
								9z	9z	B input No 3)
								10z	10z	B input No 2) Wire as required to
								11z	11z	B input No 1) the Divider inverted
								15z	15z	A input No 1) pulse outputs.
								16z	16z	A input No 2)
								18z	18z	A input No 3)
								12a		Selected output No 1)
									12a	Selected output No 1) Wire as
								17a		Selected output No 2) required to
									17a	Selected output No 2) input pins
								19a		Selected output No 3) 21-24 on the
									19a	Selected output No 3) same board.
								21z		TTL input for A Delay output No 1
									21z	TTL input for Delay B output No 1
								22z		TTL input for Delay A output No 2
									22z	TTL input for Delay B output No 2
								23z		TTL input for Delay A output No 3
									23z	TTL input for Delay B output No 3
								24z		TTL input for Delay A output No 4
									24z	TTL input for Delay B output No 4
						48z	48z			B input No 1) Wire as required to
						49z	49z			B input No 2) the Divider
						50z	50z			B input No 3) inverted pulse
						54z	54z			A input No 3) outputs.
						55z	55z			A input No 2)
						57z	57z			A input No 1)
						51a				Selected output No 1) Wire as
							51a			Selected output No 1) required to
						56a				Selected output No 2) input pins
							56a			Selected output No 2) 41-46 on
						58a				Selected output No 3) the same
							58a			Selected output No 3) board.
						41z				TTL input for O/P A output No 4
							41z			TTL input for O/P B output No 4
						42z				TTL input for O/P A output No 5
							42z			TTL input for O/P B output No 5
						43z				TTL input for O/P A output No 6
							43z			TTL input for O/P B output No 6
						44z				TTL input for O/P A output No 3
							44z			TTL input for O/P B output No 3
						45z				TTL input for O/P A output No 2
							45z			TTL input for O/P B output No 2
						46z				TTL input for O/P A output No 1
							46z			TTL input for O/P B output No 1

Rack Wiring Interconnections (Continued)

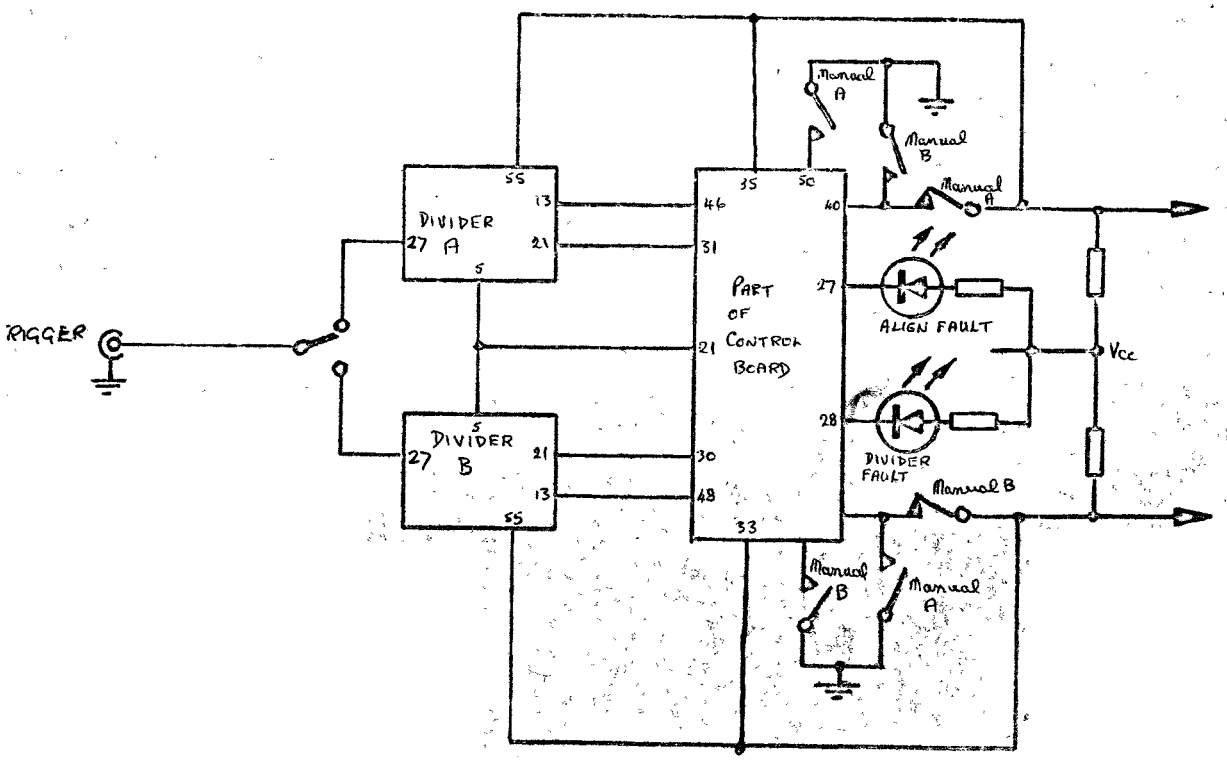
Osc A	Osc B	Cont Bd	Cont Pan	Div A	Div B	O/P A	O/P B	Del A	Del B	Power Rail	
50-2	50-2									+5volts	
42-4	42-4									+40volts	
8	8									+5volts (screened)	
1											500Hz (Sw'd) Ref. phase.
	1										500Hz (Sw'd) Ref. phase.
2	2										500Hz Ref. phase return
3											500Hz Variable phase (Sw'd
	3										500Hz Variable phase (Sw'd
4	4										500Hz Variable phase retur
				59/60 1/2	59/60 1/2					+5volts	
										Ground	
		59/60 1/2								+5volts	
										Ground	
						2-4					+40volts (Switched)
							2-4				+40volts (Switched)
						36-8 1/2	36-8 1/2			+5volts	
										Ground	
								29-31			+40volts (Switched)
									29-31		+40volts (Switched)
								37-8	37-8	+5volts	
								25-7	25-7	Ground	
						7	7				Fixed trigger output No 1
						9	9				Screen for above
						12	12				Fixed trigger output No 2
						14	14				Screen for above
						17	17				Fixed Trigger output No 3
						19	19				Screen for above
						22	22				Fixed trigger output No 4
						24	24				Screen for above
						27	27				Fixed trigger output No 5
						29	29				Screen for above
						32	32				Fixed trigger output No 6
						34	34				Screen for above
								59	59		Delayed trigger output No 1
								57	57		Screen for above
								55	55		Delayed trigger output No 2
								53	53		Screen for above
								51	51		Delayed trigger output No 3
								49	49		Screen for above
								47	47		Delayed trigger output No 4
								45	45		Screen for above

RACK INTERCONNECTION DIAGRAM
(CONTROL)

ANNEX A TO
SECTION 4
PART 6



RELAY DRIVE ASSEMBLY



INPUT CONTROL WIRES TO OUTPUT AND DELAY BOARDS.

RACK INTERCONNECTION DIAGRAM
(PCW CP)