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Colin Hinson

In the village of Blunham, Bedfordshire, UK.

AP 116E-0754-6A

March 1979

10 JUL 1979

UK/FRR 626
HF RECEIVER
(Racal Type RA. 1778/DA78120/B)

GENERAL AND TECHNICAL INFORMATION
ALSO
REPAIR AND RECONDITIONING INSTRUCTIONS

BY COMMAND OF THE DEFENCE COUNCIL

Ministry of Defence

Sponsored for use in the

ROYAL AIR FORCE by D. Sigs (Air)

Prepared by Racal Communications Systems Ltd., Bracknell, Berks.

Publications authority: ATP/MOD (PE)

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MODIFICATION RECORD

The following record confirms that this publication incorporates all technical changes necessitated by the modifications listed below. Information on modification titles, classification categories and Mark applicabilities is given in Topic 2.

Mod No.	Brief Description
A8556	Decrease length of 'read' pulse.
A8529	Introduction of alternative IF/AF board.
A8778	Introduction of 100 kΩ resistors on PM370 board.
A9006	Add ferrite bead to PM336 board.
A9007	To change diodes D13, D14 on PM674 board.
A9662	To prevent amplifier oscillation on PM335 board.
A9722	To reduce spurious signals on PM336 board.
B0077	Reposition the mains fuse.
B0190	Replacement of nickel-cadmium battery.
B0190 Alt 1.	Replacement of nickel-cadmium battery.
B0529	Addition of 1 kΩ resistors to transistors 1TR1, 1TR2 and 1TR3.
► TC0024	Replacement of unobtainable capacitors. ◄

Maintenance manual (Part 1)

RA. 1778/DA78120/B HF Communications Receiver (Chapters 1 to 16)

1976
THE QUEEN'S AWARD FOR EXPORT ACHIEVEMENT TO RACAL COMMUNICATIONS LTD.

RACAL The Electronics Group

Racal Communications Limited Western Road, Bracknell, RG12 1RG England
Tel: Bracknell (0344) 3244 Telex: 848166 Grams: Racal Bracknell.
Prepared by Central Handbooks Department, Racal Group Services Limited.
Printed in England Ref. WOH 9318 Issue 1A.3.79-80

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TECHNICAL SPECIFICATION

The performance as stated in this specification is applicable to the wideband condition. If the RF tuning unit is in use an additional 20dB of protection is given at ± 12½% off-tune.

Frequency Range: 15kHz - 30MHz

Modes of Reception: A1, A2, A2H, A2J, A3, A3A, A3J, A3H with the following options:

(1) Choice of USB or LSB
(2) Provision for reception of A3B or F1
(3) Provision of AFC

Tuning:

(1) 12 Programmable Channels
(2) Continuously tunable synthesizer in 10Hz, 20Hz or 1kHz increments over the full frequency range. Seven digit electronic readout.

Tuning Accuracy: ± 5Hz relative to the frequency of the wanted signal.

Frequency Stability:

(1) The following optional alternative frequency standards may be fitted:

(a) Temperature Controlled Crystal Oscillator (TCXO)

(i) Temperature: Better than $\pm$ 1.5 in 10^6 -10°C to +55°C.

(ii) Long Term: $\pm$ 2 in 10^7 over a 30 day period.

(b) Frequency Standard Type 9400

(i) Temperature: $\pm$ 1 in 10^8/°C.

(ii) Long Term: $\pm$ 1.5in 10^7 over a 30 day period or $\pm$5 in 10^9 per day.

(c) Frequency Standard Type 9420

(i) Temperature: $\pm$ 6 in 10^{10}/°C.

(ii) Long Term: $\pm$ 1.5in 10^8 over a 30 day period or $\pm$5 in 10^{10} per day.

(2) Provision is made for the use of an external frequency standard.

Antenna Input:

(1) Wideband. 50 ohms to 75 ohms nominal. BNC coaxial connector.

(2) RF tuning is available within the receiver. This is provided by five automatically selected bandpass filters covering the frequency range 1MHz to 30MHz. Manual RF peak tuning is provided over each pre-selected band of frequencies. Each tuned range provides a nominal attenuation of 20dB at $12\frac{1}{2}$% off-tune. A low pass filter is used below 1MHz.

(3) Receiver muting is provided to protect the receiver from local emissions on the tuned frequency. The operation of the muting circuits permits 'break in' or 'listen through' operation when keying at a rate of up to 20 bauds.

(4) The receiver will withstand without damage RF input signals of 30V (e.m.f.) continuously. A fuse and spark gap is provided for protection against higher voltages.

(5) Re-radiation with the antenna input terminated in 50 ohms is less than 10μV.

Sensitivity:

(1) CW and SSB (A1, A2H, A3A, A3H, A3J)

In a 3kHz bandwidth the signal-to-noise ratio is better than:

500kHz-30MHz, 15dB with 1 μV (e.m.f.) input.
50kHz-500kHz, 15dB with 3 μV (e.m.f.) input.
15kHz-50kHz, 15dB with 10 μV (e.m.f.) input.

(2) DSB (A2, A3)

In a 3kHz bandwidth the signal-to-noise ratio is better than:

500kHz-30MHz, 15dB with 1.5 μV (e.m.f.) input 70% modulated.

50kHz-500kHz, 15dB with 5 μV (e.m.f.) input 70% modulated.

15kHz-50kHz, 15dB with 15 μV (e.m.f.) input 70% modulated.

IF Selectivity:

(1) SSB (A3A, A3J) and ISB (A3B)

Passband at -6dB: 250Hz to 3000Hz.
Passband at -60dB: 400Hz and +4100 Hz.
or alternatively
Passband at -6dB: 150Hz to 6000Hz.
Passband at -60db: -300Hz and +8000Hz.

(2) CW/MCW/AM/FSK (A1, A2, A3, A2H, A3H, F1)

Standard Receivers. In addition to the mode-selected SSB or ISB filters, up to four optional IF filters may be fitted although certain combinations of facilities will permit only three filters to be fitted. IF filters of the following nominal passbands are available:

0.3kHz, 1kHz, 3kHz, 6kHz, 8kHz, 13kHz.

Alternative filters can be supplied to special order.

Cross Modulation:

With a wanted signal greater than 300 μV e.m.f., in a 3kHz bandwidth, an unwanted signal, 30% modulated, removed not less than 20kHz, will be greater than 300mV e.m.f., to produce an output 20dB below the output produced by the wanted signal.

Reciprocal Mixing:

With a wanted signal of less than 100 μV e.m.f., in a 3kHz bandwidth, an unwanted signal more than 20kHz removed will be greater than 70dB above the wanted signal level to give a noise level 20dB below the output produced by the wanted signal.

Blocking:

With a wanted signal of 1mV e.m.f., an unwanted signal more than 20kHz removed must be greater than 500mV to reduce the output by 3dB.

Intermodulation Products:

(1) Out of Band

With two 30mV e.m.f. signals separated and removed from the wanted signal by not less than 20kHz the third order intermodulation products are not less than -85dB below either of the interfering signals and typically better than -90dB.

(2) In Band

Two in band signals of 30mV e.m.f. will produce third-order intermodulation products of not greater than -40dB.

Spurious Responses:

(1) External

External signals, 20kHz removed from the wanted signal, must be at least 80dB above the level of the wanted signal to produce an equivalent output.

(2) Internal

The specified sensitivity figures in the CW/SSB modes are not reduced by more than 3dB as a result of any internally generated spurious signals.

AGC:

(1) Range

An increase in input of 100dB above 2 μV e.m.f. will produce an output change of less than 6dB.

(2) Switched selection of AGC 'off', 'short' and 'long' time constants is provided.

AFC (A3A, A3B):

(1) AFC is available as an optional internal facility and is provided with a front panel switch for switching AFC in or out of operation.

(2) Capture range: ± 50Hz.

Follow range: ± 500Hz or beyond.

Residual Error: 2Hz max.

Memory: In the event of carrier failure, or worsening of the carrier to noise/modulation level of 10dB, no re-tuning is necessary.

BFO Range: ± 3kHz variable by a slow motion control.

IF Output (AGC On): 1.4MHz, nominally 100mV (e.m.f.) into 50 ohms.

Audio Characteristics:

(1) Output Levels:

(a) Line outputs, 1mW nominal into 600 ohms balanced, adjustable by preset level control on front panel to +6dBm.

(b) Phone outputs unbalanced, 10mW nominal into 600 ohms.

(c) 50mW into an internal loudspeaker which is capable of being switched in or out of operation.

(d) Connection for external speaker 1 watt into 8 ohms.

(e) Two 3 mW, 600Ω outputs.

(2) AF Response:

(a) Line outputs. Within 1dB from 100Hz to 6000Hz relative to the level of a standard 1000Hz tone.

(b) The overall AF response will be dependent upon the IF bandwidth selected.

(3) AF Distortion:

(a) Line outputs. Not greater than 2% at specified output of 1mW nominal.

(b) Loudspeaker outputs. Not greater than 5% at 50mW output to internal loudspeaker, and 1W output to external speaker.

(c) Phone output. Not greater than 5% at specified output of 10mW nominal.

Cross Talk (A3B): With a wanted signal at a level of 1 mV and the AF output adjusted to 1mW, the cross talk from an equal signal in the opposite sideband, at greater than 400Hz from the carrier, is not greater than -50dB relative to 1mW.

Frequency Shift Demodulation (optional):

(1) Frequency shift range, 85Hz to 850Hz.

(2) Maximum keying speed 200 bauds.

(3) Telegraph distortion not greater than 5% up to 100 bauds.

(4) Telegraph output. Polar (double current) DC output approximately 100mA with choice of 6-0-6V or 80-0-80V. Normally positive on 'Mark'. Provision is made by internal adjustment for neutral (single current) operation.

(5) Mark/space reversal is available to the operator and a 'tune' switch position is provided to permit tuning of the receiver without operating the teleprinter.

Metering:	A meter is provided on the front panel to indicate RF level, AF level to line, FSK tune, and suitable performance or supply test levels.
Power Supply:	100V-125V or 200V-250V, ± 10%, 45-65Hz.
Power Consumption:	Approximately 60VA (Basic receiver). Approximately 90VA (Fully equipped).
Environmental Conditions:	The equipment is designed to meet certain of the requirements of the British Defence Specification DEF.133, L2, for ambient temperature range of:

Operating Temperature	- 10°C to +55°C.
Storage Temperature	- 40°C to +70°C.
Relative Humidity	95% at +40°C.

Dimensions:	Rack Mounted	In Bench Cabinet
Height:	178mm (7 in.)	220mm (8.65 in.)
Width:	483mm (19 in.)	495mm (19.5 in.)
Depth:	410mm (16.15 in.)	445mm (17.5 in.)
Weight (approx):	22kg (48.5lb)	28kg (61.5lb)

FRONT PANEL CONTROLS AND FITTINGS

12 way Rotary Channel Selector Switch
Rotary VFO Type Frequency Control
Tuning Rate Switch (Fast, Medium, Slow and Lock)
RF Tuning Control
AGC Time Constants Switch
AFC On/Off Switch (Optional)
AFC Lock Lamp
Mode Switch
Meter Facility Switch
Meter
Channel, Tune, Load
Loudspeaker
Loudspeaker Switch
Headphone Socket
IF Gain Control
AF Gain Control
BFO Slow Motion Control
Line Level Preset Adjusters
Filter Switch
Power On/Off Switch

REAR PANEL CONNECTIONS AND FACILITIES

Antenna Input Socket (BNC)	
Antenna Input Fuse	
Power Input Socket	
Mains Voltage Adjuster Panel	
Power Input Fuse	
Teleprinter Supply Fuse	
Teleprinter Supply Selector Switch	
Ground Terminal	
34MHz Input/Output Socket	
34MHz Input/Output Switch	
Frequency Standard Input/Output Socket	
Frequency Standard Internal/External Switch	
35.4MHz to 65.4MHz Input/Output Socket	
35.4MHz to 65.4MHz Input/Output Switch	
AGC Output(for diversity operation))	
Line Output(s) (2 outputs for ISB version only).)	Terminal
Two 3mW, 600 - ohm outputs)	Strip
Loudspeaker Output)	
Mute Line)	
FSK Output	
1.4 MHz IF Output Socket	

ACCESSORIES

AA.660/A	Headset, 600 ohms, with ventilated ear cushions, lead and plug.
	Headsets are also available with standard ear cushions and anti-perspiration covers.

Note: All accessories and optional facilities and modules to be specified at time of order.

CHAPTER 1

PRINCIPLES OF OPERATION

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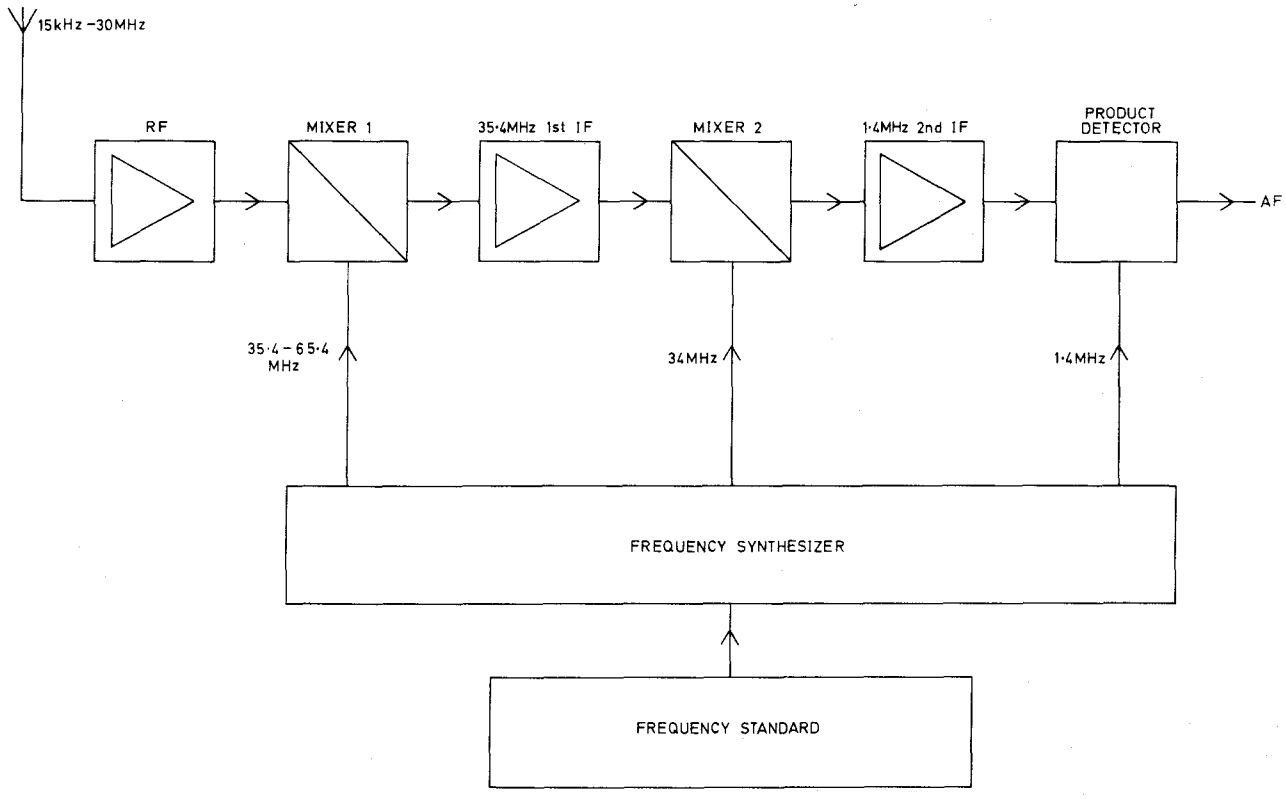
CHAPTER 1

PRINCIPLES OF OPERATION

INTRODUCTION

1. This chapter, in conjunction with the overall block diagram Fig. 1.9, describes the functional principles of the RA.1778 receiver. For explanation purposes, the receiver may be divided into two main sections, namely the frequency synthesizer and the RF/IF/AF section (see illustration below).



Simplified Block Diagram: Overall Receiver Fig. 1.1

FREQUENCY SYNTHESIS

2. The above simplified block diagram of the RA. 1778 receiver shows the three mixer injection signals produced by the frequency synthesizer. The first IF, at 35.4MHz, is high, compared with the received signal frequency at the antenna, to provide good image rejection. To produce this first IF the frequency synthesizer must provide an output signal in the range 35.4 to 65.4MHz. The second IF, at 1.4MHz, is low to provide good selectivity, and the mixer requires a fixed frequency output signal from the synthesizer at 34MHz. Finally, a frequency of 1.4MHz is needed for the product detector for the reception of SSB signals.

3. The indirect method of frequency synthesis is used where the required output frequencies (with the exception of the 1.4MHz output) are derived from voltage-

controlled oscillators which are phase locked to a common frequency standard. A simplified functional diagram of the frequency synthesizer section of the receiver is given in Fig. 1.2 at the end of the chapter.

FREQUENCY STANDARD

4. Any one of three types of 5MHz frequency standard may be fitted to the receiver, dependent upon the degree of frequency stability required. The output signal from the frequency standard is divided by five to produce a 1 MHz reference frequency for the synthesizer. Alternatively, provision is made for the use of an external 1MHz frequency standard.

1.4MHz OUTPUT

5. The 1MHz reference frequency signal from the frequency standard is further divided by five to produce an output at 200kHz. A 1.4MHz crystal filter selects the seventh harmonic and this is amplified to produce a 1.4MHz output signal at the required level.

34MHz OUTPUT

6. The 34 MHz second mixer injection frequency is derived from a 34MHz voltage controlled oscillator (VCO) which is phase locked to the 1MHz reference frequency. A sample of the VCO output is first divided by 34 and is then phase compared with the 1MHz reference frequency; any phase difference results in a correction voltage which is fed back to the VCO.

35.4 to 65.4MHz OUTPUT

7. This is the main output signal from the frequency synthesizer; it covers the frequency range 35.40000 to 65.39999 MHz in 10Hz increments and is controlled by the output of the shaft encoder and counter or by the output of the 12-channel memory circuit. The output frequency is derived from five cascaded phase-locked loops. Digital frequency information is applied to these phase-locked loops along groups of four lines, one group per digit of frequency information.

LOW FREQUENCY LOOP

8. The low frequency loop consists of a 6 to 7 MHz VCO, a programmed divider, N1, and a phase comparator. The phase comparator compares the phase of the output signal from the programmed divider with that of a 1kHz reference frequency derived from the frequency standard. Should a phase difference exist, a correction voltage is derived which is fed back to the VCO to eliminate the error.

9. The programmed divider, N1, has a division ratio of from 7000 to 6001 and is controlled by the 10Hz, 100Hz and 1kHz digits of the selected receiver operating frequency; a receiver frequency setting of 000 sets the division ratio to 7000, a setting of 999 sets the division ratio to 6001, and the division ratio for intermediate frequency

settings is given by the expression: N1 = 7000 minus selected 1kHz, 100Hz and 10Hz digits. The divider consists of a number of cascaded decade counters where the start of a count sequence may be programmed by the frequency determining lines encoder and where the counter is reset (strobed) when a count of 7000 is reached. When the VCO has been driven to the correct frequency, reset (strobe) pulses will occur at a repetition rate of exactly 1000 pulses per second, as will the output pulses applied to the phase comparator.

Tuning Example

10. Consider a receiver operating frequency of 12.34567MHz. The first mixer injection frequency required to produce the first intermediate frequency of 35.4MHz is, therefore, 12.34567MHz + 35.4MHz, which equals 47.74567MHz. Returning to the operating frequency of 12.34567MHz, only the last three digits, i.e. 567, need be considered for this part of the circuit. Thus the programmed divider, N1, is preset to start counting at 567 and counts up to 7000, a total of 6433 pulses (7000-567); this is equal to a VCO frequency of 6.433 MHz.

LOWER TRANSFER LOOP

11. The lower transfer loop, so called because the low frequency increments at its input, i.e. the 10Hz, 100Hz and 1kHz digits, are transferred to its output, consists of a programmed divider, N2, a 1.013187 to 1.019886MHz VCO, a mixer and a phase comparator. It generates, together with the upper loop, the 100kHz and 10kHz digits of the variable output frequency.

12. The programmed divider, N2, has a division ratio of from 453 to 354 and is controlled by the 100kHz and 10kHz digits of the selected receiver operating frequency. (This division ratio is modified to cover the range 455 to 352 when in the overspill condition, i.e. 20kHz beyond either end of the selected 1MHz band). A receiver frequency setting of 00 for the 100kHz and 10kHz digits results in a division ratio of 453, a setting of 99 results in a division ratio of 354 and the division ratio for intermediate frequency settings is given by the expression: N2 = 453 minus the selected 100kHz and 10kHz digits.

13. The output signal for the low frequency loop is first divided by N2 and is then applied as one input to the phase comparator. The output from the VCO is mixed with the 1MHz reference frequency, derived from the frequency standard, and the difference frequency signal from the mixer is applied as the second input to the phase comparator. Thus the output voltage from the phase comparator drives the VCO to a frequency which is exactly 1MHz above the output signal frequency from the programmed divider, N2.

Tuning Example

14. Returning to the receiver operating frequency of 12.34567MHz (see paragraph 10), the 100kHz and 10kHz digits required are 3 and 4 respectively. The division ratio of N2 is, therefore, 453-34 = 419. The 6.433MHz output frequency from the low frequency loop is divided by 419 and the result is added to 1MHz.

$$\text{Lower Transfer Loop Output} = \frac{6.433 \times 10^6}{419} + 10^6 \text{Hz}$$

$$= 1.015353\text{MHz}$$

UPPER LOOP

15. The output signal from the lower transfer loop is first divided by 100 and is then applied as one input to a phase comparator; the other phase comparator input is from a programmed divider, N2, and a 3.6 to 4.6MHz VCO is driven to the required frequency by the phase comparator output. The programmed divider, N2, is set to the same division ratio as that of the lower transfer loop, as described in paragraph 12.

Tuning Example

16. The 1.015353MHz output signal from the lower transfer loop (see paragraph 14) is first divided by 100 and is then multiplied by N2, i.e. 419.

$$\text{Upper Loop Output} = \frac{1.015353}{100} \times 419$$

$$= 0.010154 \times 419$$

$$= 4.25433 \text{ MHz}$$

UPPER TRANSFER LOOP

17. This loop, in conjunction with the HF loop, generates the MHz portion of the variable output frequency, and is controlled by the MHz digits. It consists of a programmed divider, N3, a phase comparator, a mixer and a VCO which covers the frequency range 884.950 to 948.116 kHz.

18. The programmed divider, N3, has a division ratio of from 40 to 69. In contrast to the previously described programmed dividers, N1 and N2, the division ratio of N3 is found by adding 40 to the setting of the receiver MHz digits. This is achieved by first converting the decimal 0 to 29 output from the MHz digits into a 'nines complement' code before application to the programmed divider which counts from the programmed starting point up to 99, and then to 39 when the reset occurs. Table 1 gives the conversion from decimal to nines complement code.

Decimal	BCD				Nines Complement				Decimal
	D	C	B	A	D9	C9	B9	A9	
0	0	0	0	0	1	0	0	1	9
1	0	0	0	1	1	0	0	0	8
2	0	0	1	0	0	1	1	1	7
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	0	0	4
6	0	1	1	0	0	0	1	1	3
7	0	1	1	1	0	0	1	0	2
8	1	0	0	0	0	0	0	1	1
9	1	0	0	1	0	0	0	0	0

Table 1: Decimal to Nines Complement Conversion

19. The 4.6 to 3.6MHz output from the upper loop is divided by N3 and is then applied as one input to a phase comparator. The output from the VCO is mixed with the 1MHz reference frequency, derived from the frequency standard, and the difference frequency output from the mixer is applied as the second input to the phase comparator. Thus the output voltage from the phase comparator drives the VCO to a frequency which is equal to 1MHz minus the output frequency from the programmed divider, N3.

Tuning Example

20. The division ratio for the programmed divider, N3, is obtained by adding 40 to the MHz digits of the receiver operating frequency. Thus for the frequency of 12.34567 MHz (see para. 10), N3 will be 40 plus 12 which equals 52. The 4.25433MHz output from the upper loop (see para. 16) is divided by 52 and the result is then subtracted from 1MHz to give the upper transfer loop output frequency.

$$\text{Upper Transfer Loop Output} = 1 - \frac{4.25433}{52} \text{ MHz}$$

$$= 1 - 0.081814$$
$$= 918.186 \text{ kHz}$$

HF LOOP

21. The output signal from the upper transfer loop is first divided by two and is then applied as one input to a phase comparator. The output from a 35.4 to 65.4MHz VCO is also divided by two and is then applied to the programmed divider, N3, which in turn provides the second input to the phase comparator. Thus the VCO is driven to the required frequency by the phase comparator output. The programmed divider, N3, is set to the same division ratio as that of the upper transfer loop.

Tuning Example

22. The 918.186kHz output from the upper transfer loop is first divided by two and is then multiplied by 2N3, i.e. 2 x 52, to give the final output frequency.

$$\text{First Mixer Injection Frequency} = \frac{0.918186}{2} \times 2 \times 52\text{MHz}$$

$$= 0.918186 \times 52\text{MHz}$$

$$= 47.74567 \text{ MHz}.$$

This figure is the receiver operating frequency plus the first intermediate frequency and agrees with the original frequency arrived at in paragraph 10.

23. A functional block diagram of the frequency synthesiser is given in Fig. 1.2 at the end of this chapter. To calculate the frequency or division ratio at any point in the circuit, calculate the values of N1, N2 and N3 from the frequency setting of the receiver, then substitute in the equations given. (These equations apply only when the synthesiser is in lock and the dividers are working correctly).

RF/IF/AF Section

24. The following paragraphs should be read in conjunction with the respective circuit diagrams (Figs. 1.3 to 1.9) .

RF UNIT

25. The received signal at the antenna, in the frequency range 15kHz to 30MHz, is fed via a 500mA fuse and a re-radiation filter to a wideband protection stage. This consists of a voltage sensitive circuit and a relay (RLQ/1), which open-circuits the RF path for signals which exceed approximately 3V e.m.f. at the antenna socket. This relay is also used for receiver muting and operates when an earth is applied to the rear panel MUTE terminal. After operation of the relay the receiver is protected from input signals at the antenna socket of up to at least 30V e.m.f. with automatic recovery.

26. From relay contact RLQ1 the received signal is applied to a 30MHz low-pass filter and then takes one of a number of paths dependent on the selected position of the front panel MHz switch, as detailed below.

27. (1) MHz reading of OMHz: An earth from the decoder board is connected to relays RLA/1 and RLB/1. The relays energise, the received signal from RLQ1 and the low-pass filter is applied to a 1MHz low-pass filter, via RLA1, and thence, via RLB1 and contact RLR1 of the normally energised protection relay RLR/1, to the wideband RF amplifier.

(2) MHz reading of other than OMHz and RF TUNE control set to WB (wideband) Operation of the microswitch SA (controlled by RF TUNE control) connects an earth from the decoder board to relays RLN/1 and RLP/1. The relays energise and a path is provided from the low-pass filter to the wideband RF amplifier via RLN/1, RLP1 and contact RLR1 of the normally energised protection relay, RLR/1.

(3) MHz reading of other than OMHz, RF TUNE control not in WB position: An earth from the decoder board is applied to the appropriate pair of tuneable-circuit selection relays and a common +12V relay supply is provided by the normally closed contacts of the microswitch. The contacts of the selected relays close and the received signal from the low-pass filter is applied to the appropriate tuned circuit, tuned by the RF TUNE control, and thence to the RF amplifier via RLR1.

Protection Stage

28. A further protection stage is fitted to the RF board. This allows for 'working through' off-tune signals of up to approximately 10V e.m.f. at the antenna socket The circuit is similar to that of the wideband protection stage; relay RLR/1 becomes de-energised once the 3V e.m.f. threshold is exceeded and the signal path to the RF amplifier is broken.

RF Amplifier

29. A conventional circuit of high linearity is used. After amplification, the received signal is passed via a 30MHz low-pass filter to the first mixer.

FIRST MIXER

30. The output signal from the RF unit is mixed with the 35.4 to 65.4 MHz local oscillator signal, from the frequency synthesizer, to produce the first IF at 35.4MHz.

31. The local oscillator signal is applied to one of two filters, dependant on the setting of the front panel MHz digits; for settings of 0, 1, 2 or 3MHz, a filter with a passband of 35.415 to 39.4MHz is selected whereas for settings of 4 to 29 MHz a filter with a passband of 39.4 to 65.4 MHz is selected. These filters attenuate noise at the IF frequency.

32. The output signal from the selected filter is applied to a drive amplifier and then to a high performance mixer. A detector and amplifier circuit provides an indication of DRIVE LEVEL at the front panel meter.

33. The output signal from the RF unit is mixed with the local oscillator signal and the difference frequency is fed via a 35.4 MHz band-pass filter to the second mixer.

SECOND MIXER

34. The 35.4 MHz first IF output from the first mixer is amplified and is then mixed with the 34MHz output from the frequency synthesizer. This produces the second IF, at 1.4MHz, which is fed to the IF amplifier stages via the front panel selected SSB, 1SB or symmetrical filter (see Fig 1).

35. The output signal level from the first stage of IF amplification is automatically controlled by the AGC1 input from the main IF/AF board (and, in 1SB versions, AGC2 from the 1SB IF/AF board) via a voltage controlled attenuator. The output from the second stage of IF amplification is applied to a balanced mixer via a 35.4MHz band-pass filter.

36. The 34MHz second mixer injection frequency, from the frequency synthesizer section, is applied to the mixer via a 34MHz band-pass filter. The difference frequency output from the mixer, at 1.4MHz, is amplified before being applied to the filter board.

MAIN IF/AF STAGES

37. The 1.4MHz second IF output signal from the second mixer is applied to the IF/AF board via the selected 1.4MHz filter (see Fig 1). The IF amplifier stage consists of two automatic gain controlled integrated circuit amplifiers. These feed two buffer amplifier stages; the output from one is applied to the product and AM detector, whilst the output from the other is applied to the AGC detector and the 1.4MHz output amplifier.

Product and AM Detector

38. Detector selection is controlled by the front panel MODE switch. The AM detector, which is of the envelope type, is selected in the AM position of the MODE switch, and a modified Foster-Seeley type of product detector is selected for all other modes.

AGC Detector

39. The AGC detector develops a d.c. voltage which is proportional to the amplitude of the 1.4MHz IF signal. This gain control voltage, after amplification, is applied to the 35.4MHz first IF amplifier (on the second mixer board), a rear panel terminal and also to the 1.4MHz second IF amplifier via the front panel AGC switch. This switch provides for the selection of either a long or a short AGC time constant. In the OFF position the AGC voltage is removed from the 1.4MHz second IF amplifier and the gain of this stage is then controlled by the front panel IF GAIN control.

Audio Pre-Amplifier

40. The output signal from either the product detector or the AM detector is applied to the audio pre-amplifier. This stage has a muting capability such that the output is inhibited when an earth is applied to the MUTE terminal on the rear panel. The amplified audio output is applied to the line amplifier via the AM/USB LINE LEVEL control and also to the loudspeaker amplifier (the input switching to the loudspeaker amplifier is only necessary in ISB versions of the receiver).

Loudspeaker Amplifier

41. The loudspeaker amplifier provides a 50mW output for the internal loudspeaker, a 1 Watt, 8 ohm output for an externally connected loudspeaker, and two 10mW, 600 ohm headphone outputs.

ISB IF/AF BOARD

42. This board, which is fitted to ISB versions of the receiver only, is similar to the main IF/AF board except that the AM detector is not utilised and a loudspeaker amplifier is not fitted.

AUTOMATIC FREQUENCY CONTROL

General Description

43. The purpose of the AFC system is to effectively stabilise the signal received from a drifting transmitter. This function is performed by slightly varying the frequency of the 34 MHz injection to the second mixer, maintaining a constant 1.4 MHz output signal. The 34 MHz injection is provided by an oscillator phase locked to an applied 1 MHz input signal.

44. With AFC switched OFF, the 34 MHz generator uses the 1 MHz derived directly from the frequency standard. When the AFC is switched ON, the generator uses a 1 MHz signal derived from the AFC board. The exact frequency of this signal is 1 MHz - $\frac{\Delta}{34}$ where Δ is the positive frequency error of the incoming carrier. The AFC board accepts the 1.4 MHz carrier via the carrier filter, senses that an error is occurring, and adjusts the frequency of its 1MHz output to correct this error.

Operation of the Correction System

45. The 1.4 MHz carrier arrives at the input of the AFC board, after extraction from the main IF signal via a 100 Hz carrier filter. The carrier is amplified, converted to 400 kHz by mixing with a 1 MHz signal and amplified again, resulting in a 400 kHz square wave suitable for driving CMOS.

46. The square wave is applied to the input of the digital mixer. The mixer is clocked by two 200 kHz signals spaced 72° in phase (1/5 of a clock period). The mixer provides two outputs, one a square wave at the error frequency the other d.c. up/down information which is a logic '1' for negative error, and a '0' for positive error, for example:

(a) If the transmitter drifts 100 Hz high, the error output will be 100 Hz, and the output a '0'.

(b) If the transmitter drifts 50 Hz low, the error output will be 50 Hz, and the up/down output a '1'.

The two outputs are fed to a 12-bit binary counter, which increments up or down at the error rate.

47. The ten most significant outputs (Q2 to Q11) are connected to a 10-bit digital to analogue converter, and the analogue output is used, after buffering and level shifting, as the varactor control voltage of a 7MHz oscillator. The 7MHz oscillator signal is divided down to 1MHz, and taken to the 34 MHz board. Since the correction rate is proportional to the error frequency, the lock up time is a logarithmic function of the initial error.

FREQUENCY SHIFT KEYING

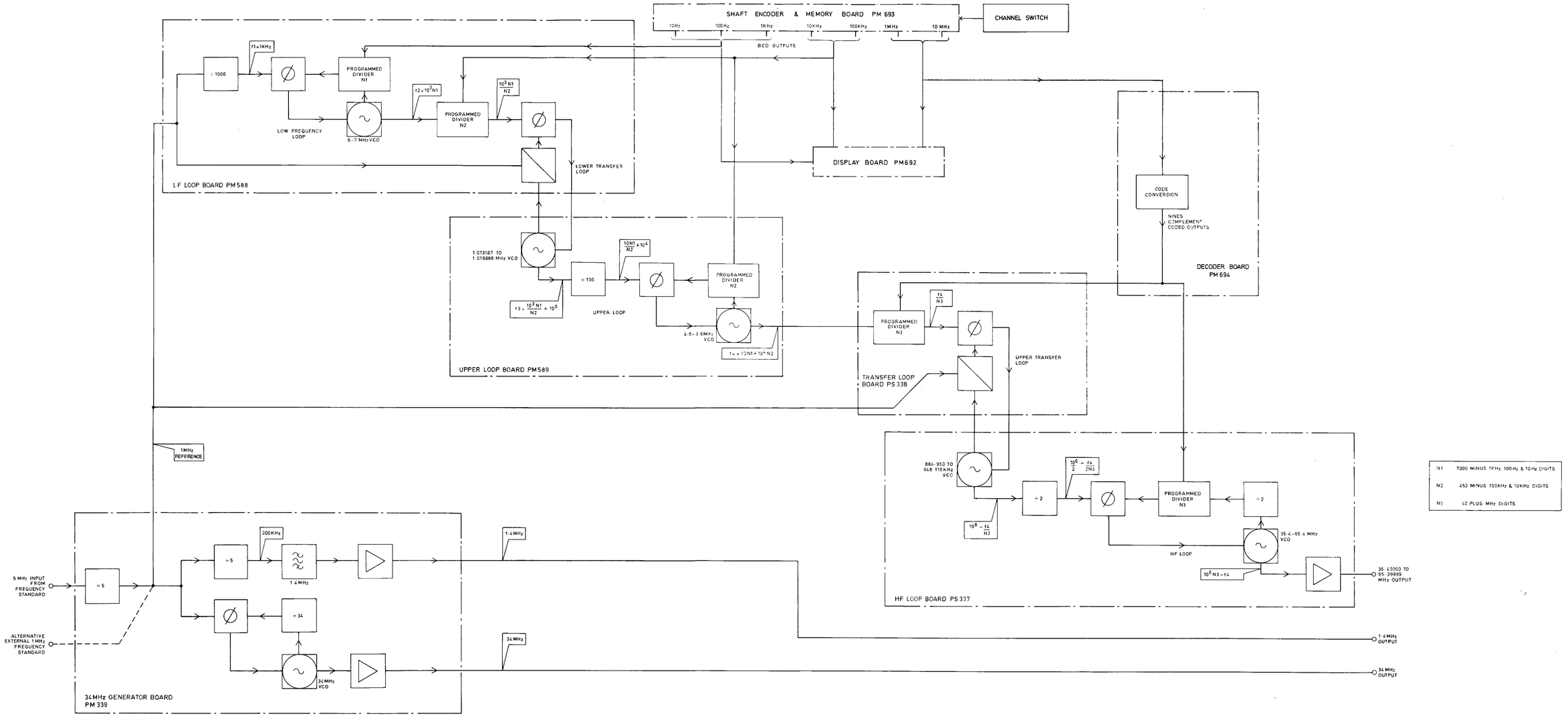
48. The optional FSK board converts a frequency shift keyed signal into bipolar d.c. information suitable for operating a teleprinter or similar device. Provision is included for dual diversity operation (using a pair of receivers), with keying speeds up to 200 bauds and a frequency shift range of 85 Hz to 850 Hz.

49. The 1.4MHz IF output from the selected IF filter is applied to a mixer via a 1.4MHz band pass filter. The second input to the mixer is a 1398 kHz signal generated by a crystal oscillator. The difference output from the mixer at 2kHz, is clipped by a limiting amplifier and fed to a frequency discriminator consisting of two active band-pass filters and two full-wave rectifier circuits.

50. The output from the discriminator is compared with a reference voltage to produce a digital FSK signal which is taken to a rear panel terminal for connection to a second receiver for diversity operation; it is also applied via a schmitt trigger to a diversity signal comparator and switch.

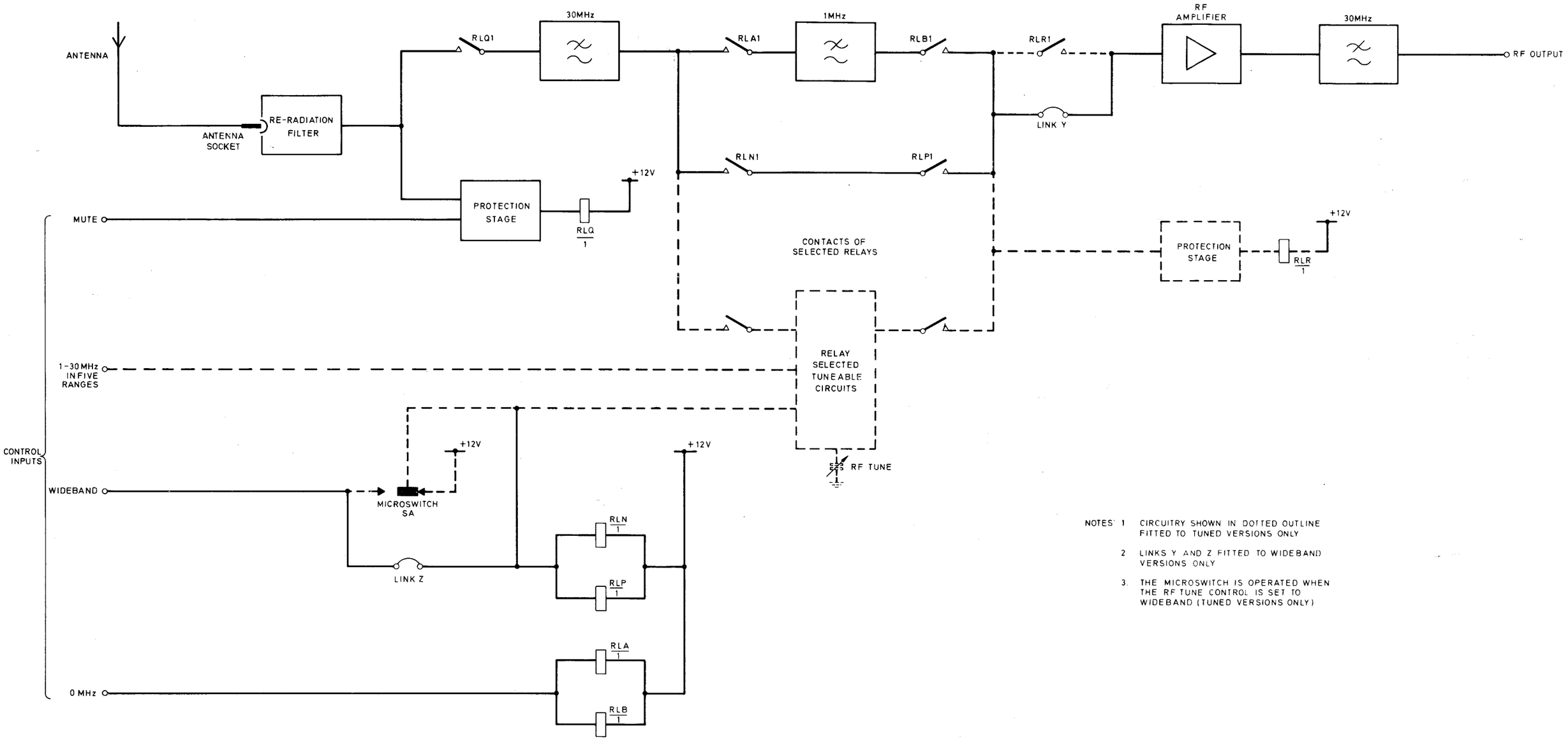
51. An AGC comparator compares the diversity AGC input (from the second receiver) with a voltage derived from the AGC output from the main IF/AF board. The output from the AGC comparator, limited by a zener diode to either +5V (approximately) or -0.7V is applied to the diversity signal comparator and switch.

52. The diversity signal comparator and switch employs digital techniques to compare the two FSK signals from the master and slave receivers and, in conjunction with the information obtained from the AGC comparator, opens a path for the selected FSK signal. Switching only occurs when the mark or space output signal from one receiver is coincident with that from the second receiver. This is to avoid the introduction of switching distortion. The output signal from the diversity signal comparator and switch is routed by the MODE switch-controlled on/off and normal/reverse switching circuits to the relay drive amplifier.



Simplified Functional Diagram: Frequency Synthesis

Fig.1.2



NOTES: 1. CIRCUITRY SHOWN IN DOTTED OUTLINE FITTED TO TUNED VERSIONS ONLY

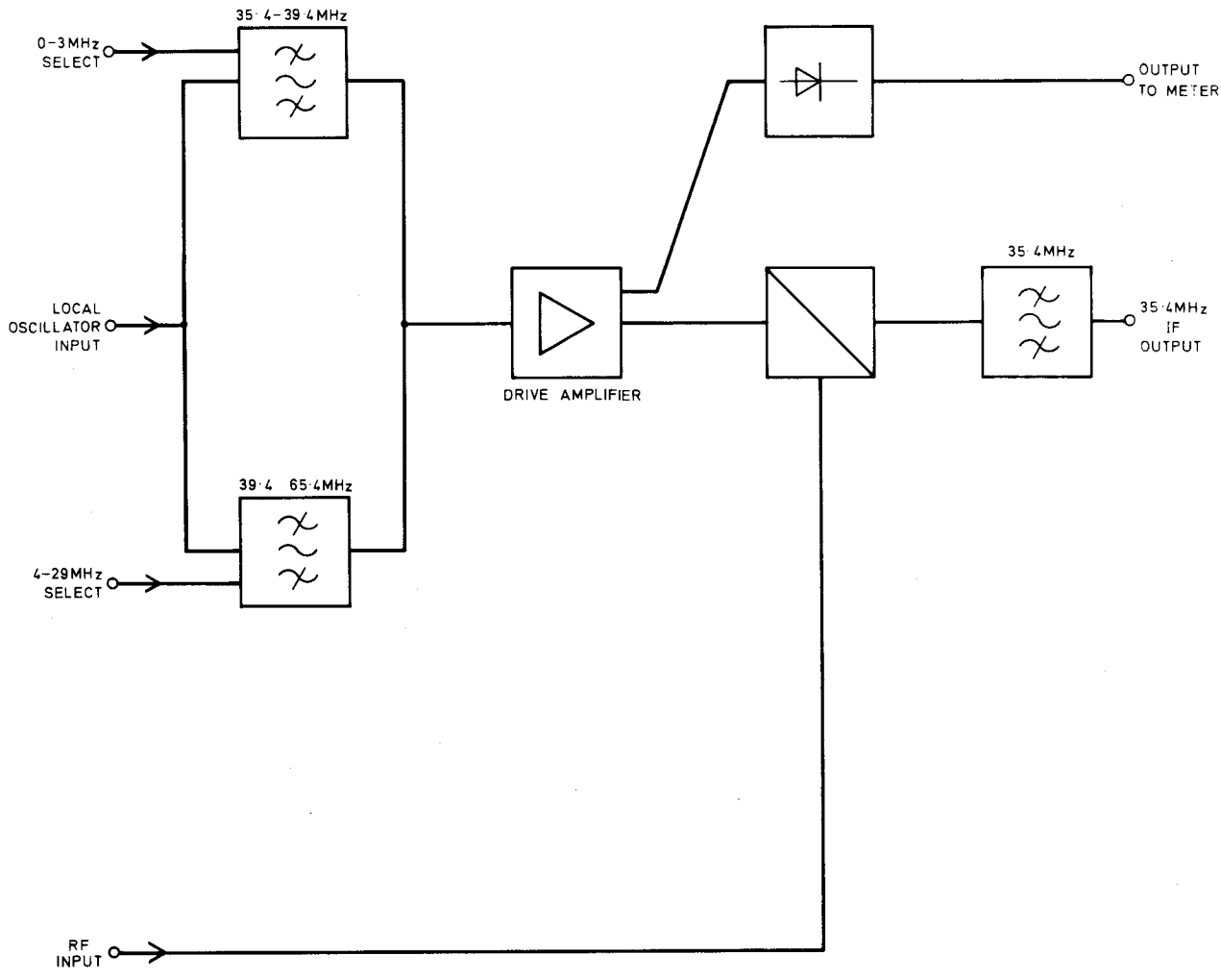
2. LINKS Y AND Z FITTED TO WIDEBAND VERSIONS ONLY

3. THE MICROSWITCH IS OPERATED WHEN THE RF TUNE CONTROL IS SET TO WIDEBAND (TUNED VERSIONS ONLY)

RACAL
WOH 7049

Simplified Block Diagram : RF Unit

Fig. 1-3



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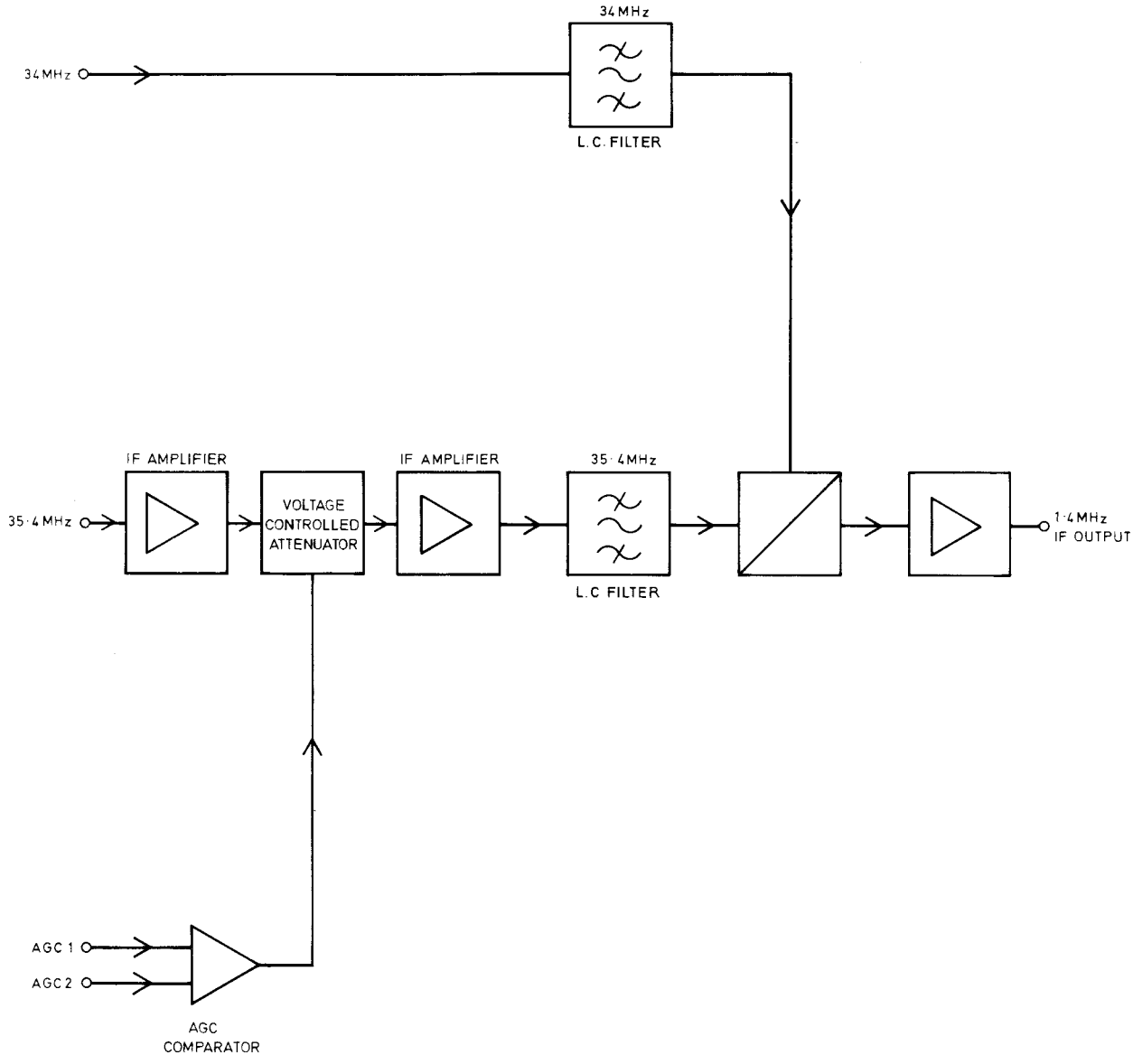
Simplified Block Diagram: First Mixer PS 512 Fig. 1·4



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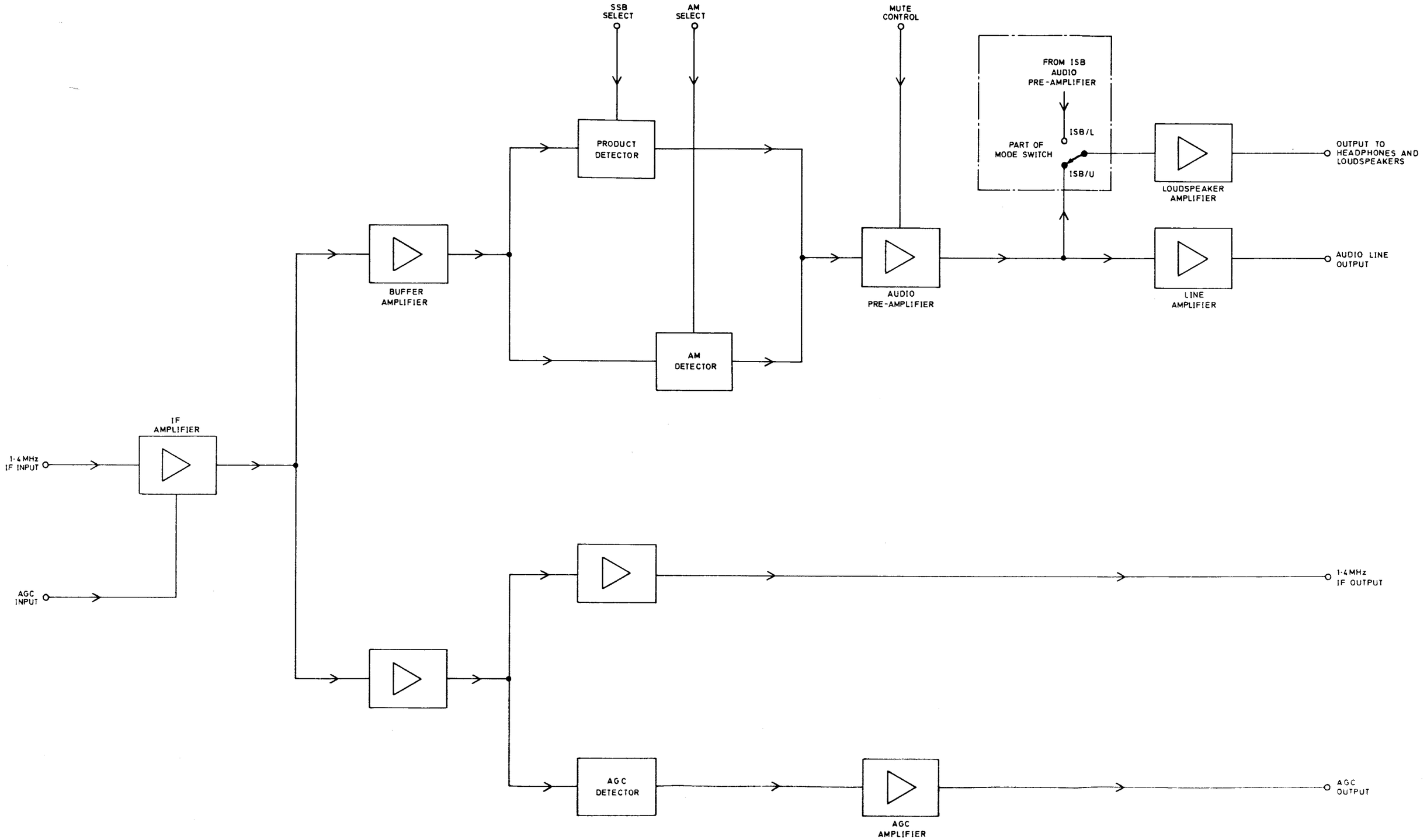
Simplified Block Diagram: Second Mixer Fig. 1·5
PM336



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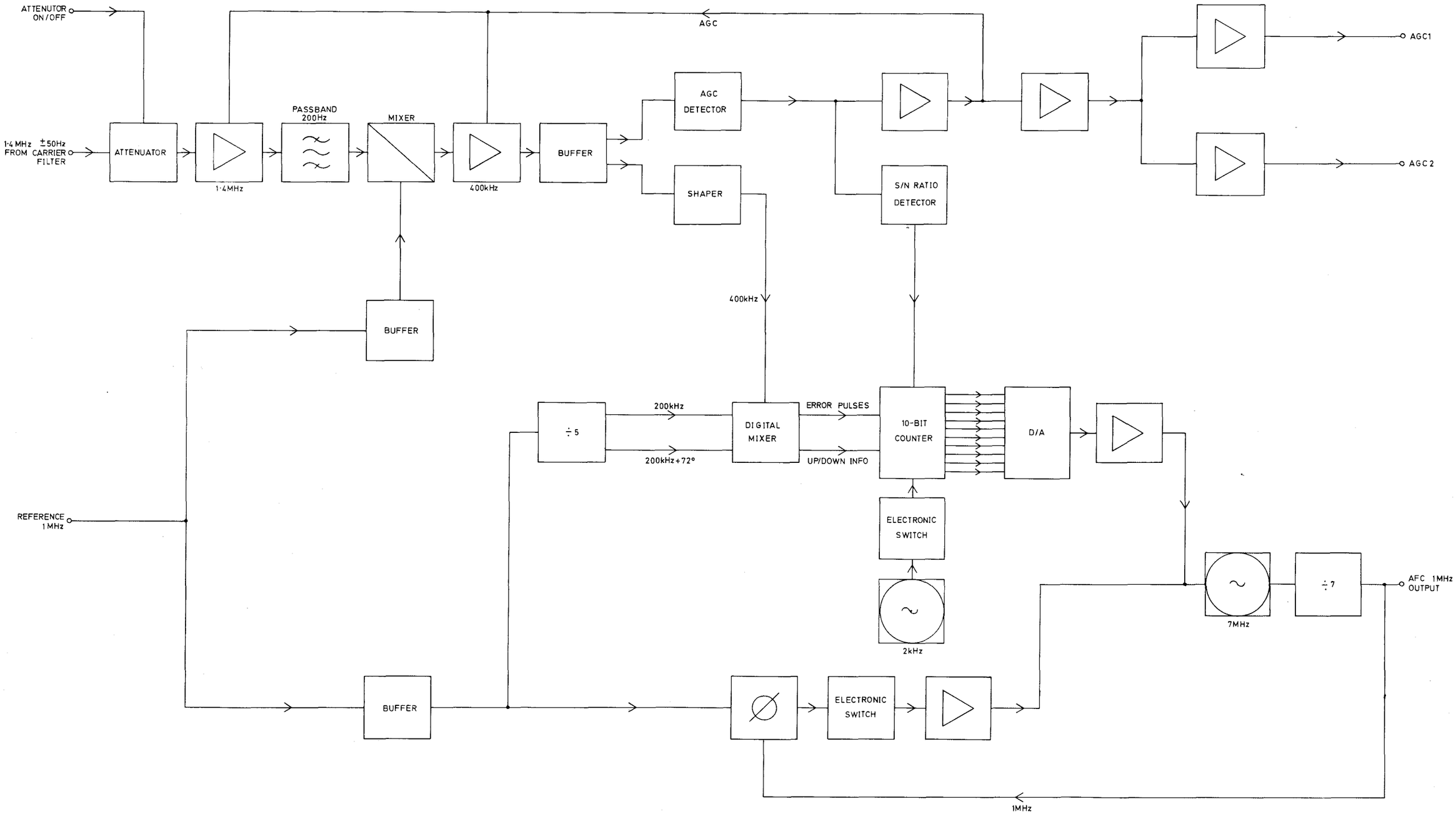
Simplified block diagram : main IF/AF board PM364/1

Fig. 1·6



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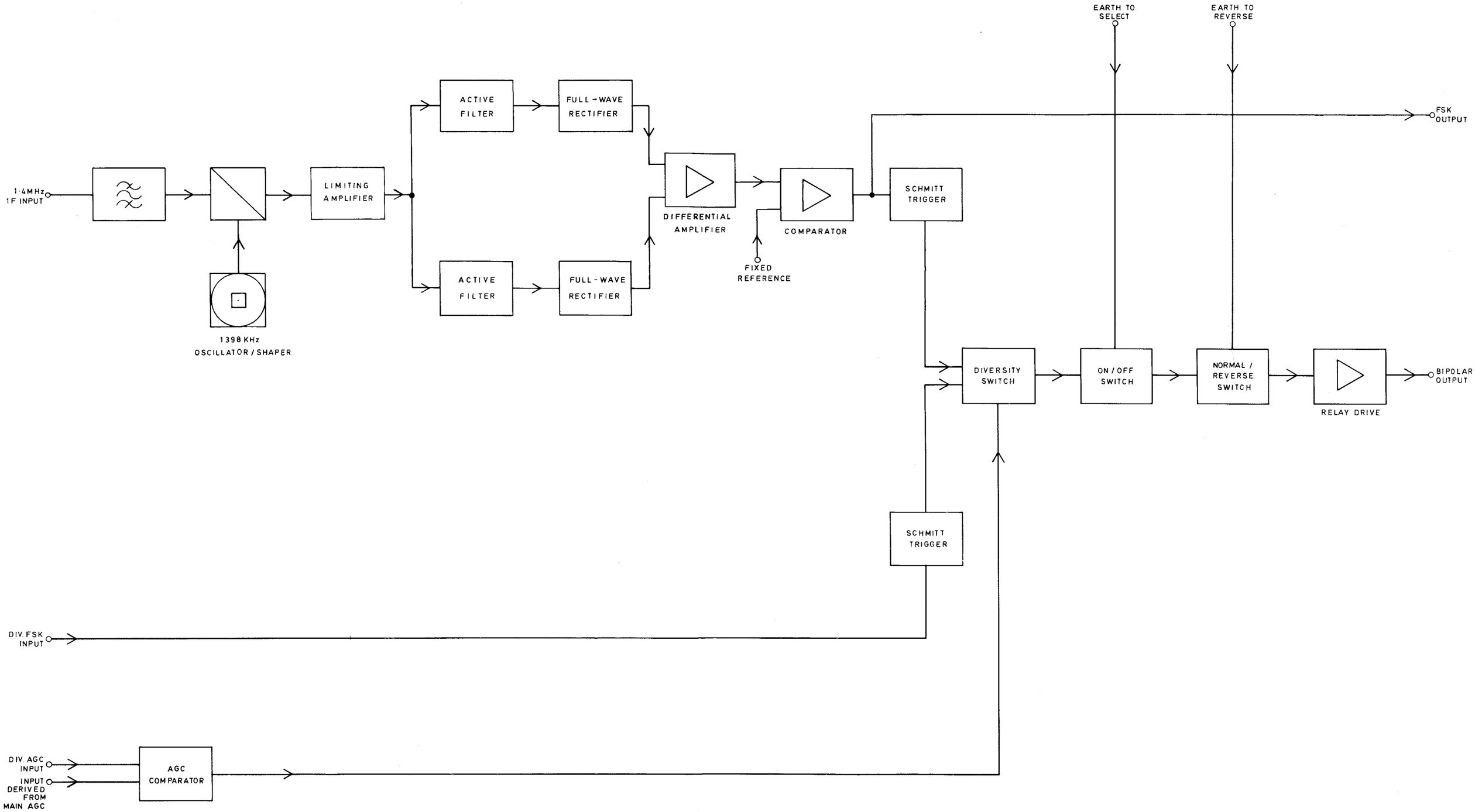
Simplified Block Diagram :
AFC Board PM664

Fig. 1·7



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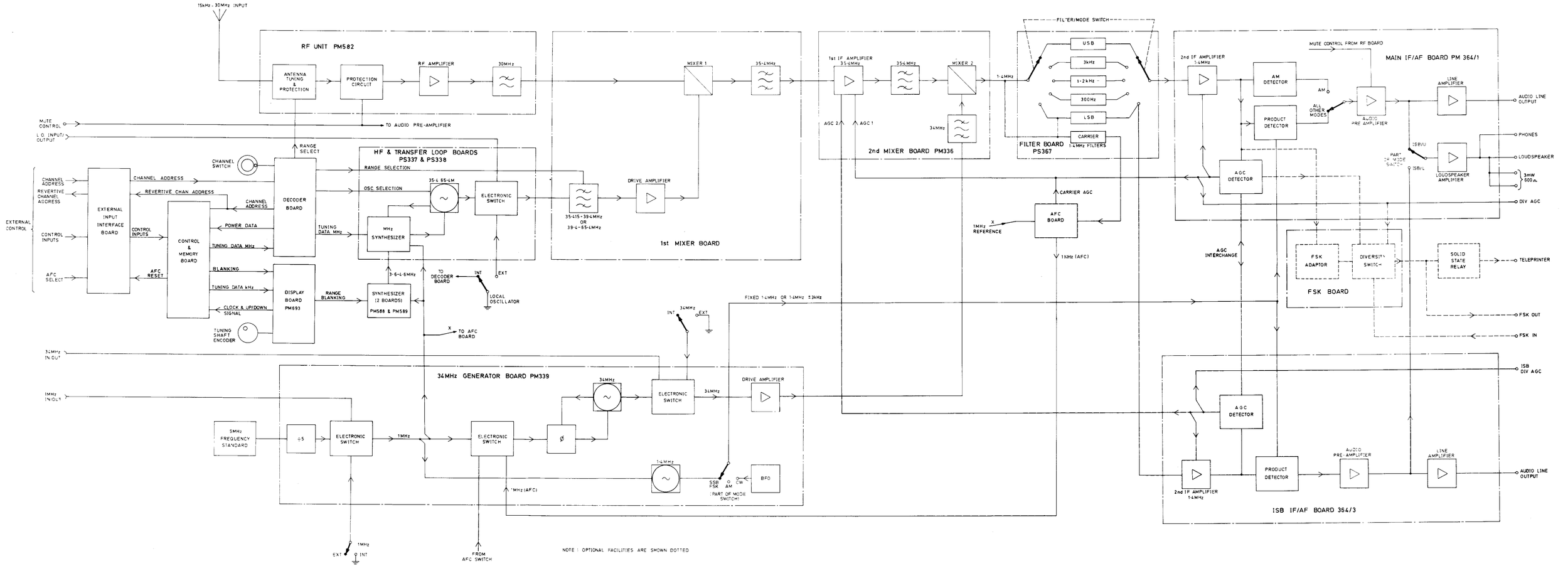
Simplified Block Diagram: FSK Board PM-368

Fig. 1·8



RACAL WOH9318

Block Diagram : RA.1778 HF Communications Receiver

Fig.1.9

CHAPTER 2

LOW FREQUENCY LOOP BOARD PM588

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CHAPTER 2

LOW FREQUENCY LOOP BOARD PM588

INTRODUCTION

1. This board contains the low frequency loop and also the programmed divider, mixer phase comparator and out-of-lock detector circuits of the lower transfer loop; the lower transfer loop VCO is contained on the upper loop board (PM589). A circuit diagram of the board is given at the end of this chapter.

6-7 MHz Voltage Controlled Oscillator (VCO)

2. The VCO is a Colpitts circuit consisting of L1, C2 and D1 (the varactor diode in series with C1.). The active component is ML1 buffered by transistor TR1. The square wave output signal is applied to the programmed divider, N1, and also to the programmed divider of the lower transfer loop, N2, via G8 (ML1).

Programmed Divider N1 (See Fig. 1.2)

3. The programmed divider consists of four presettable decade counters, ML3, ML5, ML6, ML10, NAND gates G2, G3 and a dual J-K flip-flop, ML11.

4. The decade counters have strobed parallel-entry capability such that the starting point of a count sequence may be preset (see Technical Appendix A). A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do,) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

5. The division ratio of the programmed divider, which is controlled by the 1kHz, 100Hz, 10Hz digits of the selected operating frequency, is given by the expression N1 = 7000 minus the selected digits, i.e. the division ratio is 7000 for a setting of 000 and is 6001 for a setting of 999. The operation of the divider is described below.

6. Binary coded decimal (BCD) frequency setting information is applied to the data inputs of ML3 (10Hz data), ML5 (100Hz data) and ML6 (1kHz data). The Da, Dc, and Dd data inputs of ML10 are connected to the 0V line whilst the Db data input is floating and is equivalent to logic '1'. ML10, therefore, is set to start counting at binary 2.

7. To start a counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) input of each decade counter. As described in paragraph 4, this causes the logic level applied to each input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative-going edge of the clock pulse (from the VCO) is applied to the clock 1 input of ML3 and each pulse is now counted until an output from the counter of 8996 is reached, i.e. until the Do output from ML10 is at '1', the Ao and Do outputs from ML6 and ML5 are at '1', and the Bo and Co outputs

from ML3 are at '1'. Since ML10 is set to start counting at 2, and since the remaining counters may be set to start counting at any number from 0 to 9, the maximum number of clock pulses that may be counted is equal to 8996 minus 2000 which equals 6996.

8. Once a count of 8996 is reached, the input lines to the NAND gate, G2 are all at a logic '1' and the '0' output, inverted by G3, is applied to the K input of a dual negative-edge triggered J-K flip-flop, ML11. The operation of this flip-flop, which generates the strobe pulse for the decade counters is given in the Timing Diagram, Fig.2.1. From this diagram it can be seen that two clock pulses elapse before the start of the strobe pulse and a further two clock pulses elapse to coincide with the end of the strobe pulse. Thus four clock pulses are counted by ML11, making a total count of 7000, i.e. 6996 + 4.

Reference Frequency Divider

9. The 1MHz input signal at board pins 45 and 46 is coupled by transformer T1 to a shaper stage, TR2. The output signal from the collector of TR2 is applied to a divider consisting of three cascaded decade dividers, ML2, ML4, ML7 and the output signal at 1000 pps, is applied to one of the clock inputs of the LF loop phase comparator, ML8.

LF Loop Phase Comparator

10. The phase comparator consists of a dual D-type flip-flop, ML8, a two-input NAND gate, G4 and a voltage control circuit, TR3, TR4, TR5. It compares the output signal frequency from the programmed divider, N1, with the output signal frequency from the reference divider; any error between these two frequencies is used to develop a d.c. voltage which is applied to the 6 to 7 MHz VCO to eliminate the error. The action of the circuit is as follows:

11. The output signal from the programmed divider, N1, from ML10 pin 12, consists of positive-going pulses which are applied to the clock input of ML8b (Pin 3). The output signal from the reference divider also consists of positive-going pulses, and these are applied to the clock input of ML8a, (Pin 11). The D inputs of ML8, at pins 2 and 12, are both taken to the +5V rail (logic '1') via R50. Thus when the positive edge from ML10 pin 12 clocks ML8b, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output changes to '0'. Similarly, when the positive edge from the reference divider clocks ML8a, the Q output at pin 9 changes to '1' and the $\overline{Q}$ output changes to '0'. When both Q outputs are at '1' the output from the NAND gate, G4 (ML1), changes to '0' clearing both flip-flops at ML8 via R53 and thus resets the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

12. Consider the case where the 6 to 7 MHz VCO frequency is high. This will mean that the positive edge from the programmed divider will occur before the positive edge from the reference divider. The resulting setting and resetting of the flip-flops causes increased conduction of TR4, due to the Q output waveform from ML8b (see Timing Diagram Fig. 2.2) as compared with the conduction of TR5; this causes the voltage at the collector of TR4 to become less positive, thereby reducing the voltage applied to varactor diode, D1, and reducing the VCO frequency.

13. If the VCO frequency is low, the programmed divider output pulse will occur after the reference pulse, the Q output waveform from ML8a will cause increased conduction of TR5 and the voltage at the collector of TR4 will become more positive. The increased voltage applied to the varactor diode causes the VCO frequency to increase, thus correcting the error.

14. When the two signals are equal in frequency and phase the two flip-flops of ML8 are clocked at the same time, the two Q output waveforms are equal and varactor line voltage remains constant.

LF Loop Out-of-Lock Detector

15. The LF loop out-of-lock detector consists of a bistable latch, G5, G6 and an output buffer, G7. The $\bar{Q}$ outputs from the phase comparator, ML8, are connected directly to G5, and also to G6 via integrating components, R50, C19 and R51, C20. Under phase-locked conditions the in-phase negative-going $\bar{Q}$ output pulses from ML8, pins 6 and 8 are prevented from reaching G6 due to the time constants presented by the integrating components. Pins 1 and 2 of G6 therefore float up to logic '1' and the resulting logic '0' output, at G6 pin 12, forces the output of G5 to logic '1'. The inputs to the output buffer, G7, are connected in parallel with those of G6 and the logic '0' in-lock indication output is taken to board pin 1.

16. When an out-of-lock condition exists, the clock input waveforms applied to ML8 are no longer in phase and the resultant longer-duration negative-going output pulses from ML8 pin 6 or ML8 pin 8 (dependant on whether a phase lead or a phase lag exists) are sufficient in width to overcome the time constant presented by the respective integrating components. The effect of this is to produce an alternating '0' - '1' output signal from the buffer, G7, as shown in the timing diagram, Fig. 2.3.

Programmed Divider N2 (See Fig. 1.2).

17. This programmed divider, which forms part of the lower transfer loop, consists of three presettable decade counters, ML14, ML15, ML19, NAND gates, G10, G11 and a dual J-K flip-flop, ML20.

18. The decade counters have strobed parallel - entry capability such that the starting point of a count sequency may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

19. The division ratio of the divider is controlled by the 10kHz and 100kHz digits of the selected operating frequency. The division ratio is given by the expression N2 = 453 minus selected digits; i.e. the division ratio is 453 for a setting of 00 and is 354 for a setting of 99.

20. BCD frequency setting information is applied to the data inputs of ML14 (10kHz data) and ML15 (100kHz data). The data inputs to ML19 are all at 0V (logic '0') and under this condition ML19 starts counting at zero.

21. To start a counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) input of each decade counter. As described in paragraph 19, this causes the logic level applied to each data input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative-going edge of the clock pulse (the output from the LF loop via G8) is applied to the clock 1 input of ML14 and each pulse is counted until a count of 449 is reached, i.e. until the Co output from ML19 is at '1'. Thus when a count of 449 is reached the four input lines to the NAND gates G10 are at logic '1' and the resulting '0' output, inverted by G11, is applied to the K input of a dual, negative-edge triggered, J-K flip-flop, ML20. The operation of this flip-flop, which generates the strobe pulse for the decade counters, is given in the timing diagram, Fig. 2.4. From this diagram it can be seen that two clock pulses elapse before the start of the strobe pulse and a further two clock pulses elapse to coincide with the end of the strobe pulse, thus four clock pulses are counted by ML20, making a total count of 453, i.e. 449 + 4, before the start of the next sequence.

Mixer Stage.

22. ML13 is an integrated circuit mixer where the 1MHz square wave from TR2 is applied to the carrier input, pin 8, and the 1.013 - 1.020 MHz output from the lower transfer loop oscillator is applied to the signal input, pin 1. The output signal from the mixer, at pin 6, is applied to a low-pass filter, C27, C28, L3, which selects the difference frequency. The filter is followed by a buffer stage, TR19, and an output shaper, G9, which is fed from a voltage regulator consisting of TR20 and a 5.6V zener diode, D3; the square-wave output from G9 is applied to the lower transfer loop phase comparator.

Lower Transfer Loop Phase Comparator

23. The phase comparator consists of a dual D-type flip-flop, ML16, NAND gates, G15, and a voltage control circuit, TR21, TR22, TR23. It compares the output signal frequency from the mixer with the output signal frequency from the programmed divider N2; any error between these two frequencies is used to develop a d.c. voltage which is applied to the lower transfer loop oscillator to eliminate the error. The action of the circuit is described below.

24. The output signal from the programmed divider, at ML20 pin 3, consists of negative-going pulses which are applied to the clock input of ML16b (pin 11). The output signal from the mixer via ML17 pin 6 is applied to the clock input of ML16a (pin 3). The D inputs of ML16, at pins 2 and 12, are both taken to the +5V (logic '1') via R66. Thus when the positive edge from ML20 pin 3 clocks ML16b, the Q output at pin 9 changes to '1' and the $\bar{Q}$ output at pin 8 changes to '0'. Similarly, when the positive edge from ML17 pin 6 clocks ML16a, the Q output at pin 5 changes to '1' and the $\bar{Q}$ output at pin 6 changes to '0'. When both Q outputs are at '1' the output from the NAND gate, G15, changes to '0' clearing both flip-flops of ML16 via R74 and thus resets the Q outputs to '0' and the

and the $\bar{Q}$ outputs to '1'.

25. Consider the case where the output frequency from the mixer is high (due to an increase in the frequency of the lower transfer loop oscillator). This will mean that the positive edge from the programmed divider will occur after the positive edge from the mixer. The resulting setting and resetting of the flip-flops causes increased conduction of TR23, due to the Q output waveform from ML16a (see timing diagram, Fig. 2.2) as compared with the conduction of TR21; this causes the voltage at the collector of TR23 to become less positive, thereby reducing the voltage applied to the varactor diode of the lower transfer loop oscillator. This causes a reduction in the oscillator frequency and a corresponding decrease in the output frequency from the mixer.

26. If the mixer output frequency is low (due to a decrease in the frequency of the lower transfer loop oscillator), the positive edge from the programmed divider will occur before the edge from the mixer, the Q output waveform from ML16b will cause increased conduction of TR21 and the voltage at the collector of TR23 will become more positive. The increased voltage applied to the varactor diode of the lower transfer loop oscillator causes an increase in the oscillator frequency and a corresponding increase in the output frequency from the mixer.

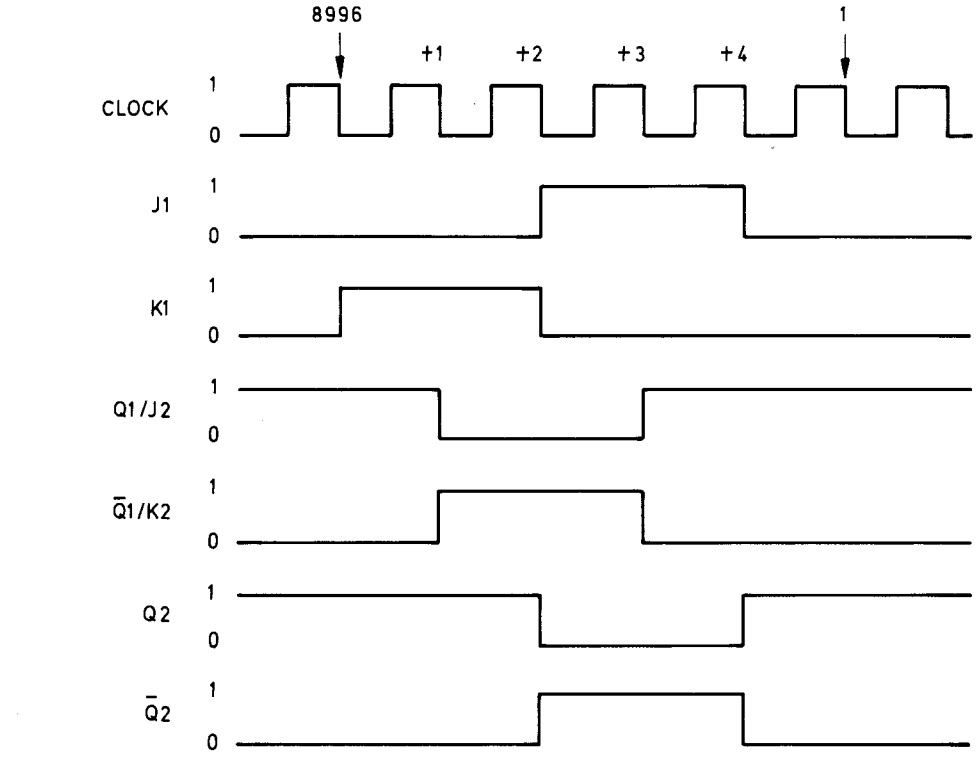
27. When the two signals are equal in frequency and phase the two flip-flops of ML16 are clocked at the same time, the two Q output waveforms are equal and the varactor line voltage remains constant.

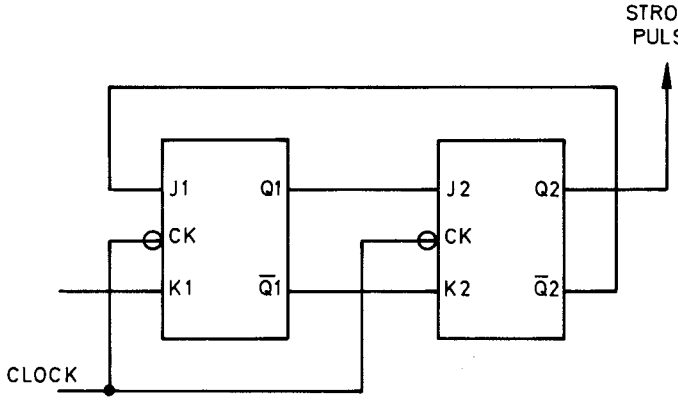
Lower Transfer Loop Out-of-Lock Detector

28. This consists of a bistable latch, G12, G13, and an output buffer, G14. It is fed from the $\bar{Q}$ outputs of the phase comparator flip-flop, ML16, and produces a steady logic '0' in-lock signal or an alternating '0' - '1' out-of-lock signal at board pin 42. The action of the circuit, which is identical to that of the LF loop lock detector (paragraph 13) is depicted in the timing diagram, Fig. 2.3.

Adjustments

29. Refer to Chapter 23, paragraphs 16 to 18 for details of adjustments to the Low Frequency Loop Board PM588.

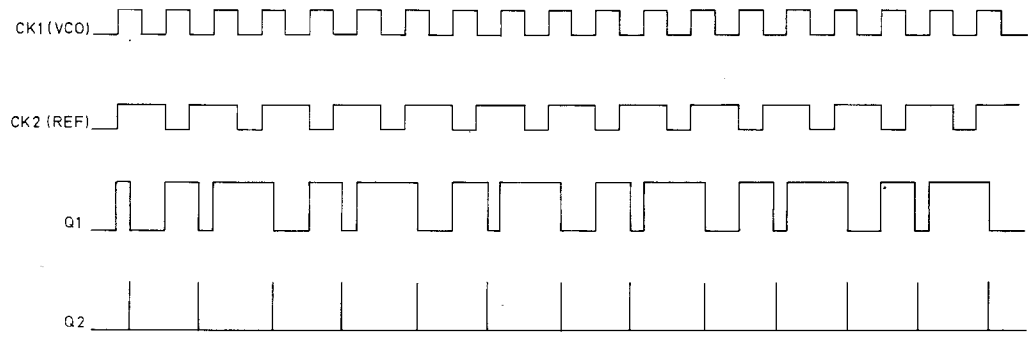




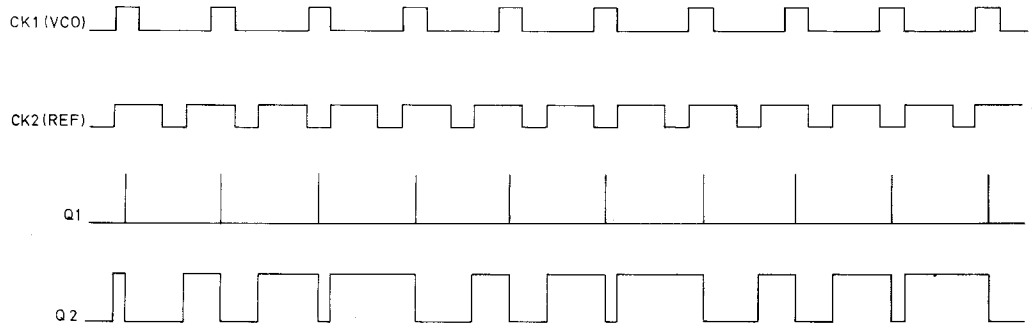
TRUTH TABLE (Each Section)		
tn		tn + 1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\bar{Q}$n

Timing Diagram: Strobe Pulse Generation LF Loop PM588

Fig.1

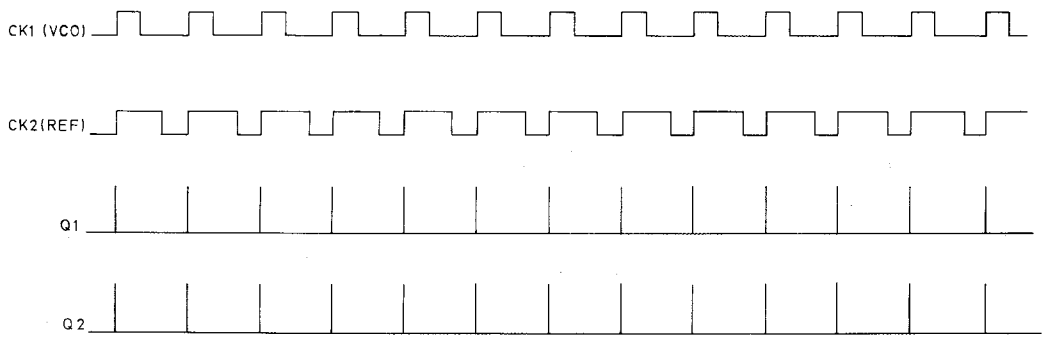


OUT-OF-LOCK : VCO FREQUENCY LOW



OUT-OF-LOCK : VCO FREQUENCY LOW

NOTE : ONLY RISING CLOCK EDGES ARE SIGNIFICANT.
ONE OUTPUT (Q1 OR Q2) PRODUCES SHORT (50-200nS) PULSES ; THE OTHER PRODUCES LONG PULSES, ACCORDING TO WHICH FREQUENCY IS THE HIGHER.
THE LONG PULSES CANNOT BE DISPLAYED ON AN OSCILLOSCOPE, AS THEY ARE OF VARYING LENTHS.

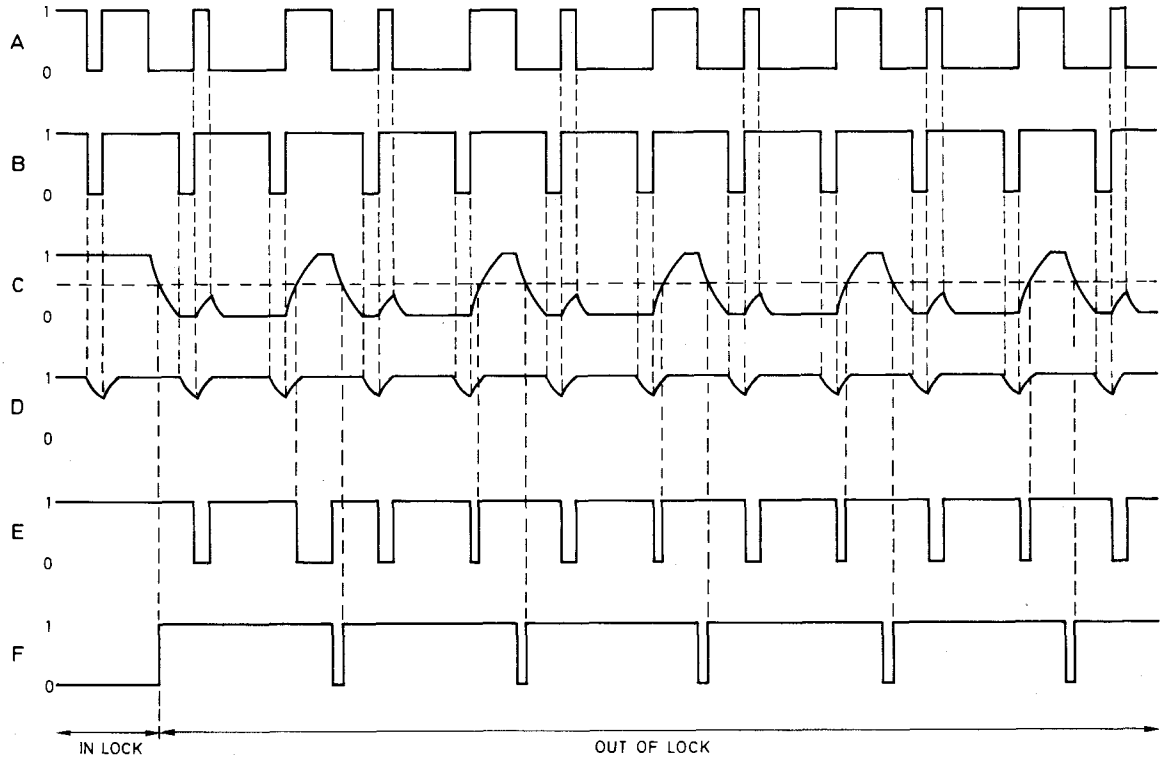


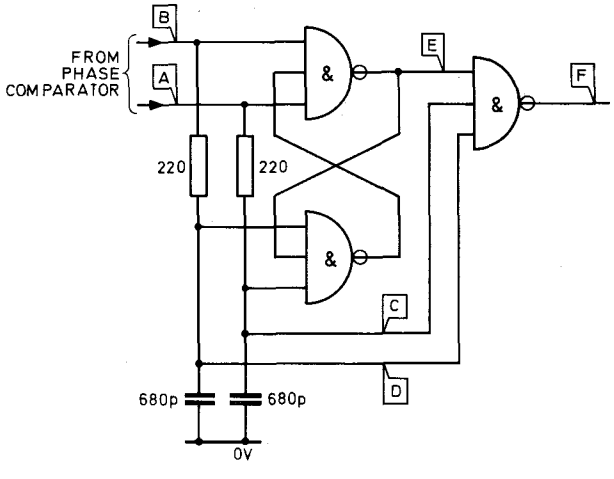
IN LOCK : VCO FREQUENCY AND REFERENCE EQUAL

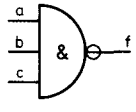
NOTE : ONLY RISING CLOCK EDGES ARE SIGNIFICANT.
Q1 AND Q2 OUTPUT PULSE LENGTHS ARE OF THE ORDER OF 50-200nS

Timing Diagram : Phase Comparator

Fig.2·2







TRUTH TABLE 3-INPUT NAND GATE			
a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

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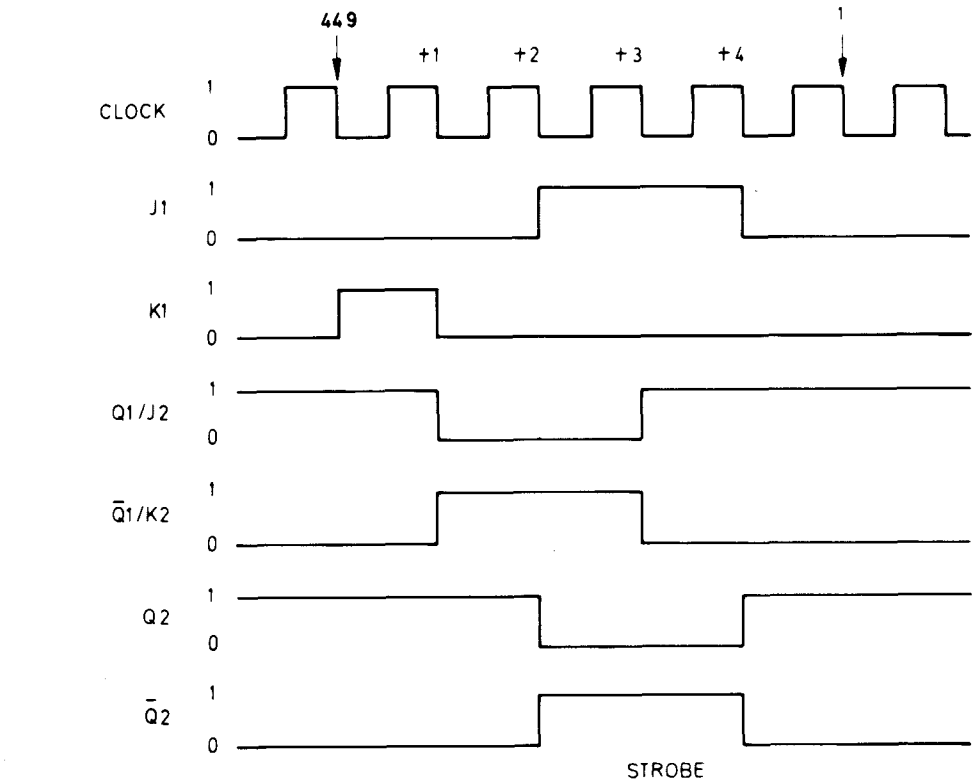
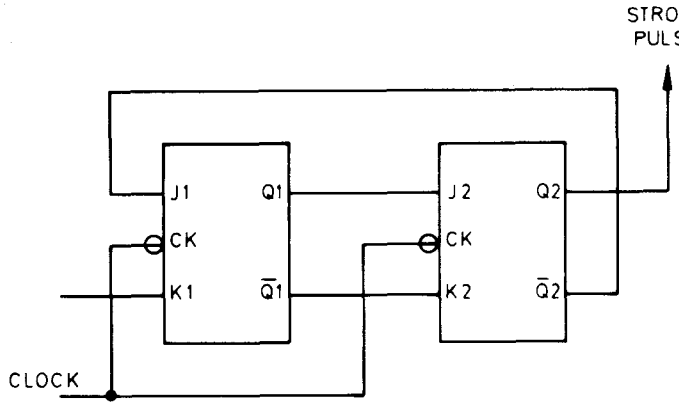
WOH 7049

Timing Diagram Lock Detector

Fig. 2·3





TRUTH TABLE (Each Section)		
tn		tn + 1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\bar{Q}$n

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WOH7049

Timing Diagram: Strobe Pulse Generation Lower Transfer Loop

Fig 2.

EA47432
PM588

RACAL

Layout : Low Frequency Loop Board PM588

Fig.2·5

LOW FREQUENCY LOOP

TRANSFER (LOWER) LOOP

KEY

TRANSISTORS
2N 2369 - TR2, 4, 5, 21 & 23
BFX48 - TR3 & 22
BC109 - TR1, 18, 19 & 20

DIODES
ZC714 - D1
IN4149 - D2
BZY88 C5V6 - D3

10Hz DATA (A B C D) 100Hz DATA (A B C D) 1KHz DATA (A B C D)

PROGRAMMED DIVIDER N1

OUTPUT OF G2 IS ZERO ON COUNT 8996 & 8997 ONLY. K INPUT OF F.F.1. HIGH STARTS STROBE SEQUENCE. THE FIRST NEGATIVE CLOCK AT 8997 TOGGLES F.F.1. THE SECOND NEGATIVE CLOCK AT 8998 TOGGLES F.F.2., THEREFORE TP6 CHANGES FROM `1' TO `0.' THE THIRD CLOCK TOGGLES F.F.1. AT 8999 BY VIRTUE OF `J' BEING AT `1.' THE FOURTH CLOCK TOGGLES F.F.2. AT 9000, RELEASING STROBE, AND THE NUMBER (N1) IS PRODUCT OF 2XYZ WHERE X = 1KHz DATA. Y = 100Hz DATA AND Z = 10Hz DATA. THEREFORE COUNT RUNS FROM 7000 - 6001.

TRANSFER PROGRAMMED DIVIDER

10KHz STEPS 100KHz STEPS OVERANGE & UNDERANGE 1MHz STEPS

THIS VARIABLE DIVIDER IS NOT WITHIN A LOOP. ML14, ML15 & ML19 ARE BCD `UP' COUNTERS. G10 IS THE CODE DETECTOR, AND THE OUTPUT IS LOW ON COUNT 449 ONLY. G11 INVERTS TO PROVIDE A `HIGH' ON THE K INPUT OF F.F.5. THE FIRST NEGATIVE CLOCK (450) RESETS F.F.5. THE SECOND CLOCK (451) RESETS F.F.6. AND THE STROBE LINE GOES `LOW.' THE THIRD CLOCK (452) SETS F.F.5. THE FOURTH CLOCK (453) SETS F.F.6, RELEASING STROBE. THE DIVISION RATIO IS THEREFORE :- (453 - N) WHERE N IS INPUT DATA. NORMALLY THE 1MHz DATA WILL BE 0 AND THE DIVISION RATIO RANGE IS 453 - 354. FREE TUNE RECEIVERS HAVE OVERANGE AND UNDERANGE. IN EACH CASE PIN 36 IS HIGH. PIN 37 IS HIGH FOR UNDERANGE OR LOW FOR OVERANGE. THE TOTAL RANGE IS THEREFORE FROM 474 - 333.

7·000 to 8·000 MHz VOLTAGE CONTROLLED OSCILLATOR

PHASE COMPARATOR P.S.D.

PHASE COMPARATOR OPERATION
IN-LOCK :- UP LINE AND DOWN LINE PULSE TO `1' EQUALLY FOR ABOUT 50nS
OUT-OF-LOCK :- TP7 FREQ. LOW, UP-LINE PULSES TO `1' FOR LONGER. TP7 FREQ. HIGH, DOWN LINE PULSES TO `1' FOR LONGER.

VARACTOR LINE-DRIVER

TYPICAL D.C. VOLTAGES MEASURED ON 20Kᴀ/VOLT-METER. ±20%

TYPICAL A.C. VOLTAGES MEASURED ON HIGH IMPEDANCE OSCILLOSCOPE. ±3dB

PHASE COMPARATOR (P.S.D.)

CIRCUIT CHECKS FOR PULSE LENGTH LESS THAN 150ns
OUTPUT :- 0 = IN-LOCK.
1 = OUT-OF-LOCK

OUT-OF-LOCK DETECTOR

OUT-OF-LOCK DETECTOR
DETECTS PULSES LONGER THAN 150ns
OUTPUT :- 0 = IN-LOCK, 1 = OUT-OF-LOCK

1KHz REFERENCE DIVIDER

TRANSFER LOOP MIXER

OUTPUT FREQUENCY IS DIFFERENCE BETWEEN 1MHz REF. AND 1·013 → 1·020MHz. TRANSFER FREQUENCY. (E.G. 13 - 20KHz)

1·012MHz - 1·021MHz INPUT FROM TRANSFER OSCILLATOR

20KHz L.P. FILTER AND BUFFER

TTL LEVEL CONVERTER

TRANSFER LOOP OUT-OF-LOCK LINE (LOW LEVEL INDICATES LOCK CONDITION).

LOWER LOOP OUT-OF-LOCK LINE (LOW LEVEL INDICATES IN-LOCK CONDITION).

OUTPUT TO TRANSFER OSC. VARACTOR

STROBE LINE

UP LINE

DOWN LINE

1MHz INPUT TTL

1MHz FOR MIXER

1KHz f REF

INPUTS

VARACTOR LINE

INPUT BUFFER

CHAPTER 3

UPPER LOOP BOARD PM589

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CHAPTER 3

UPPER LOOP BOARD PM589

INTRODUCTION

1. This board contains the upper loop, the lower transfer loop VCO and a lock indicator circuit. A circuit diagram of the board is at the end of this chapter fig.3.3.

Lower Transfer Loop VCO

2. This voltage controlled oscillator/shaper stage TR5, TR6, produces a squarewave output signal in the frequency range 1.013 to 1.020 MHz. The tuned circuit comprises L4, capacitor C10, C11, C13, and a varactor diode, D4; positive feedback is applied to the tuned circuit via R14. TR4 and 5.6V Zener diode D3 provide supply voltage stabilization.

3. The oscillator output signal to the mixer stage of the lower transfer loop (PM588) is taken from the emitter of TR5 and is fed to board pin 8 via C12; the varactor line input, from PM588, is applied to D4 via board pin 7 and inductor L5.

4. The lower transfer loop VCO output signal is taken from the collector of TR6 and may be monitored at TP1; it is applied to the lower loop phase comparator via a fixed divider stage ML4, ML6.

Upper Loop VCO/Shaper

5. This VCO/Shaper stage comprises emitter followers, TR19, TR2, inverting NAND gate G1, and a tuned circuit, L1, C2, C3, and varactor diode, D2. Supply voltage stabilization is provided by TR1 and 5.6V Zener diode, D1. The oscillator output signal, in the frequency range 4.6 to 3.6MHz, is applied to the following:-

(1) The upper transfer loop board (PS338) via a NAND gate, G2, a filter R4, L2, C5, a tuned circuit, T1, C1, and board pins 1 and 2.

(2) The programmed divider, N2, of the upper loop via a NAND gate G3.

(3) ML8a (Pin 11), which forms part of the strobe pulse generator for the programmed divider, N2.

Programmed Divider N2. (See Fig. 1.2)

6. The upper loop programmed divider, which has the same division ratio, N2, as that of the lower transfer loop, consists of three presettable decade counters, ML2, ML3, ML5, NAND gate, G4, and a D-type flip-flop, ML8a.

7. The decade counters have strobed parallel - entry capability such that the starting point of a count sequence may be preset. A '1' or a 'O' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at 'O'. The counting operation is performed on the negative-going edge of the input clock pulse.

8. The division ratio of the divider is controlled by the 10kHz and 100kHz digits of the selected operating frequency. The division ratio is given by the expression N2 = 453 minus selected digits, i.e. the division ratio is 453 for a setting of 00 and is 354 from a setting of 99. The operation of the divider is described below.

9. BCD frequency setting information is applied to the data inputs of ML2 (10kHz) and ML3 (100kHz). The data inputs to ML5 are all at 0V (logic 'O') and under this condition ML5 starts counting at zero.

10. To start a counting sequence, assume that a logic 'O' strobe pulse is applied to the strobe (S) input of each decade counter. As described in paragraph 8 this causes the logic level applied to each data input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative-going edge of the clock pulse (the 4. 6 - 3.6MHz VCO output via G3) is applied to the clock 1 input of ML2 and each clock pulse is counted until a count of 451 is reached, i.e. until the Co output from ML5 is at '1', the Ao and Co outputs from ML3 are at '1', and the Ao output from ML2 is at '1'. Thus when a count of 451 is reached, the four input lines to NAND gate G4 are at logic '1', and the output from G4, which is applied to the D input of flip-flop ML8a (pin 12), changes to 'O'. The next clock pulse to arrive at ML8 pin 11 transfers the logic 'O' at ML8 pin 12 to the Q output at pin 9, and this is applied as the strobe pulse to the three decade counters. The four input lines to the NAND gate, G4, are now no longer at logic '1' and the D input of ML8a, changes to '1'. The next clock pulse to arrive at ML8 pin 11 transfers the logic '1' at ML8 pin 12 to the Q output at pin 9, the 'O' strobe pulse is removed, and the counter is ready to start the next count sequence. Thus two clock pulses are used to generate the strobe pulse, making a total count of 453, i.e. 451 + 2.

Range Blanking

11. The range blanking input, at board pin 11 is used to momentarily inhibit the two inputs to the upper loop phase comparator when, during receiver tuning, a 0-to-1 or a 1-to-0 transition of the 10kHz digit occurs. This allows the LF and lower transfer loop outputs to run up or down to the new frequency whilst the 3.6 to 4.6MHz VCO is prevented from changing frequency.

12. The range blanking input line, which is normally at approximately +5V (logic '1'), is connected to the D (pin 12) and clear (pin 13) inputs of a D-type flip-flop, ML9a. This provides the required logic '1' to the D inputs of the phase comparator, ML8b, ML9b. The logic 'O' 25 millisecond range blanking pulse, from the display board, clears ML9a and forces the Q output, at ML9 pin 9, to 'O'. This is applied to the D inputs of the phase comparator and also to the clear input of the strobe pulse generator flip-flop, ML8a. Thus a 25 millisecond strobe pulse, from ML8 pin 9, is applied to the programmed divider, N2, and the output is inhibited.

Fixed Divider

13. The fixed divider consists of two decade counters, ML4, ML6, connected in cascade. The lower transfer VCO output signal is applied to the A input of ML4 and the divide-by-100 output is taken from ML6 pin 11; this is applied as the clock input to the phase comparator (ML9b pin 3) and may be monitored at TP3.

Phase Comparator

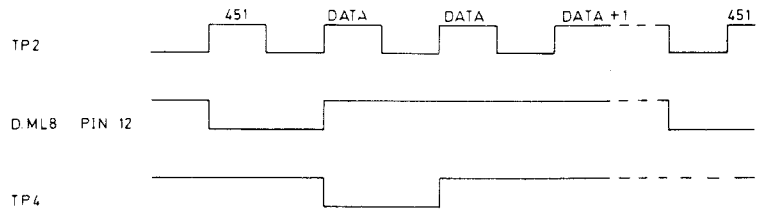
14. The phase comparator consists of two D-type flip-flops, ML8b, ML9b, NAND gate, G5, and a voltage control circuit, TR16, TR17, TR18. It compares the output signal frequency from the programmed divider with the output signal frequency from the fixed divider; any error between these two frequencies is used to develop a d.c. voltage which is applied to the 3.6 to 4.6 MHz VCO to eliminate the error. The action of the circuit is as follows:-

15. The output from the programmed divider, at ML8 pin 8, consists of positive-going pulses which are applied to the clock input of ML8b (pin 3). The output from the fixed divider, at ML6 pin 11, also consists of positive going pulses and these are applied to the clock input of ML9b (pin 3). The D inputs of both ML8b and ML9b are at logic '1' (see paragraph 12). Thus when the positive edge from ML8a pin 8 clocks ML8b, the Q output at pin 5 changes to '1' and the $\overline{Q}$ at pin 6 changes to '0'. Similarly, when the positive edge from ML6 pin 11 clocks ML9b, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output at pin 6 changes to '0'. When both Q outputs are at '1', the output from the NAND gate, G5, changes to '0', clearing both ML8b and ML9b; thus the Q outputs are reset to '0' and the $\overline{Q}$ outputs are reset to '1'.

16. Consider the case where the frequency from the programmed divider is high. This will mean that the positive edge from ML8a pin 8 will occur before the positive edge from ML6 pin 11. The resultant setting and resetting of the flip-flop causes increased conduction of TR18, due to the Q output waveform from ML8b (see Q1 on Timing Diagram Fig. 2.2), as compared with the conduction of TR16; this causes the voltage at the collector of TR18 to become less positive, thereby causing a reduction in the voltage applied to the varactor diode, D2, of the 3.6 to 4.6MHz VCO, and a corresponding reduction in the VCO frequency.

17. If the output frequency from the programmed divider is low, the positive edge from ML8a pin 8 will occur after the positive edge from ML6 pin 11, the Q output waveform from ML9b pin 5 will cause increased conduction of TR16 and the voltage at the collector of TR18 will become more positive. The resultant increase in the voltage applied to the varactor diode, D2, causes a corresponding increase in the VCO frequency thus correcting the error.

18. When the two signals are equal in frequency and phase the two comparator flip-flops are clocked at the same time, the two Q output waveforms are equal and the varactor line voltage remains constant.



Timing Diagram : Strobe Pulse Generation
Upper Loop PM 589 Fig. 3.1

Lock Detector

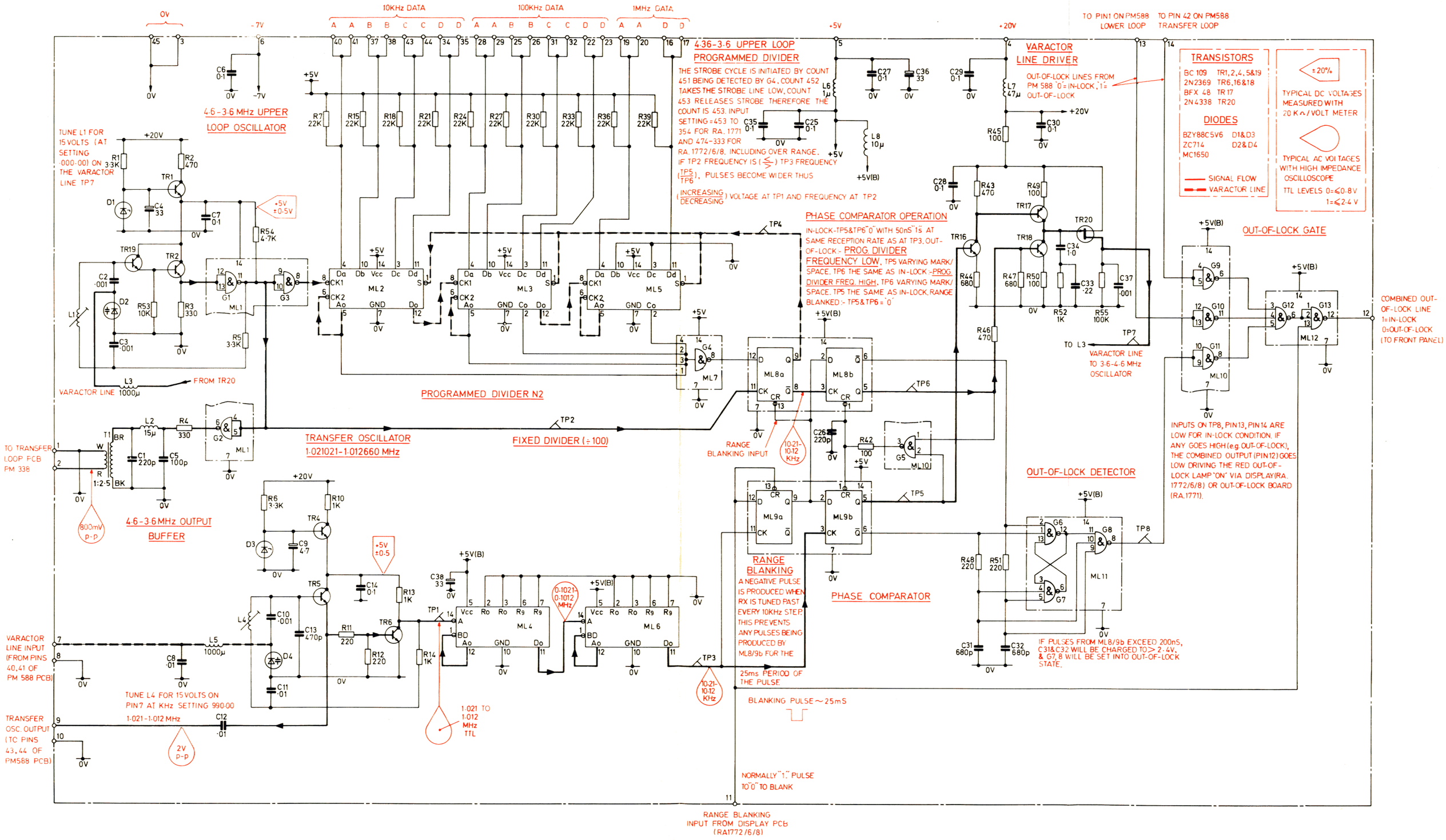
19. This consists of a bistable latch, G6, G7 and an output buffer, G8. It is fed from the $\overline{Q}$ outputs of the phase comparator flip-flops, ML8b, ML9b, and produces a steady '0' in-lock signal, or an alternating '0' - '1' out-of-lock signal, at ML11 pin 8. The action of the circuit, which is identical to that of the LF Loop lock detector (Chapter 2, paragraph 15), is depicted in the Timing Diagram, Chapter 2, Fig.2.3.

Lock Indicator

20. The lock indicator consists of five NAND gates, G9 to G13 inclusive. The lock detector outputs from the LF and lower transfer loops are applied to G10 and G9 via board pins 13 and 14 respectively, whilst the upper loop lock detector output, at ML11 pin 8, is applied to G11. The output from G13 ('1' for in-lock, '0' for out-of-lock) is applied to a diode OR gate and the out-of-lock indicator lamp driver on the display board.

Adjustments

21. Refer to Chapter 23, paragraphs 19 to 21, for details of adjustments to the Upper Loop Board PM589.



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WOH 7049	DC47410/D
D 2 3 4	

Circuit: Upper Loop Board PM589

Upper Loop

Fig.3·3

CHAPTER 4

TRANSFER LOOP BOARD PS338

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CHAPTER 4

TRANSFER LOOP BOARD PS338

INTRODUCTION

1. The transfer loop board contains the upper transfer loop (with the exception of the upper transfer loop oscillator which is located on the HF loop board PS337), programmed divider N3 and lock indicator circuits. This board, together with HF loop board, generates the 35.4 to 65.4 MHz local oscillator injection frequency for the first mixer. A circuit diagram of the board is given at the end of the chapter fig. 4.3.

2. The 4.6 to 3.6MHz output signal from upper loop, at board pin 17, is coupled by C3 to a shaper stage, TR4, TR5. The squarewave output is inverted by ML4a and is then applied to a programmed divider consisting of two presettable decade counters ML1, ML2, and inverter, ML4b, a six-input NAND gate, ML5 and a D-type flip-flop, ML6.

Programmed Divider N3 (See Fig. 1.2)

3. The two decade counters, ML1, ML2, have strobed parallel-entry capability so that the starting point of a count sequence may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

4. The division ratio of the programmed divider, which is controlled by the 10MHz and MHz lines, is given by the expression N3 = 40+ selected MHz digits, i.e. when 00MHz is selected, the division ratio is 40, and when 29 MHz is selected, the division ratio is 69. The operation of the divider is described below.

5. Information from the memory board is applied to the decoding board where it is converted into a BCD nines complement code (see Table 1). The nines complement coded outputs are applied to the data inputs of the two decade counters 'units' to ML1 and 'tens' to ML2, and control the starting point of a count sequence.

6. To start the counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) inputs of both ML1 and ML2 (at pin 1). As described in paragraph 3 this causes the logic level applied to each input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative going edge of the clock pulse (from the shaper stage, TR4, TR5 and the inverter ML4a) is now applied to the clock 1 input of ML1 at pin 8. Each clock pulse is now counted until a count of 37 is reached, i.e. until the Ao, Bo and Co outputs from ML1 and the Ao and Bo outputs from ML2 are all at logic '1'. (The C output from ML2 is applied to an inverter, ML4b, to inhibit binary 7).

7. When a count of 37 is reached, the input lines to the NAND gate, ML5, are all at logic '1' and the '0' output, at ML5 pin 8, is applied to the D input of flip-flop ML6. The next clock pulse, which is applied to pin 3 of ML6, transfers the '0' at ML6 pin 2 to the Q output, at ML6 pin 5, and this is applied as the next strobe pulse to the two decade counters, ML1 and ML2, ready for the next count. The output from ML5 changes to logic '1' and the next clock pulse applied to ML6 causes the Q output to change to logic '1' ; this output is applied to the phase comparator, ML8 .

8. Table 2 shows the operation of the divider for various settings of the MHz digits.

Mixer

9. ML3 is an integrated circuit mixer; the 1MHz reference frequency signal, shaped by TR1, TR2, is applied to pin 8 and the 885-948kHz transfer loop oscillator output signal, from the HF loop board, buffered by TR3, is applied to pin 4 via a low-pass filter, L9, L10, C29 to C32. The difference frequency output from the mixer, 115kHz to 52kHz, is coupled to a low-pass filter, L11, L12, C36, C38, C39, and is then applied to a shaper stage, TR6. The squarewave output from TR6 is applied to the phase comparator, ML8 via a buffer, ML7a.

Phase Comparator

10. The phase comparator consists of a dual D-type flip-flop, ML8, a two-input NAND gate ML7b and a voltage control circuit, TR7, TR8, TR9, TR10. It compares the output signal frequency from the programmed divider with the output signal frequency from the mixer; any error between these two frequencies is used to develop a d.c. voltage, which is applied to the transfer loop oscillator (on the HF loop board) to eliminate the error. The action of the circuit is as follows.

11. The output from the programmed divider, at ML6 pin 5, consists of negative-going pulses; these are applied to the clock input of ML8b. The output from the mixer (via the low-pass filter, shaper and buffer), at ML7a pin 8, is applied to the clock input of ML8a. The D inputs to both ML8a and ML8b are taken to the +5V rail (logic '1'). Thus when the positive edge from ML6 pin 5 clocks ML8b, the Q2 output at pin 5 changes to '1' and the $\overline{Q}2$ output changes to '0'. Similarly, when the positive edge from ML7a pin 8 clocks ML8a, the Q1 output changes to '1' and the $\overline{Q}1$ output changes to '0'. When both Q outputs are at '1', the output from the NAND gate, ML7b, changes to '0' clearing both ML8 flip-flops via R38 and thus resetting the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

12. Consider the case where the frequency of the mixer output signal is high. This will mean that the positive edge from ML7a will occur before the edge from ML6. The resultant setting and resetting of the flip-flops causes increased conduction of TR7, due to the $\overline{Q}1$ output from ML8a (see timing diagram, Fig. 2) as compared with the conduction of TR10; this causes the voltage of the collector of TR9 to become more positive, thereby increasing the varactor line voltage applied to the transfer loop oscillator on the HF loop board. This increases the oscillator frequency, but since this frequency is subtracted from the reference 1MHz in the mixer, ML3, the output frequency from the mixer is reduced.

13. If the mixer output signal frequency is low, the pulse from ML7a will occur after the pulse from ML6, the $\bar{Q}$2 output waveform from ML8b will cause increased conduction of TR10 and the voltage at the collector of TR9 will become less positive. Thus the reduced varactor line voltage applied to the transfer loop oscillator causes a reduction in oscillator frequency and a corresponding increase in the mixer output signal frequency.

14. When the two frequencies are in phase, the two flip-flops of ML8 are clocked at the same time, the $\bar{Q}$1 output waveform is equal to the $\bar{Q}$2 output waveform and the varactor line voltage remains constant.

Lock Indicator and Fast Lock Circuit

15. This circuit comprises two monostables, ML9, ML10, a dual D-type flip-flop, ML11, and NAND gates ML4c, ML4d. Its purpose is to augment the conduction of TR7 or TR10 in the out-of-lock condition and so obtain a faster return to the locked condition; it also provides a lock indication output signal. The action of the circuit is as follows.

16. The Q output from the phase comparator flip-flop, ML8a, is applied to the B input (Schmitt trigger) of the monostable, ML9, and also to the D and clear inputs of a D-type flip-flop, ML11a. Similarly, the Q output from ML8b is applied to the B input of the monostable, ML10, and also to the D and clear inputs of a second D-type flip-flop, ML11b. The two monostables, triggered when positive going signals are applied to the respective B inputs, each produce a negative going output pulse ($\bar{Q}$), of approximately 1.5μs duration.

17. From the timing diagram, Fig. 4.1 it will be seen that for the in-lock condition, the $\bar{Q}$ outputs from the two flip-flops, ML11a, ML11b, are both at logic '1': these these two signals do not, however, affect the conduction of the voltage control transistors, TR7, TR10, due to the presence of the two diodes, D2, D3. The logic '0' output from ML4c is inverted by ML4d to produce a logic '1' in-lock signal at board pin 6.

18. If the output frequency from the mixer is low, as depicted by the out-of-lock waveform of Fig. 4.1, the negative excursion of the $\bar{Q}$ output from ML11b will be applied to TR10, via diode D3. The conduction of TR10 will, therefore, be rapidly increased to bring about a fast return to the in-lock condition. The $\bar{Q}$ output waveform from ML11b is also applied to ML4c to produce an alternating '0' - '1' out-of-lock signal at board pin 6.

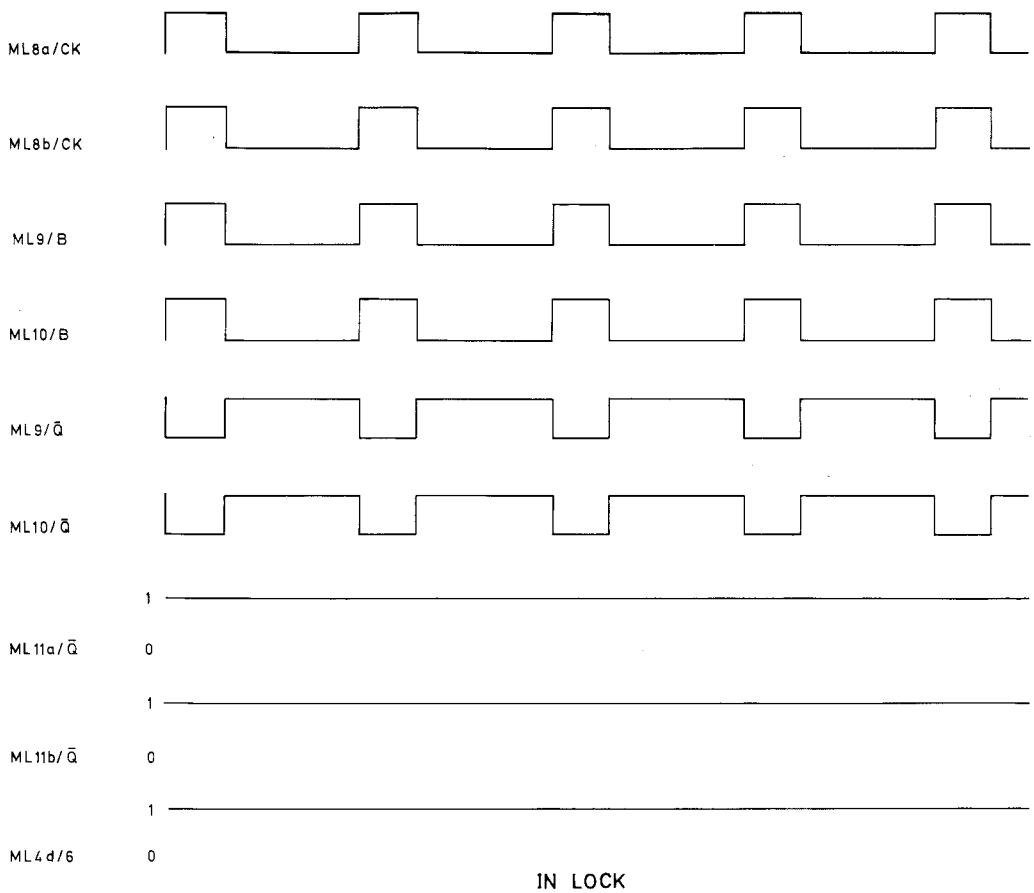
19. Should the out-of-lock condition be due to a high mixer output frequency the $\bar{Q}$ output from ML11a will cause a rapid return to the in-lock condition by increasing the conduction of TR7; the $\bar{Q}$ output from ML11a is also applied to ML4c to produce an alternating '0' - '1' out-of-lock signal at board pin 6, as before.

Decimal	BCD				Nines Complement				Decimal
	D	C	B	A	D9	C9	B9	A9	
0	0	0	0	0	1	0	0	1	9
1	0	0	0	1	1	0	0	0	8
2	0	0	1	0	0	1	1	1	7
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	0	0	4
6	0	1	1	0	0	0	1	1	3
7	0	1	1	1	0	0	1	0	2
8	1	0	0	0	0	0	0	1	1
9	1	0	0	1	0	0	0	0	0

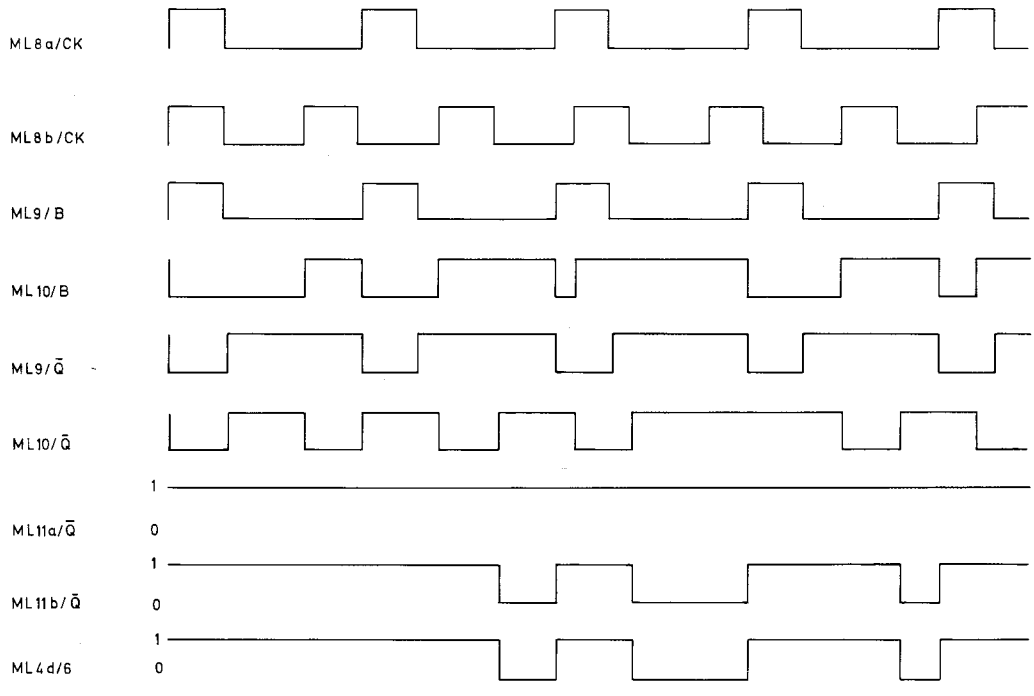
Table 1 : Code Conversion

'MHz' setting	Nines Complement	Clock Pulses				
		Count up to 100	Fixed Count	Strobe Pulse		Total Division ratio
				Begin	End	
00	99	1	37	1	1	40
07	92	8	37	1	1	47
14	85	15	37	1	1	54
21	78	22	37	1	1	61
29	70	30	37	1	1	69

Table 2: Programmed Divider Operation (PS338)



IN LOCK

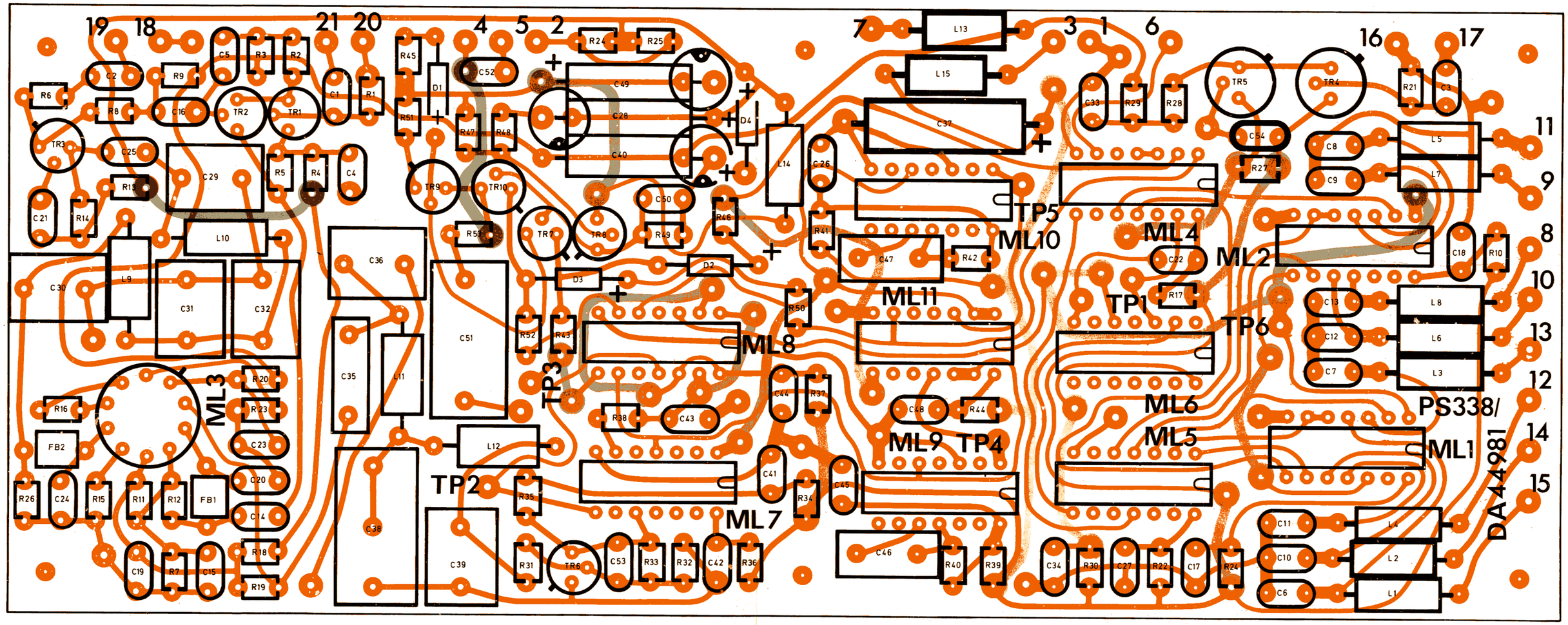


OUT OF LOCK

RACAL
WOH7049

Timing Diagram : Fast Lock and Indicator Upper Transfer Loop PS338

Fig 4



ACAL

H 7049	DA44981
4 5	

WOH 7049	DD44979 SHT 2
2 3 4 5 6	

WOH 7049	DD44979 SHT3
2 3 4 5	

Layout : Transfer Loop Board PS338

Fig 4

LINEAR MIXER

OUTPUT IS DIFFERENCE BETWEEN TRANSFER OSC. FREQUENCY AND 1MHz STANDARD. FOR CORRECT OPERATION, SIGNAL INPUT SHOULD BE ⩾300mV p-p AND CARRIER INPUT 1V p-p (approx). R16 SETS THE GAIN. OUTPUT LEVEL SHOULD BE >0·2Vp-p FOR OUTPUT AT TP2.

LOW PASS FILTER AND TTL LEVEL CONVERTER

ONLY FREQUENCIES BELOW 115KHz ARE PASSED. IF HIGHER THAN THIS, NO OUTPUT WILL BE OBTAINED ON TP2. (ALWAYS CHECK THE FREQUENCY BEFORE REPLACING ANY COMPONENT). G4 IS A SCHMITT TRIGGER AND REQUIRES AN INPUT OF <+0·8V TO >+1·6V FOR CORRECT OPERATION.

PHASE COMPARATOR

VARACTOR LINE-DRIVER

EXTRA TRANSISTOR TR8 IS AN EMITTER-FOLLOWER TO STABILISE REFERENCE VOLTAGE ON TR7 AND TR10 BASES. CIRCUIT FUNCTION IS UNALTERED.

VARACTOR LINE TO PINS 17,18 ON HF LOOP PCB

INPUT AMPLIFIER

OUTPUT VOLTAGE ⩾300mV pk-pk

1MHz REFERENCE INPUT

INPUT AMPLIFIER

TRANSFER OSCILLATOR FREQUENCY 7·885-9·48 MHz

OUTPUT VOLTAGE 1Vp-p (approx) FOR CARRIER INPUT OF MIXER (CHECK THAT FREQUENCY IS CORRECT BEFORE PROCEEDING).

LOW PASS FILTER

SYNTHESIZER OUTPUT AMPLIFIER

1·6-4·6MHz SYNTHESIZER e.g. PM589

TTL

FAST-LOCK MONOSTABLE

STROBE LINE

OUT-OF-LOCK INDICATOR (HIGH FOR IN-LOCK CONDITION)

WHEN LOOP IS OUT-OF-LOCK, THESE CIRCUITS PRODUCE EXTRA PULSES TO FORCE THE LOOP INTO LOCK MORE QUICKLY.

± 2% TYPICAL D.C. VOLTAGES MEASURED ON 20KΩ/VOLT-METER

± 3dB TYPICAL A.C. VOLTAGE MEASURED ON HIGH IMPEDANCE OSCILLOSCOPE

TRANSISTORS

2N2369 - TR1, 2, 3, 4, 5, 7 & 10

BC109 - TR6 & 8

BFX 48 - TR9

DIODES

IN4149 - D1, 2 & 3

BZY88 C12V - D4

INDICATES SIGNAL FLOW

PROGRAMMED DIVIDER OPERATION

WHEN MHz IS SET TO 00, COUNTER (ML1, ML2) COUNTS UP TO 37. WHEN AN OUTPUT OF 37 IS REACHED, ML5/8 WILL GO TO '0'. NEXT CLOCK PULSE (38) CLOCKS THIS '0' INTO ML6. LOW ON ML6/5 CAUSES DATA TO BE ENTERED INTO ML1,2. AS DATA IS 9'S COMPLEMENT, COUNTER IS SET TO 99. AS INPUT TO ML5 IS NO LONGER 37, OUTPUT GOES BACK TO '1'. NEXT CLOCK (39) THEREFORE RESETS ML6/5 TO '1', RELEASING STROBE LINE. COUNTER IS NOW READY TO COUNT AGAIN. NEXT CLOCK (0) SETS COUNTER TO ZERO AND CYCLE IS REPEATED, E.G. ON 0MHz, CYCLE REPEATS EVERY 40 CLOCK PULSES (0-39 INCLUSIVE). TOTAL COUNT IS 40+N WHEN 'N' IS THE MHz SETTING.

MHz READING TO DATA CONVERSION

	UNITS OF MHz DATA				TENS OF MHz DATA			
PIN	12	13	14	15	8	9	10	11
0	1	0	0	1	1	0	0	1
1	1	0	0	0	1	0	0	0
2	0	1	1	1	0	1	1	1
3	0	1	1	0				
4	0	1	0	1				
5	0	1	0	0				
6	0	0	1	1				
7	0	0	1	0				
8	0	0	0	1				
9	0	0	0	0				

FAST-LOCK OPERATION

IN-LOCK
PIN 5, ML9 AND 10
PIN 1, ML9 AND 10

OUT-OF-LOCK
PIN 5, ML9 AND 10
PIN 1, ML9 AND 10

CORRECTION WAVEFORM
PIN 6 OR 8, ML 11

PROGRAMMED DIVIDER

DATA

CAL

7049	DC 44981
2 3 4 5 6	

Circuit: Upper Transfer Loop Board PS338

Transfer Loop

Fig. 4·3

CHAPTER 5

HIGH FREQUENCY LOOP BOARD PS337

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CHAPTER 5

HIGH FREQUENCY LOOP BOARD PS337

INTRODUCTION

1. This board provides the 35.4 - 65.4 MHz local oscillator frequency for the first mixer; it also contains the 885-948 kHz upper transfer loop oscillator. A circuit diagram of the board is given at the end of this chapter fig. 5.3.

Upper Transfer Loop Oscillator

2. Transistors TR17 and TR20, together with associated components, form a variable frequency LC oscillator, tunable by the voltage applied to the varactor diode D19. The varactor line voltage at pin 18, from the transfer loop board, is applied to D19 via a filter, C66, C67, R62, C69 and L19.

3. The oscillator output signal, at the collector of TR20, is applied to the clock input of a divide-by-two stage, ML12; the output from ML12, at pin 5, is applied as one signal input to the phase comparator, ML7.

4. A second output from the oscillator is coupled by C76 to a buffer amplifier, TR21, the output from which is applied to the mixer on the transfer loop board, via C81 and pin 13.

HF Loop Oscillators

5. Three separate, switched oscillators are provided to cover the frequency range 35.40000 to 65.39999 MHz. Oscillator selection is controlled by the memory board of the receiver· an earth (OV) is connected to the appropriate switching transistor, TR1, TR2 or TR3 (via pins 28, 27 or 26 respectively) and the supply voltage to the selected oscillator is switched on. The oscillator selected is in accordance with the table below.

OSCILLATOR	FREQUENCY RANGE (MHz)	MHz DIGITS SETTING
1	35.40000 to 43.9999	0 to 7
2	43.40000 to 53.9999	8 to 17
3	53.40000 to 65.39999	18 to 29

6. The three oscillators are similar in construction and operation. Frequency is controlled by the voltage applied to a pair of varactor diodes: this voltage, derived by the phase comparator, is applied via a common line and an inductor (L21, L22, L23) to each oscillator. The gain of the selected oscillator stage is automatically controlled by peak-detecting diodes D13, D14, and the current source transistor, TR13· the automatic gain control (AGC) level is preset by R38.

7. The output from the selected oscillator transistor and associated buffer (TR7, TR8 or TR9) is amplified by TR10 and applied to:-

(a) The AGC stage, TR13, via C26.

(b) A programmed divider, via C24.

(c) A pair of output buffer amplifier stages, TR14, TR15, via C36.

8. Details of the three oscillator stages are tabulated below.

OSCILLATOR NUMBER	VOLTAGE SWITCH	OSCILLATOR CIRCUIT	OUTPUT BUFFER
1	TR3	TR6, D8, D9, L6	TR9
2	TR2	TR5, D6, D7, L5	TR8
3	TR1	TR4, D4, D5, L4	TR7

LO Output Buffer Stages

9. The output buffer amplifier stages, TR14, TR15, are conventional and are of similar design; stage gain is preset by potentiometers R44 (for TR14) and R50 (for TR15). The amplified outputs are fed to a diode switch, D16, D17, D18, which is controlled by the rear panel LO INT/EXT switch. When this switch is set to EXT, an earth (OV) is connected to board pin 25; this causes diodes D16 and D17 to become reversed biassed, and diode D18 to become forward biassed. The outputs from the two buffer stages are inhibited and an external LO signal (from a second receiver), connected to the rear panel LO IN/OUT socket, is routed to board pin 24 and thence via C57, D18, C58 and pin 22 to the first mixer board.

10. When the LO INT/EXT switch is set to INT, the earth is removed from board pin 25; diodes D16, D17 are now forward biassed and diode D18 is reverse biassed. The output signal from TR14 is routed to the first mixer board via C44, D16, C58 and board

pin 22; the output signal from TR15 is routed to the rear panel LO IN/OUT socket via C54, D17, C57 and board pin 24.

Programmed Divider N3 (See Fig. 1.2)

11. The programmed divider, which is set to the same division ratio, N3, as that of the upper transfer loop board programmed divider, consists of a shaper stage, TR11, TR12, a divide-by-two stage, ML2a, two presettable decade counters, ML3, ML5, with associated gates, and three J-K flip-flops, ML2b, ML9a, ML9b.

12. The two decade counters, ML3, ML5, have strobed parallel-entry capability such that the starting point of a count sequence may be preset. A '1' or '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

13. The division ratio of the programmed divider, which is controlled by the memory board, is given by the expression N3 = 40+ selected MHz digits, i.e. when 00MHz is selected, the division ratio is 40, and when 29 MHz is selected, the division ratio is 69. The operation of the divider is described below.

14. Frequency setting information from the memory board is applied to the logic board where it is converted into a nines complement code (see Table 1). The nines complement coded outputs from the logic board are applied to the data inputs of the two decade counters, 'units' to ML3 and 'tens' to ML5, and preset the starting point of a count sequence.

15. To start the counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) inputs of both ML3 and ML5 (at pin 1). As described in paragraph 12, this causes the logic level applied to each input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative going edge of the clock pulse (from the shaper stage, TR11, TR12, and the divide-by-two ML2a) is now applied to the clock 1 input of ML3 at pin 8. Each clock pulse is now counted until a count of 35 is reached, i.e. until the Ao and Co outputs from ML3 and the Ao and Bo outputs from ML5 are all at logic '1'. (The C output from ML5 is applied to an inverter, ML6d, to inhibit binary 7).

16. When a count of 35 is reached, the input lines to the NAND gate, ML4b, are all at logic '1' and the '1' output, at ML4 pin 6, is applied to the J input of flip-flop ML2b. Both Q outputs from ML2b are fed to the dual J-K flip-flop, ML9 (Q to J, $\overline{Q}$ to K), and the Q output of ML9b is fed back to the K input of ML2b. The effect of this circuit is to produce a logic '0' strobe pulse (ML2b$\overline{Q}$) sufficient in width for the two decade counters, ML3 and ML5. As can be seen from the timing diagram, Fig. 2.6, the strobe pulse is extended to the negative-going edge of the 39th clock pulse, at which point the counting sequence is repeated.

17. Table 1 shows the operation of the programmed divider for various settings of the MHz digits.

Phase Comparator

18. The phase comparator comprises a dual D-type flip-flop, ML7, a two-input NAND gate, ML6 (pins 4, 5 and 6), and a voltage control circuit TR16, TR18, TR19. It compares the output signal frequency from the transfer loop oscillator (after division by two in ML12) with the output signal frequency from the programmed divider: any error between these two frequencies is used to develop a d.c. voltage which is applied to the selected HF loop oscillator to eliminate the error. The action of the circuit, which is similar to that of the transfer loop board (PS338), is as follows.

'MHz'	Nines Complement	Clock Pulses			
		Count Up to 100	Fixed Count	Strobe Pulse Generation	Total Division Ratio
00	99	1	35	4	40
07	92	8	35	4	47
14	85	15	35	4	54
21	78	22	35	4	61
29	70	30	35	4	69

Table 1: Programmed Divider Operation (PS 337)

19. The programmed divider output, which is taken from ML2b pin 9, consists of positive-going pulses: these are applied to the clock input of ML7a. The output from the divide-by-two stage, ML12, at pin 5, is applied to the clock input of ML7b. The D inputs of both ML7a and ML7b are taken to the +5V rail (logic '1'). Thus when the positive edge from ML2b clocks ML7a, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output changes to '0'. Similarly, when the positive edge from ML12 pin 5 clocks ML7b, the Q output changes to '1' and the $\overline{Q}$ output changes to '0'. When both Q outputs are at '1', the output from the NAND gate, ML6, changes to '0', clearing both ML7 flip-flops via R61 and thus resetting the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

20. Consider the case where the frequency of the selected HF loop oscillator output signal (which is applied to the programmed divider) is high. This will mean that the positive edge from ML2b will occur before the edge from ML12. The resultant setting and resetting of the flip-flops causes increased conduction of TR19, due to the $\overline{Q}$ output

from ML7a (see timing diagram, Fig. 2.2), as compared with the conduction of TR16. This causes a reduction in the varactor line voltage, taken from the collector of TR18, and thus a reduction in the frequency of the selected HF loop oscillator output signal.

21. If the frequency of the selected HF loop oscillator output signal is low, the edge from ML2b will occur after the edge from ML12· the $\bar{Q}$ output from ML7b will cause increased conduction of TR16, the voltage at the collector of TR18 will become more positive and this will cause an increase in the frequency of the selected HF loop oscillator output signal.

22. When the two frequencies are equal, the two flip-flops of ML7 are clocked at the same time, the $\bar{Q}$ output waveform from ML7a is equal to that from ML7b and the varactor line voltage remains constant.

Lock Indicator and Fast Lock Circuit

23. The circuit comprises monostable ML11, D-type flip-flop ML12a and NAND gates ML6a and ML6b. Its function is to augment the conduct on of TR16 or TR19 in the out-of lock condition and so obtain a faster return to lock; an out-of-lock indication signal is also produced. The action of the circuit is as follows.

24. The $\bar{Q}$ outputs of the phase comparator flip-flops are applied to the A inputs of ML1 A negative edge on one of these inputs produces a negative-going pulse (of approximately 1.5μs) at the inputs of ML6a and ML6b. The positive-going pulses at the Q outputs of ML7a and ML7b are applied to the other inputs of the NAND gates after a delay of about 200μs (determined by R60, C94 and R36, C92).

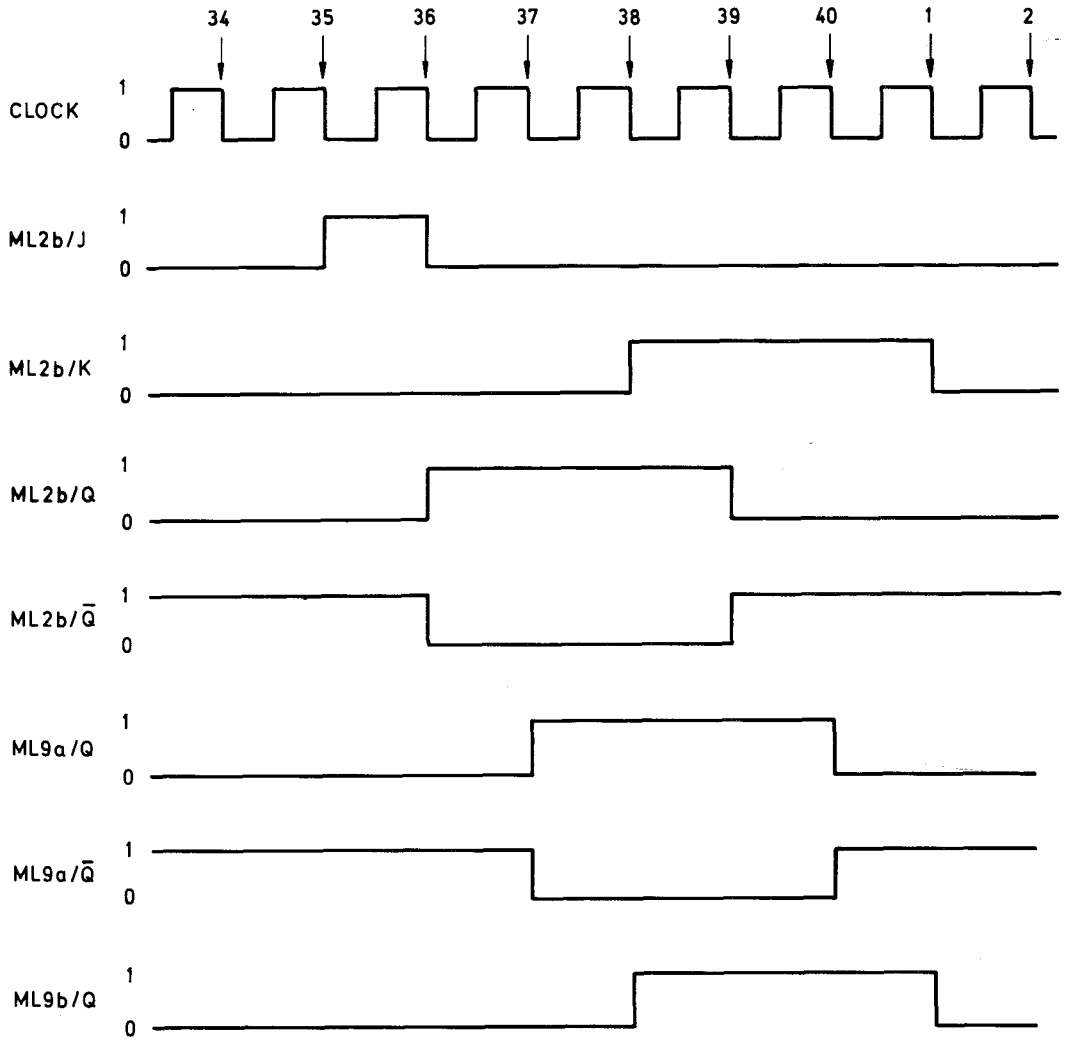
25. When the circuit is in lock, the Q outputs (approximately 50μs pulses) return to zero before the 1.5μs pulse has ended. Thus the outputs of the NAND gates remain at '1' and a 0 is clocked into ML12a, producing a '1' in-lock signal at $\bar{Q}$.

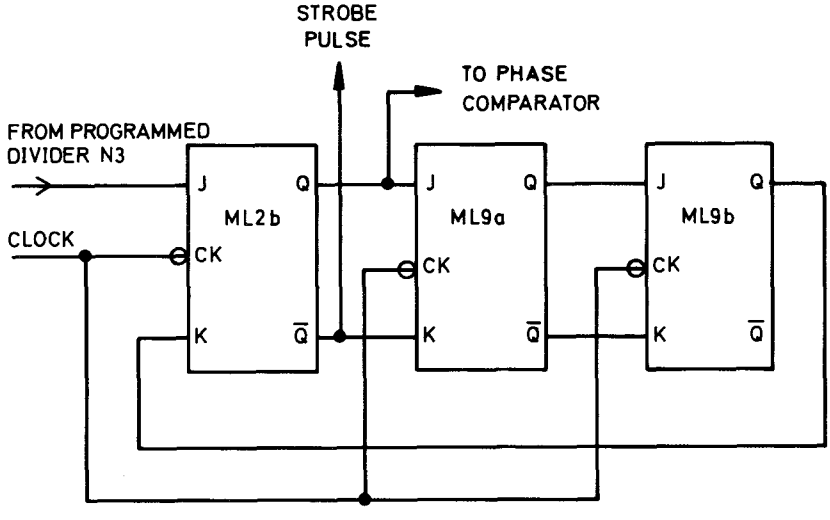
26. If the frequency of the HF loop oscillator is high the longer pulses at ML7a pin 5, if they extend beyond the 1.5μs pulses, cause ML6a to produce a '0'. The conduction at TR19 is thus increased, bringing about a rapid return to lock. The '0' on the PR input of ML12a causes the $\bar{Q}$ output to produce a '0' out-of-lock indication.

27. Similarly, if the HF loop oscillator is low in frequency the longer pulses at ML7b, if they extend beyond the 1.5μs pulses, cause ML6b to produce a '0' increasing the conduction of TR16. The '1' at the D input of ML12a is clocked in, producing a '0' out-of-lock indication at the $\bar{Q}$ output.

Adjustments

28. Refer to Chapter 23, paragraphs 25 to 27, for details of adjustments to the HF Loop Board PS337.



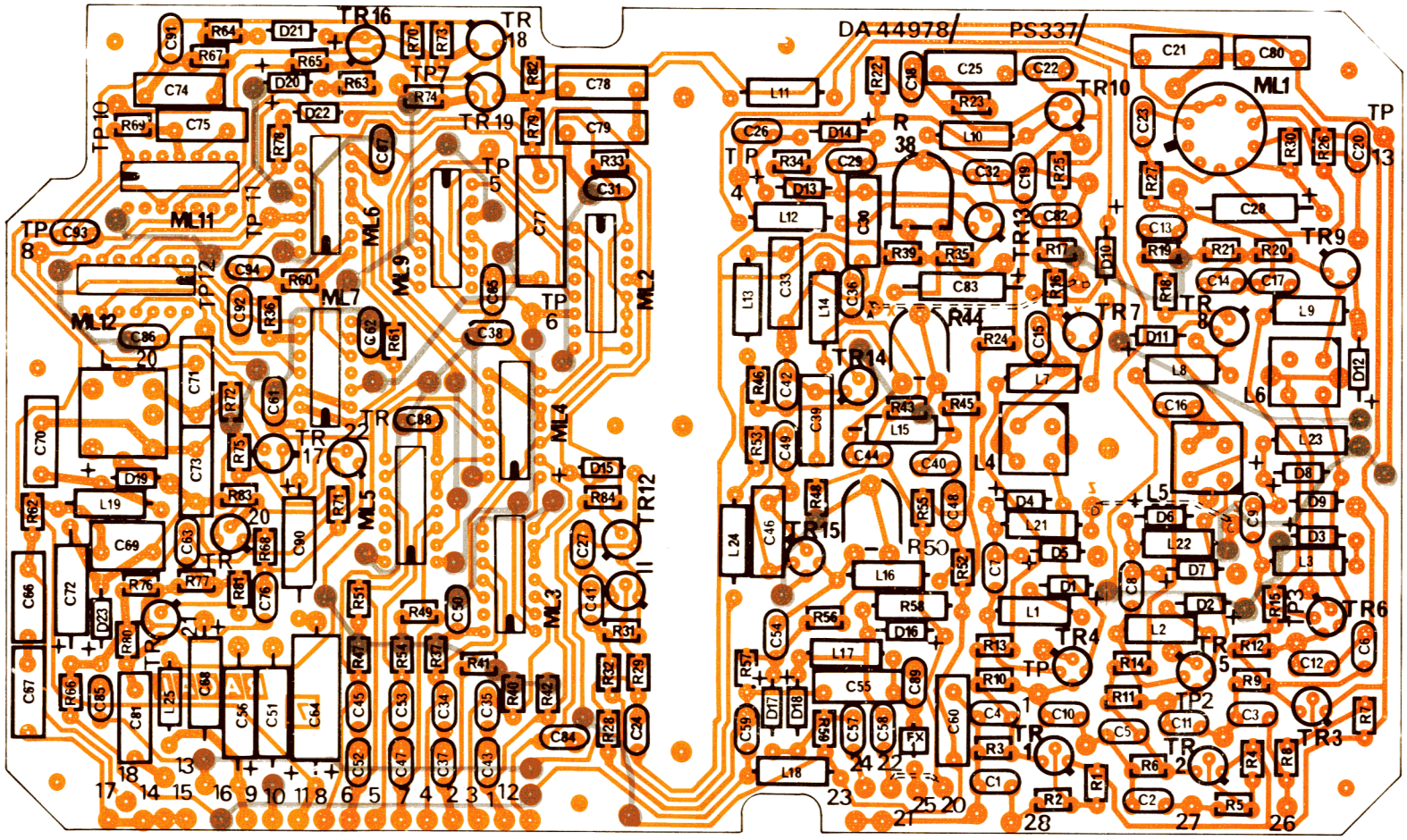


TRUTH TABLE (Each Section)		
tn		tn+1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\bar{Q}$n

RACAL

WOH7049

Timing Diagram: Strobe Pulse Generation HF Loop (PS337) Fig. 5.



RACAL

WOH 7049	DA44978 SHT 1	5·2	1
WOH 7049	DD44976 SHT. 2	5·2	2
WOH 7049	DD44976 SHT 3	5·2	3

Layout : HF Loop Board PS337

Fig. 5·2

TR1 SWITCHES OSCILLATOR ON/OFF. EARTHING INPUT MAKES TR1 CONDUCT AND APPLY SUPPLY TO TR4. D10 CONDUCTS AS CURRENT FLOWS (R13 – D10 – R23), OTHERWISE D10 IS OFF.

0V WHEN NOT SELECTED

0 – 7MHz RANGE OSCILLATOR

REFER TO CHAP. 5 FOR OSCILLATOR ADJUSTMENT PROCEDURES

FROM LOGIC PCB (EARTH TO SELECT OSCILLATOR) 28

SUPPLY

R1 100K, R2 47K, R3 22K, R4 ·001, R10 220, R13 680, C1 ·001, C10 ·001, C15 ·001, L7 4·7µ, TR1, TR4, TP1, D4, D5, D10, C7 100p, L4, TR7, R16 220, R17 680, C82 ·001, L1 15µ, L21 15µ, D1

+14V ± 1V

0V

– 0·7V

35·4 – 42·399MHz

– 0·7V

THIS OSC. SHOWN OFF. (VOLTAGES APPLY TO OSC'S WHICH ARE OFF).

8 – 17MHz RANGE OSCILLATOR

FROM LOGIC PCB (EARTH TO SELECT OSCILLATOR) 27

SUPPLY

R4 100K, R5 47K, R6 22K, R11 220, C2 ·001, C5 ·001, C11 ·001, R14 680, C16 ·001, L8 4·7µ, TR2, TR5, TP2, D6, D7, C8 100p, L5, TR8, D11, R18 220, R19 680, C13 ·001, L2 15µ, L22 15µ, D2

75mV pk pk

42·4 – 52·999MHz

THIS OSCILLATOR SHOWN SELECTED. (VOLTAGES APPLY TO WHICHEVER OSC. IS SELECTED)

18 – 29MHz RANGE OSCILLATOR

FROM LOGIC PCB (EARTH TO SELECT OSCILLATOR) 26

SUPPLY

0V

R7 100K, R8 47K, R9 22K, R12 220, C3 ·001, C6 ·001, C12 ·001, R15 680, C17 ·001, L9 4·7µ, TR3, TR6, TP3, D8, D9, C9 100p, L6, TR9, D12, R20 220, R21 680, C14 ·001, L3 15µ, L23 15µ, D3

2V pk pk

75mV pk pk

52·4 – 65·399MHz

– 0·7V

AGC

VARACTOR LINE FROM JUNCTION R82 & C80

FROM SHEET 2

POWER SUPPLY

PROVIDES A HIGHLY STABILISED SUPPLY VOLTAGE TO OSCILLATORS

+20V, L11 4·7µ, C21 0·1, 14V ± 1V, 0V, VC, +V, VO, REF, ML1, INV, NON INV, COMP, R26 10K, R27 10K, R30 10K, C20 ·01, C23 100p, C28 6·8

+12V 10, +20V 11, –7V 16

L18 4·7µ, C59 ·001, C51 6·8µ, C60 0·1, C64 6·8µ, C68 6·8µ, C85 0·01, L24 4·7µ

A +12V, +20V, B –7V, –7V

SQUARING AMPLIFIER AND HIGH SPEED DIVIDE – BY – 2

T.T.L.

+5V, C27 ·001, C31 0·33, R36 220, R33 330, C24 ·001, R29 560, TR11, TR12, R28 220, R31 150, D15, C41 ·001, R32 100, –7V, ML2a

T.T.L. LEVEL OUTPUT. FREQUENCY = HALF OF L.O. FREQUENCY (TO SHEET 2, ML3 PIN 8)

BUFFER AMPLIFIER

+12V, R24 390, C19 ·001, L10 4·7µ, R22 1K, C18 ·001, TR10, R23 220, R25 470, C22 ·001, C25 0·1, TP4

650mV TO 1·2V rms

+2·0V

2·4V

AGC DETECTOR

ADJUSTMENT: SET MHz SWITCH TO 01·000. ADJUST R38 FOR 1V RMS AT TP4. CHECK THAT LEVEL IS WITHIN LIMITS AT ALL MHz SETTINGS STATED.

C26 ·001, D13, D14, C29 100p, C30 0·1, TR13, R34 100K, L12 1m, C32 ·001, R38 10K, C83 33, C36 ·001, R35 220, R39 1·5K, C33 0·1, L13 1m

SIGNAL IS RECTIFIED BY D13/14 WHICH SETS THE COLLECTOR CURRENT OF TR13. QUIESCENT CURRENT IS SET BY R38.

OUTPUT AMPLIFIERS

–12V (A), R45 390, R52 390, C40 ·001, C48 ·001, L15 4·7µ, L16 4·7µ, R44 1K, R50 1K, C44 ·001, TR14, TR15, R43 680, R48 680, C39 0·1, C42 ·001, R46 470, C46 0·1, C49 ·001, R53 470, –7V(B), L14 4·7µ

ADJUSTMENT: SET MHz SWITCH TO 29·000. (1) ADJUST R50 FOR 220mV IN 50Ω AT PIN 24. (2) ADJUST R44 FOR 320mV RMS AT PIN 22.

NORMAL OPERATION:– PIN 25 NOT EARTHED. D16 & D17 CONDUCT AND SIGNAL IS APPLIED TO 1st MIXER AND L.O. SOCKET AS SHOWN BY FULL BLACK LINE.

SLAVE OPERATION:– PIN 25 EARTHED BY BACK PANEL SWITCH (IN 'EXT.' POSITION). D16 & D17 CUT OFF. D18 CONDUCTS. EXTERNAL OSCILLATOR SIGNAL FROM L.O. SOCKET TO 1st MIXER AS SHOWN BY DASHED LINE (– – – –).

OUTPUT SWITCH

8·2V, 7·5V, (A), +12V, LK1 20, R55 1K, R58 220, R59 560, D16, D18, D17, C58 ·001, C54 ·001, C57 ·001, L17 15µ, R56 220, R57 220, C55 0·1, C89 ·001, 3·3V, 4·0V, FB1

320mV RMS

200mV RMS

22 OUTPUT TO FIRST MIXER PCB

23 0V

24 L.O. IN/OUT SOCKET

25 L.O. SWITCH INT./EXT.

VOLTAGES FOR PIN 25 NOT EARTHED (NORMAL OPERATION)

NOTES

ADJUSTMENTS SHOULD ONLY BE MADE WHEN IN-LOCK. THE THREE OSCILLATORS ARE IDENTICAL WITH THE EXCEPTION OF L4, L5 AND L6.

± 20% TYPICAL D.C. VOLTAGE AS MEASURED WITH 20KΩ/V METER

± 3dB TYPICAL A.C. VOLTAGE MEASURED WITH HIGH IMPEDANCE VALVE VOLTMETER OR OSCILLOSCOPE

VARACTOR LINE

AGC LINE

SIGNAL FLOW

TRANSISTORS

BFX48	TR1, 2 & 3
BFW10	TR4, 5 & 6
2N2369	TR7, 8, 9, 11 & 12
BFX89	TR10, 14 & 15
BC109	TR13

DIODES

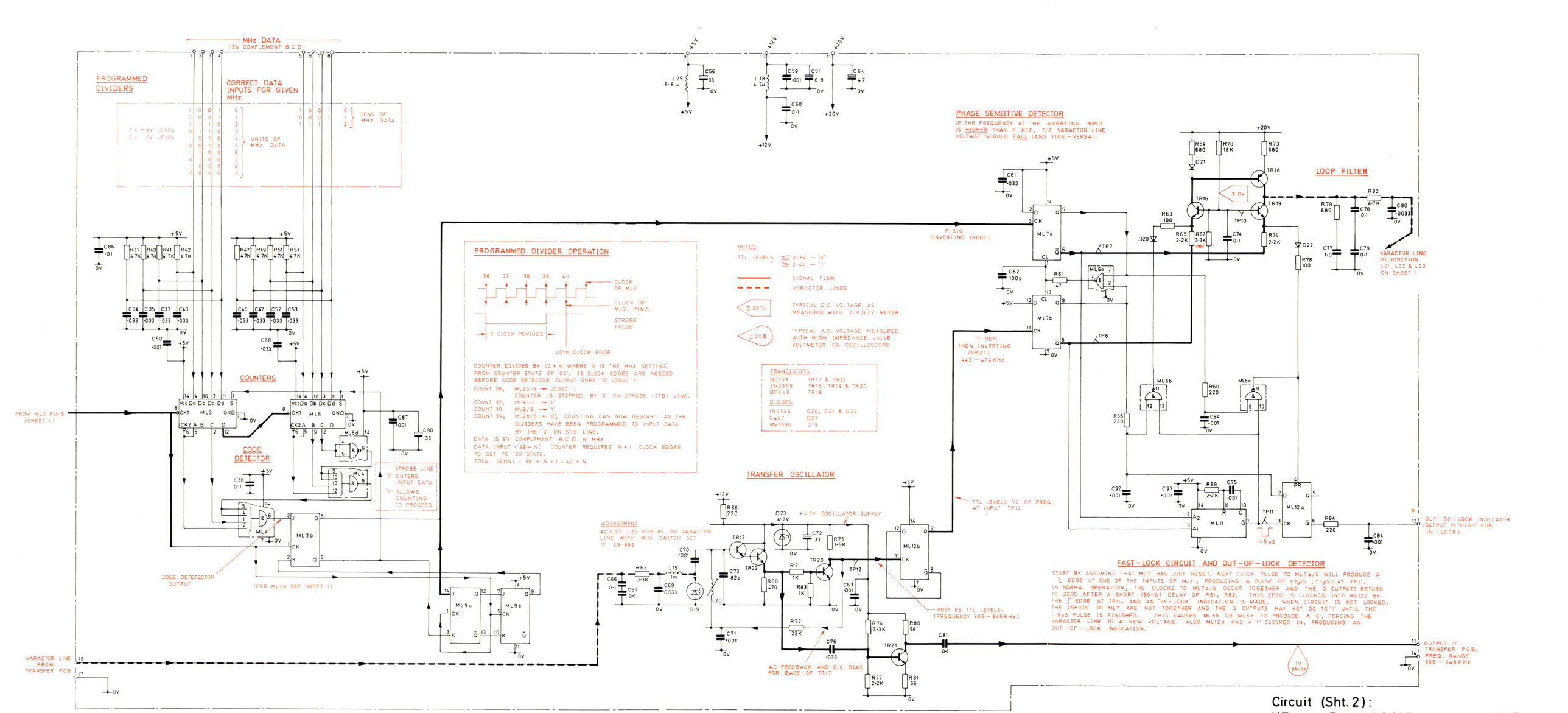
IN4149	D1, 2, 3, 10 11 & 12
MV1650	D4, 5, 6, 7, 8 & 9
HP2800	D13, 14 & 15
BAW62	D16 17 & 18

Circuit (Sht.1): HF Loop Board PS337

Fig.5·3

WOH 7049	EC44978
8	

RACAL



Circuit (Sht. 2):
HF Loop Board PS 337

Fig.5-4

CHAPTER 6

34MHz GENERATOR BOARD PM339

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CHAPTER 6

34 MHz GENERATOR BOARD PM339

INTRODUCTION

1. This board provides the 34 MHz second mixer injection frequency; it also contains the 1.4MHz carrier re-insertion generator and the 1.4MHz BFO. A circuit diagram of the board is given at the end of this chapter figs. 6.2 and 6.3.

34 MHz Oscillator

2. The 34 MHz oscillator stage, TR6, TR7, is controlled by the switching/voltage regulator transistor, TR1. With no earth applied to diode D1, TR1 conducts and provides a regulated +5V supply to the oscillator transistors. A sample of the oscillator output signal is fed to the buffer amplifier stage, TR3, TR5, and then via the forward biassed switching diodes, D5 and D6, to a balanced output amplifier, TR11, TR12 and the rear panel 34 MHz IN/OUT socket via board pin 22.

3. When the rear panel 34 MHz INT/EXT switch is set to EXT (for slave operation), an earth is routed to D1, to switch off TR1 and thereby remove the +5V supply to the oscillator transistors, and also to the diode switch via L7. Diodes D5 and D6 are reverse biassed, diode D7 is forward biassed, and the 34 MHz external input (from the master receiver) is routed via board pin 22, C34, D7 and C33 to the output amplifier, TR11, TR12.

Divide-by-34 Stage

4. A second output from the 34 MHz oscillator is buffered by NAND gate G1 of ML2 before being applied to a divide-by-34 stage: this consists of a divide-by-two (ML4 CK1-A output) and a divide-by-17 stage (ML3, ML4 CK2-C output, G2 and G3). The 17 MHz output from ML4 pin 5 is applied to the clock inputs of both halves of ML3 whilst the J1 input (ML3 pin 14) is held at logic '1' (+5V). The division factor of 17 is obtained by dividing the first 9 input clock pulses by three and the next 8 clock pulses by four. Thus for the first 9 clock pulses, 3 output pulses are produced ($9 \div 3 = 3$) and for the next 8 clock pulses, 2 output pulses are produced ($8 \div 4 = 2$), making a total of 5 output pulses for 17 input pulses. These 5 pulses are then divided by ML4 to produce a 3.2 mark-to-space ratio 1MHz squarewave output at ML4 pin 2.

1MHz Divider

5. The output from the 5MHz frequency standard, at board pin 27, is applied to a buffer amplifier, TR2, and then to a shaper stage, TR4. The squarewave output from TR4 is applied to a divide-by-five stage, ML1, which is controlled by the rear panel 1MHz INT/EXT switch. When this switch is set to INT an earth is applied to board pin

16; this is routed to the reset (R9) inputs of ML1 (via L5) and enables the divider. The resultant 1MHz output from ML1 is amplified by TR9 and the filtered (C39, L9, C44) sinusoidal output is taken to the rear panel 1MHz IN/OUT socket, via board pin 4, and also to a shaper stage, TR13.

6. When the rear panel 1MHz INT/EXT switch is set to EXT, the earth is removed from the reset (R9) inputs of ML1 and the counter is inhibited. An external 1MHz signal (from a Master receiver), applied to the rear panel 1MHz IN/OUT socket, is routed to the shaper stage, TR13, (via board pin 4) in place of the internally generated 1MHz signal.

7. The 1MHz squarewave output from TR13 is applied to ML7: this consists of four NAND gates which are used as buffers. The output from G8, at ML7 pin 6, is taken to the synthesizer, via board pin 6; the output from G9, at ML7 pin 11, is taken to the transfer loop, via board pin 8, and the output from G10, at ML7 pin 8, is taken to the phase comparator, via ML5. G11 of ML7, which has a controlling input from TR14, is used as part of the 1.4MHz carrier re-insertion generation circuit and is described in paragraph 16.

Phase Comparator

8. The output signal from the 34 MHz oscillator is divided to provide a frequency of 1MHz when the oscillator frequency is correct. This frequency is compared with a reference 1MHz frequency and any error between the two frequencies is used to develop a d.c. voltage which adjusts the oscillator frequency to eliminate the error. This voltage is generated in the phase comparator, and is applied to 34 MHz oscillator varactor diode, D4 via L3.

9. The 1MHz reference frequency signal is derived either from the 5MHz frequency standard and 1MHz divider (ML7 pin 8) or within the AFC board, connected to board pin 18. When the AFC mode is selected an earth (logic '0') is applied to board pin 19. This is inverted by G6 of ML5 to open G7, and is also applied to G5 to open G4. The 1MHz signal at board pin 18 is now applied to the clock 1 input of ML6 (part of the phase comparator) via gates G7 and G4 of ML5. When the AFC switch is set to OFF (or should the AFC facility not be fitted) gates G5 and G4 are opened for the 1MHz reference frequency from ML7 pin 8.

10. The phase comparator consists of a dual D-type flip-flop, ML6, a two-input gate, G12 of ML2, and an output voltage control circuit, TR17, TR18, TR19. The action of the circuit is as follows.

11. The output from the divide-by-34 stage, at ML4 pin 2, is applied to the clock 1 input of ML6, whilst the reference frequency output, from ML5 pin 8, is applied to the clock 2 input of ML6. The D inputs to ML6, at pins 2 and 12, are both taken to the +5V rail (logic '1'). Thus when the positive edge from ML4 pin 2 clocks ML6, the Q1 output at pin 5 changes to '1' and the $\overline{Q1}$ output changes to '0'. Similarly, when the positive edge from ML5 pin 8 clocks ML6, the Q2 output changes to '1' and the $\overline{Q2}$ output changes to '0'. When both Q1 and Q2 are at '1', the output from the NAND gate, G12 of ML2, changes to

'0', clearing both ML6 flip-flops via R74 and thus resetting the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

12. Consider the case where the 34 MHz oscillator frequency is high. This will mean that the positive going edge from the divide-by-34 stage will occur before the edge from the 1MHz reference frequency. The resultant setting and resetting of the flip-flops causes increased conduction of TR18, due to the $\overline{Q}1$ output waveform (see Figure 2.2) as compared with the conduction of TR19: this causes the voltage at the collector of TR18 to become less positive, thereby reducing the voltage applied to the varactor diode, D4, and reducing the oscillator frequency.

13. If the oscillator frequency is low, the divide-by-34 pulse will occur after the reference pulse, the $\overline{Q}2$ output waveform will cause increased conduction of TR19 and the voltage at the collector of TR18 will become more positive. The increased voltage applied to the varactor diode causes the oscillator frequency to increase, thus correcting the error.

14. When the two frequencies are in phase the two flip-flops of ML6 are clocked at the same time, the $\overline{Q}1$ output waveform is equal to the $\overline{Q}2$ output waveform and the varactor line voltage remains constant.

1.4MHz Generation

15. The 1.4MHz output signals at board pins 10 and 11 may be derived from the fixed frequency carrier re-insertion generator, a beat frequency oscillator (BFO) or a fixed offset 1.4MHz oscillator.

1.4MHz Carrier Re-insertion Generator

16. When a 1.4MHz carrier re-insertion output is required, an earth is connected to board pin 15; this is routed to the reset (RO) inputs of a divide-by-five stage, ML8, via L11, and the divider is enabled. The earth is also routed to the base of TR14; the transistor switches off and a logic '1' is applied to the NAND gate, G11 of ML7, at pin 1. The gate opens and the 1MHz square-wave signal from TR13 is applied to the BD input of ML8. The resultant 200kHz output from ML8, at pin 8, is applied to a 1.4MHz crystal filter which selects the seventh harmonic of the input. The filter is followed by a two-stage amplifier, TR15, TR16, which feeds the two output amplifier stages, TR20, TR21.

BFO

17. The BFO is selected by applying an earth to board pin 14; this completes the circuit for transistor TR8 which, with associated components, forms a 1.4MHz ± 3kHz oscillator. The front panel BFO control (a potentiometer), which is connected to board pins 23, 24 and 25, controls the voltage applied to the varactor diode, D3, and hence the oscillator frequency. The BFO output signal is coupled by C30 to the two output amplifier stages, TR20, TR21, and the amplified outputs appear at board pins 10 and 11.

Fixed Offset 1.4MHz Oscillator

18. This is an optional facility and consists of a crystal controlled Colpitts oscillator TR10. It is switched on by applying an earth to board pin 13 and the amount of frequency offset is determined by the frequency of the crystal, XL1, and the adjustment of C35. The oscillator output signal is coupled by C47 to the two output amplifier stages, TR20, TR21.

Adjustments

19. Refer to Chapter 23, paragraphs 28 to 30, for details of adjustments to the 34MHz Generator Board PM339.

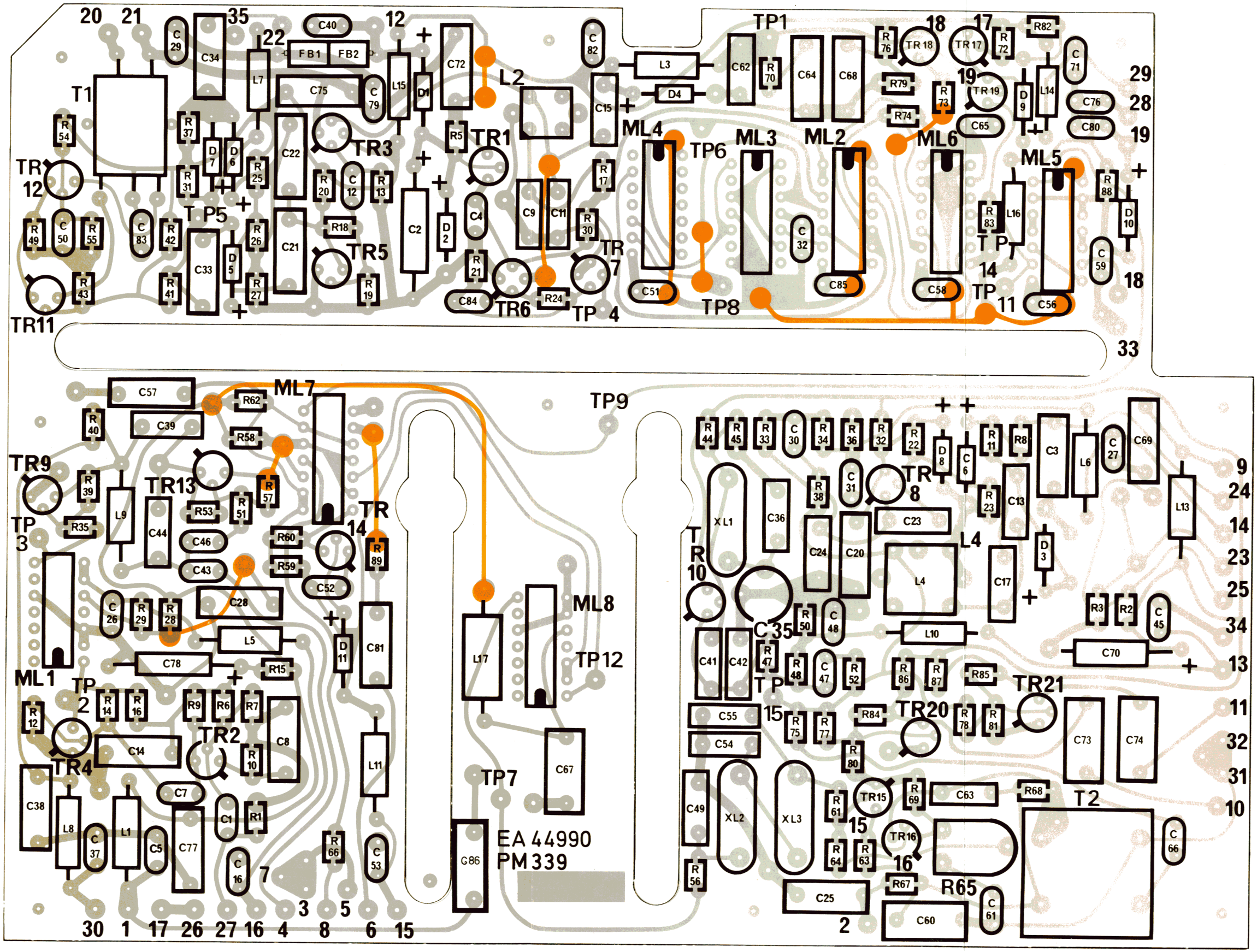

Fig.6.1

Nov.79 (Amdt.2)

Layout : 34MHz Generator Board PM339

Fig.6.1

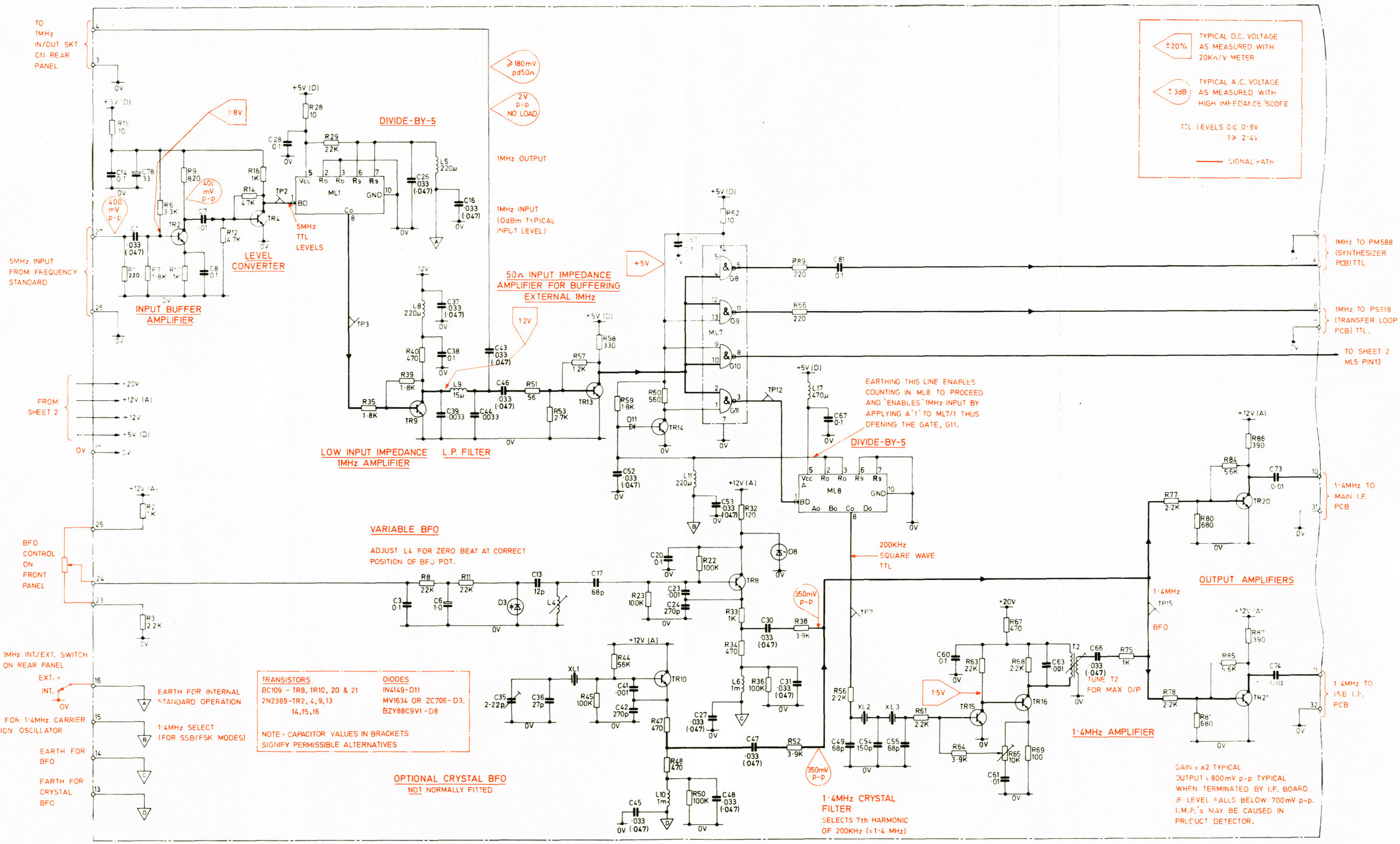

Fig.6·2

Fig.6·2

Nov. 79 (Amdt.2)

Circuit: 34MHz Generator Board PM339 (Sheet 1)

OSCILLATOR ON/OFF SWITCH

IN 'EXT' POSITION PIN 12=0V. NO +5V SUPPLY WILL BE PRESENT AND OSC. STOPS

VOLTAGE-CONTROLLED OSCILLATOR

VARACTOR LINE DRIVER

VARACTOR LINE

DIVIDE-BY-34 COUNTER

ML4a DIVIDES BY TWO, OUTPUT IS NEGATIVE EDGE OF WAVEFORM WHEN ML4/12 IS LOW.

PHASE COMPARATOR

f SIGNAL NON INVERTING INPUT

f REF INVERTING INPUT

1MHz SELECTOR SWITCH

1MHz FROM ML7 (SHT. 1)

EARTH FOR AFC

1MHz FROM AFC PCB

INT

EXT

34MHz INT./EXT. SWITCH (ON REAR PANEL)

WHEN AFC IS SELECTED (PIN 19 EARTHED), 1MHz GENERATED BY AFC BOARD IS USED AS REFERENCE FREQUENCY. NORMALLY (AFC OFF), 1MHz IS GENERATED BY 34MHz BOARD (SEE SHT. 1)

OUTPUT AMPLIFIER

AMPLIFIER

DIODE SWITCH

NORMAL (INT) MODE

FIN12 NOT EARTHED, D5,6 CONDUCT (WITH VOLTAGES AS SHOWN ABOVE) PASSING SIGNAL TO MIXER AND 34MHz IN/OUT SOCKET.

EXT. MODE

D5,6 CUT-OFF, D7 CONDUCTS, 34MHz INPUT THROUGH TO MIXER.

180mV MIN. RMS INTO 50Ω

34MHz OUTPUT (SWITCH IN 'INT' POSN)

34MHz INPUT (SWITCH IN 'EXT' POSN)

34MHz IN/OUT SOCKET

1V RMS

34MHz OUTPUT TO SECOND MIXER

+5V (D)

+12V

+12V (A)

+20V

ML2 ML3a ML3b ML4 ML5 ML6a ML6b

TR1 TR3 TR5 TR6 TR7 TR11 TR12 TR17 TR18 TR19

D1 D2 D4 D5 D6 D7 D9 D10

FB1 FB2 FB3

T1

TP1 TP4 TP5 TP6 TP8 TP9 TP11 TP14

DISTORS

-TR5, TR11, TR12, TR18, TR19.
TR1
TR6, TR7
-TR17
-TR3

:S

· D1, D9, D10
:5V6 - D2
OR ZC706-D4
-D5, D6, D7

·SIGNAL PATH
·VARACTOR LINE

· CAPACITOR VALUES IN
ETS SIGNIFY PERMISSIBLE
NATIVES.

WOH 7049	EC44990/V
B 2 5 9 10 11 12 13	

Circuit: 34MHz Generator Board PM339 (Sheet 2)

34MHz-2

Fig.6·3

CHAPTER 7

FREQUENCY STANDARD ASSEMBLY

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CHAPTER 7

FREQUENCY STANDARD ASSEMBLY

INTRODUCTION

1. One of two types of 5 MHz frequency standard may be fitted to the receiver, dependent upon the degree of frequency stability required. The frequency standard module plugs into a B7G base attached to a small printed circuit board, and is secured to the board by two screws. The two types of frequency standard available are described below. Provision is included for the use of an external frequency standard, which is connected to the receiver via a rear panel BNC provides for the selector of either internal or external standard operation.

FREQUENCY STANDARD TYPE 9400

2. The Racal 9400 frequency standard is a fast warm-up crystal oscillator providing a high degree of accuracy and long term stability with low power consumption (table 1). The crystal is housed in a temperature controlled oven which, together with the maintaining circuit and a buffer amplifier, is fitted in a metal can with polyurethane foam to provide heat insulation. Access may be gained to the internal trimmer capacitor after removal of a small rubber bung. Adjustment instructions are given in para. 5.

FREQUENCY STANDARD TYPE 9420

3. The Racal 9420 frequency standard is a compact crystal oscillator similar to the 9420. It contains a high quality crystal which is operated in the third overtone mode. Like the 9400, the metal can contains polyurethane foam for heat insulation, and a removeable rubber bung allows access to the internal trimmer capacitor. For finer adjustment, a potentiometer is fitted to the assembly printed circuit board which sets the voltage applied to an internal varactor diode. Adjustment instructions for the 9420 are given in para. 5.

REPAIR

4. If the specified performance of either type of frequency standard cannot be obtained, users are advised to return the faulty module to Racal Instruments Limited for servicing, since select-on-test components and precise assembly techniques are employed to ensure the specified performance.

ADJUSTMENT

Test Equipment

5. The items of test equipment listed below are required for adjustment of the frequency standard assembly.

(1) Frequency Standard.
(Example: Rubidium Standard Racal Instruments 9475)

(2) Frequency Comparator
(Example: Montronic Type 100-7)

(3) Digital Frequency Meter

Range: d.c. to 70 MHz

Accuracy: Internal Standard : 1 part in 10^6 plus or minus 1 count.

External Standard : Accuracy of standard plus or minus 1 count

(Example : Racal Instruments 9915)

Procedure

6. No attempt should be made to adjust the frequency standard until the receiver has been operating continuously for at least one hour. Both the 9400 and the 9420 frequency standards have an internal preset trimmer capacitor for adjustment purposes; access is gained, in each case, by the removal of the rubber plug. The capacitor trim range for the 9400 standard is -6 to +3 parts in 10^6, whilst that for the 9420 trimmer capacitor is -8 to +2 parts in 10^7. For finer adjustment a multi-turn potentiometer is fitted to the 9420 frequency standard board: this has an adjustment range of 1 part in 10^7. The adjustment procedure given below uses a frequency comparator which compares the 1 MHz output signal from the receiver with a reference 1 MHz signal from an external frequency standard which has a higher degree of accuracy and stability than either the 9400 or the 9420. The frequency comparator produces a 100 kHz difference frequency output signal which is applied to the digital frequency meter.

7. (1) Connect the 1 MHz IN/OUT socket on the receiver rear panel to the TEST INPUT socket on the frequency comparator.

(2) Connect the 100 kHz output socket on the frequency comparator to the signal input socket on the digital frequency meter.

(3) Using a T-piece, connect the 1 MHz output from the external standard to the REF INPUT socket on the frequency comparator, and to the external standard input socket on the digital frequency meter. Set the digital

frequency meter to operate from an external 1 MHz standard.

(4) Set the digital frequency meter to resolve 1 Hz/second: the frequency of the receiver 1 MHz standard will now be displayed to the resolution set on the frequency comparator.

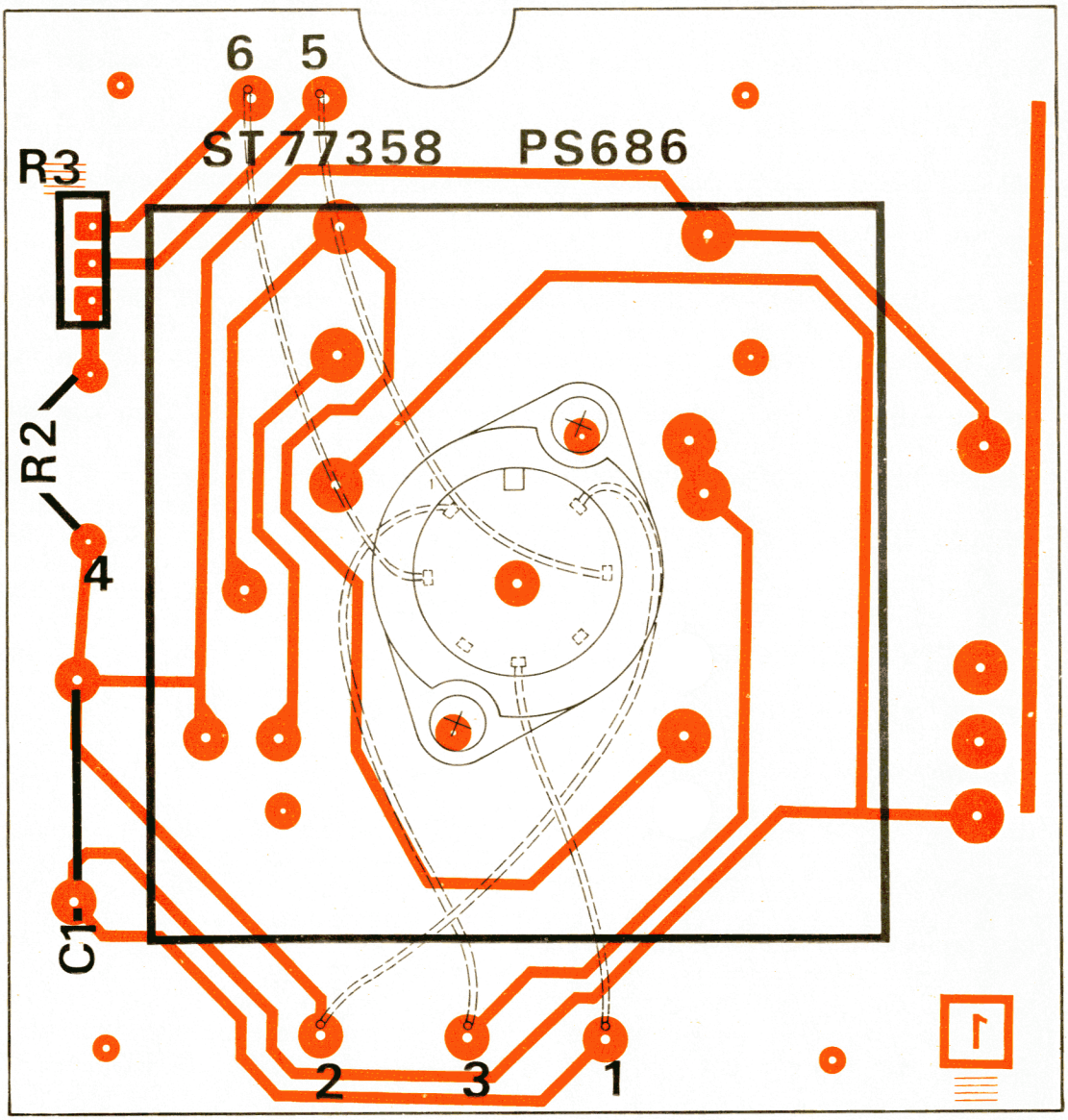
(5) Set the receiver frequency standard to the appropriate specification, as follows:

9400 : Better than 5 parts in 10^9
9420 : Better than 5 parts in 10^{10}

(6) Disconnect all test equipment.

Table 1 : Frequency Standard Specifications

	Units	9400	9420
Frequency	MHz	5	5
Daily Ageing Rate on delivery		$1x10^{-8}$	$2x10^{-9}$
Daily Ageing Rate after 1 month		$5x10^{-9}$	$5x10^{-10}$
Warm-up time for $1x10^{-7}$ accuracy	minutes	4	20
Retrace characteristics		$4x10^{-8}$ in 24 hours	$2x10^{-8}$ in 24 hours
Temperature Operating Range	°C	-10 to +60	-10 to +60
Stability with Temperature Change	Per °C	$1x10^{-8}$	$6x10^{-10}$
Stability with Supply Voltage Change	For 10% change	$5x10^{-8}$	$3x10^{-9}$
Minimum Output Level	mW r.m.s.	250 into 50Ω	250 into 50Ω
Trim Range		-6 +3 parts in 106	-8 +2 parts in 107
Supply Voltage	V	12	12
Typical Supply Current at 25°C	mA	55	90
Size	cm	5x5x5	5x5x9.5
	in	2x2x2	2x2x3.75
Base		B7G	B7G



9400 STANDARD (ST77358/B) : BASE CONNECTIONS TO BOARD PINS 5 & 6 OMITTED
R2 & R3 OMITTED

9420 STANDARD (ST77358/C) : AS SHOWN

RACAL

WOH7049	CA77357/3	7·1
1		1/1

WOH7049	CA77357/2	7·1
1		1/2

Layout : Frequency Standard Board

Fig. 7·1

CHAPTER 8

RF UNIT

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CHAPTER 8

RF UNIT

INTRODUCTION

1. The RF unit comprises a re-radiation filter unit, mounted in a metal box which houses the antenna socket and fuse, and an RF amplifier based PM582. The output of the filter unit fed to the RF board which contains an RF amplifier, low-pass filters, protection circuitry and, in the tuned version, preselection circuits. The circuit diagram of the unit is given at the end of this Chapter in Figure 8.3.

Wideband Protection Stage

2. This comprises transistors TR1, TR2, TR3, relay RLQ/1 and associated components. Under normal reception conditions TR2 is turned off, TR3 is turned on and relay RLQ/1 is energised. Relay contact RLQ/1 is closed and the received signal is applied to a 30MHz low-pass filter, L7, L9, C14, C15, C16, C19, C20.

3. Should the amplitude of the received signal at the antenna socket exceed a predetermined threshold (set by trimmer C31), the detected output from TR1, which is applied to the base of TR2, rises sufficiently positive to cause TR2 to conduct. Conduction of TR2 causes TR3 to switch off, relay RLQ/1 is de-energised and contact RLQ/1 removes the received signal from the 30MHz low-pass filter.

4. The threshold is set by C31 such that RLQ/1 becomes de-energised for signals which exceed approximately 30V e.m.f. at the antenna socket.

Mute Control

5. An earth, from the rear panel MUTE terminal, is routed to the base of TR3 via board pin 3 and diode D8. TR3 is turned off, relay RLQ/1 becomes de-energised, and the RF path to the 30MHz low-pass filter is broken.

6. The output signal from the 30MHz low-pass filter, which may be monitored at TP1, may take one of a number of paths dependent on the type of the RF board fitted and also the selected positions of the front panel MHz switch, as detailed below.

7. (1) MHz reading of 0 MHz: An earth from the decoder board is routed to board pin 4. Relays RLA/1 and RLB/1 are energised, the received signal from the 30MHz low-pass filter is applied to the 1MHz low-pass filter via RLA1, and thence to the wideband RF amplifier via RLB1 and contact RLR1 of the normally energised protection relay, RLR/1.

(2) MHz reading of other than 0MHz and RF TUNE control set to WB (wideband) Microswitch SA, operated when the RF TUNE control is set to WB, routes an earth from the decoder board at pin 13 to relays RLN/1 and RLP/1. The relays energise and the received signal from the 30MHz low-pass filter is routed to the wideband RF amplifier via RLN1, RLP1 and contact RLR1 of the normally energised protection relay, RLR/1.

(3) MHz reading of other than 0 MHz, RF TUNE control not in WB position: An earth from the decoder board is routed to the appropriate board pin (5 to 9) and the respective pair of relays are energised from a common +12V supply via the normally closed contacts of the micro-switch, SA. The contacts of the selected relays close and the received signal from the 30MHz low-pass filter is applied to the appropriate tuned circuit, tuned by the RF TUNE control anf thence to the wide-band RF amplifier via RLR1.

8. Contact wetting for the reed-type control relays is provided from the +12V rail via resistors R9 and R11.

Protection Stage

9. A further protection stage is fitted to the RF board. The circuit, which is similar to that of the wideband protection stage, comprises transistors TR4, TR7, TR8, relay RLR/1 and associated components. Under normal reception conditions TR7 is turned off, TR8 is turned on and relay RLR/1 is energised. Relay contact RLR1 is closed and the received signal is applied via C42 to the wideband RF amplifier.

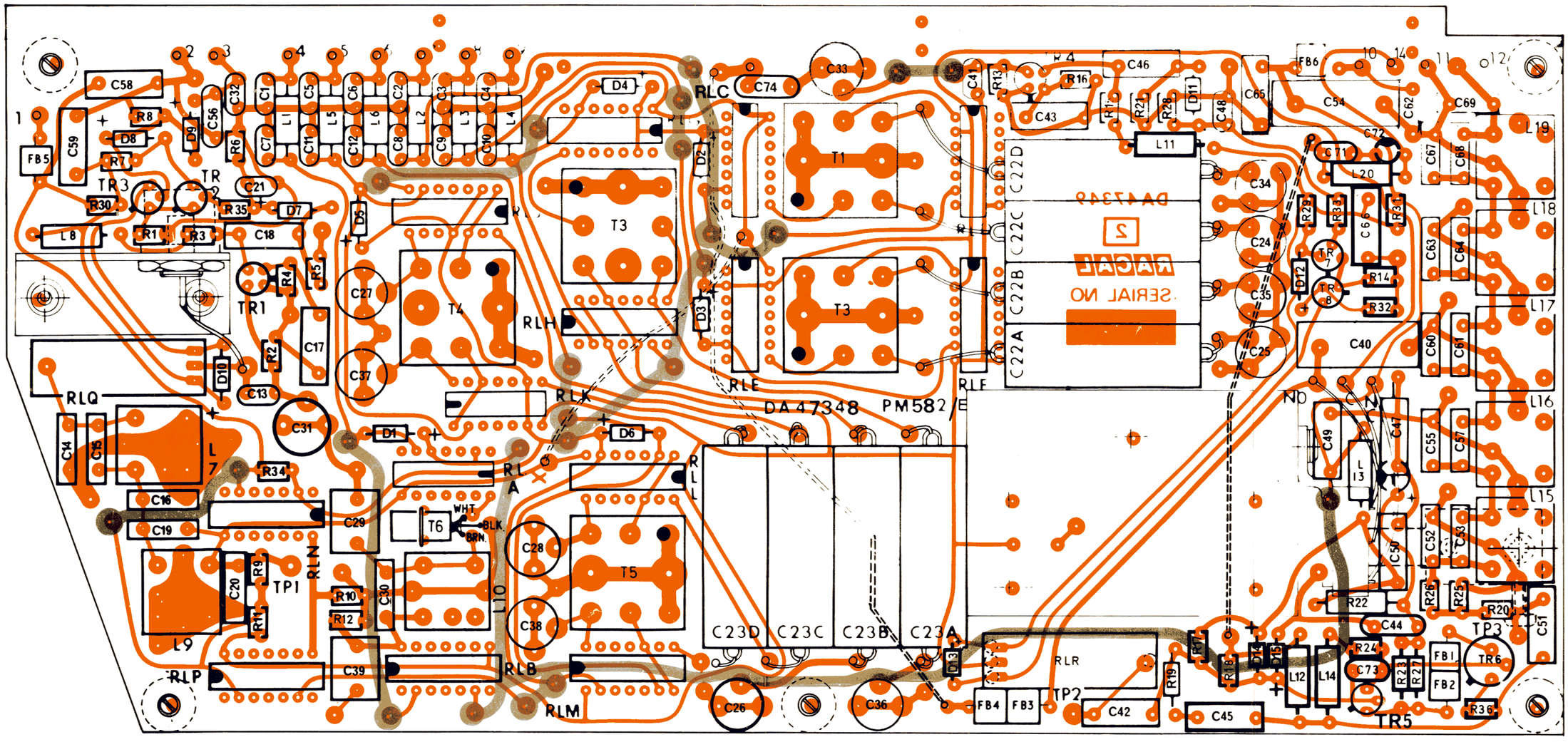
10. Should the amplitude of the RF signal applied to the protection stage exceed a predetermined threshold (set by C33) the detected output from TR4, which is applied to the base of TR7, rises sufficiently positive to cause TR7 to conduct. This causes TR8 to switch off, relay RLR/1 is de-energised and contact RLR/1 opens to remove the input to the the wideband RF amplifier.

Wideband RF Amplifier

11. The wideband amplifier, TR5, TR6 is of conventional design. The amplified output is coupled by C51 to a five-section 30 MHz low-pass filter and is then applied to the first mixer via board pin 12.

Adjustments

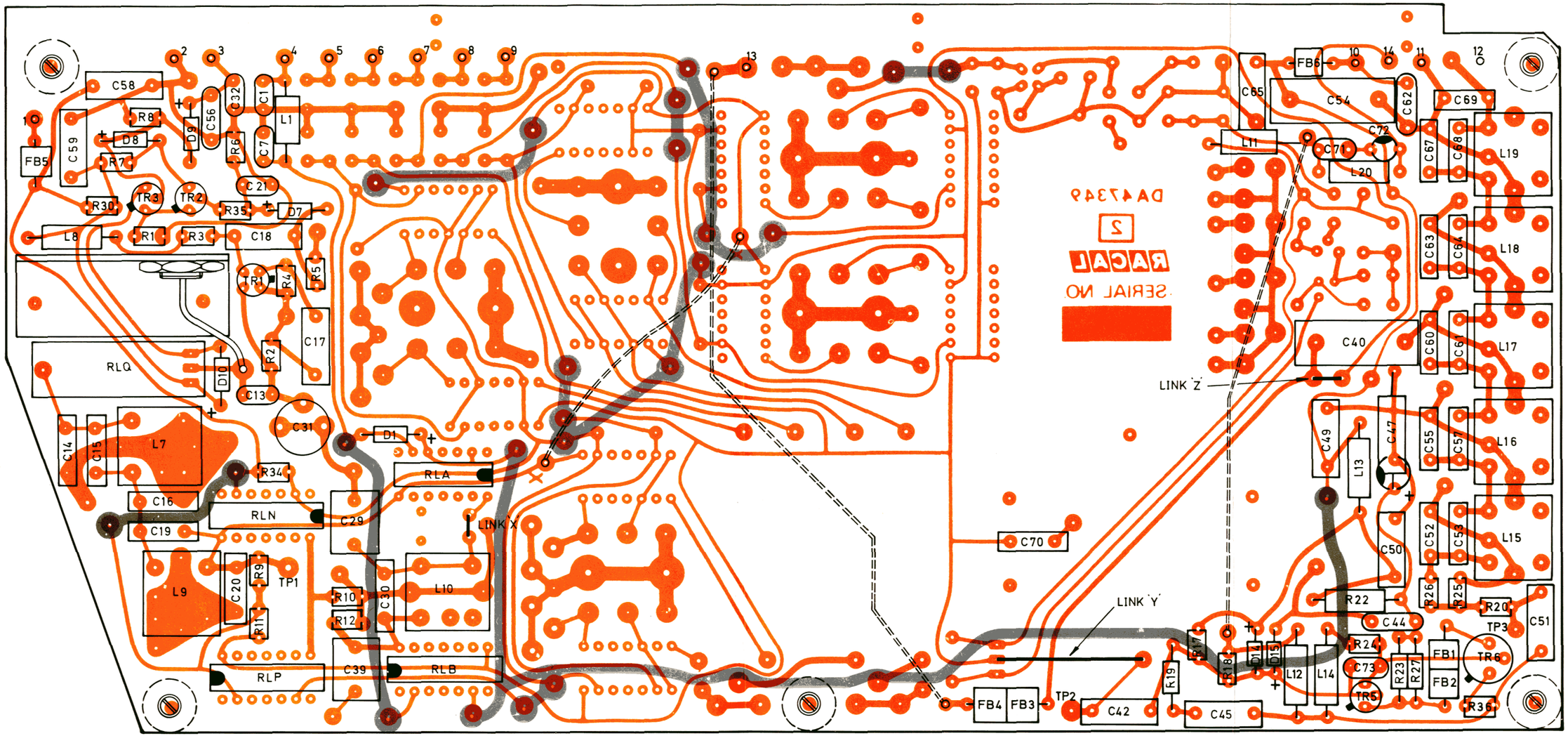
12. Refer to Chapter 23, paragraphs 63 to 68, for details of adjustments to the RF Board PM582.



WOH 7049 DA47348	8·1/1	WOH 7049 DD47350 SHT 2	8·1/2
A 1 3 4		2 5 6	
WOH 7049 DD47350	8·1/3		
2 5			

Layout : R.F. Board PM582 (Tuned)

Fig. 8.1



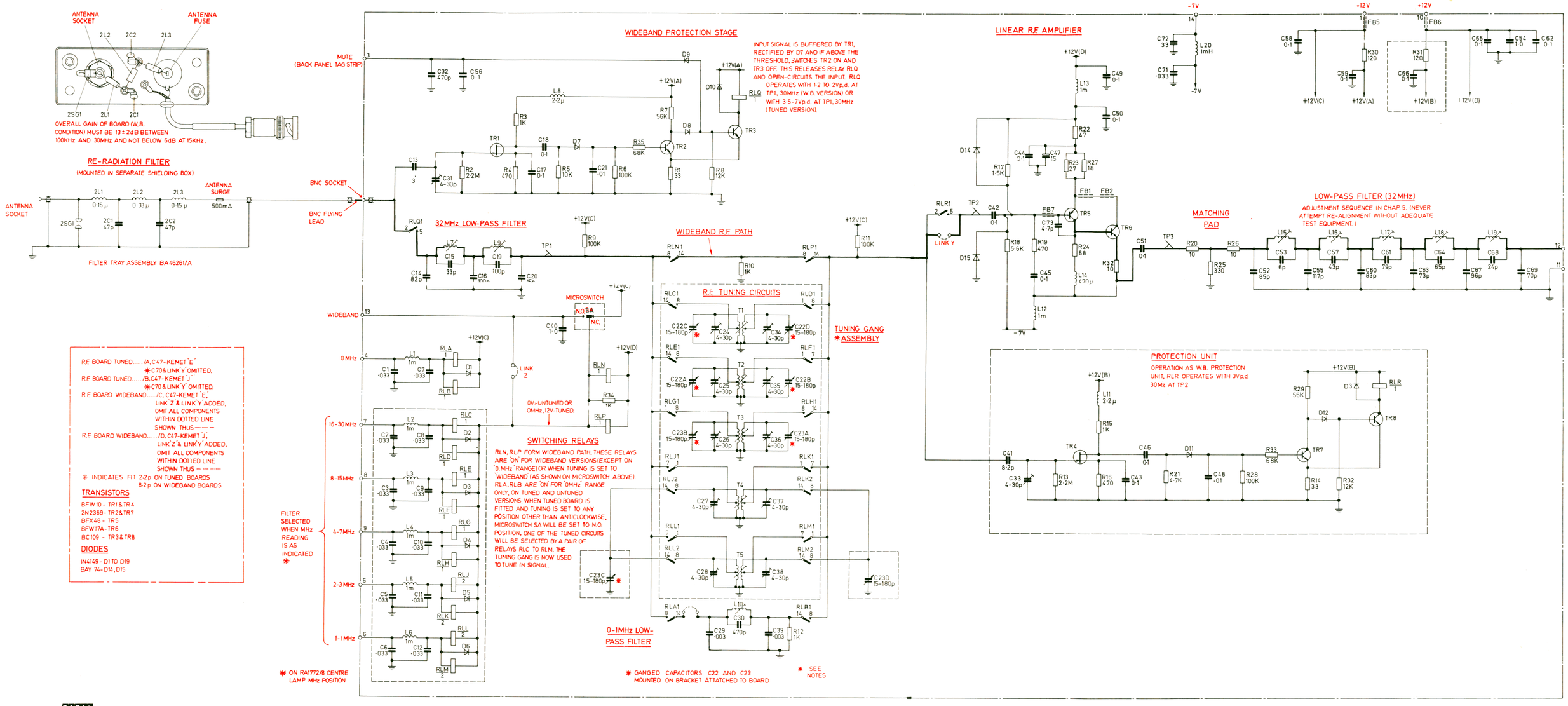
WOH 7049	DA47348	8·2
A 1 3		1/3

WOH 7049	DD47350 SHT 2	8·2
2 5		2/3

WOH 7049	DD47350	8.2
2 5		3/3

Layout : R.F. Board PM582 (Wideband)

Fig. 8·2



RACAL

WOH 7049	EC44744
1 2 4 5	

Circuit: RF Unit

RF

Fig. 8·3

CHAPTER 9

FIRST MIXER BOARD PM335

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CHAPTER 9

FIRST MIXER BOARD PM335

INTRODUCTION

1. The circuit diagram of the first mixer board is given at the end of this Chapter Figure 9.2.

2. The 35.4 to 65.4MHz local oscillator signal, from the frequency synthesizer, is applied to one of two band-pass filters, dependent on the setting of the MHz digits. For settings of 0, 1, 2 or 3MHz, an earth from the decoder board is applied to board pin 11; this is routed to diode D1 via L2 and also to D3 via L11. Diode D1 becomes forward biassed and opens a path for the local oscillator signal at board pin 10 to a crystal notch filter (passband 35.415 to 39.415 MHz with a notch frequency of 35.400 MHz) via C2, D1 and C6. Diode D3 is also forward biassed and allows the output from the crystal filter to be applied to the drive amplifier via C20, D3 and C24. Diodes D2 and D4 are both reverse biassed, via the potential dividers R3, R4, R6 and R9, R11, R12 respectively, and thus isolate the LC band-pass filter.

3. For MHz switch settings between 4 and 29 MHz inclusive, the earth is applied to board pin 8. This causes diodes D2 and D4 to become forward biassed and diodes D1 and D3 to become reverse biassed. Thus a path is opened for the local oscillator signal via the LC band-pass filter (passband 39.4 to 65.4 MHz) whilst the crystal filter becomes isolated.

Drive Amplifier

4. The mixer drive amplifier comprises transistors TR1, TR2 and TR5. The local oscillator signal from the selected filter, which may be monitored at TP5, is coupled by C28 to a common-emitter amplifier TR1. This is followed by an emitter-coupled differential amplifier, TR2, TR5 and the balanced output is coupled by transformer T4 to the mixer circuit via transformer T6.

5. A second output from transformer T4 is rectified by diode D5 to provide a d.c. output via TR8 and board pin 5. This is fed to the meter switching board and provides a meter indication of the DRIVE LEVEL to the first mixer.

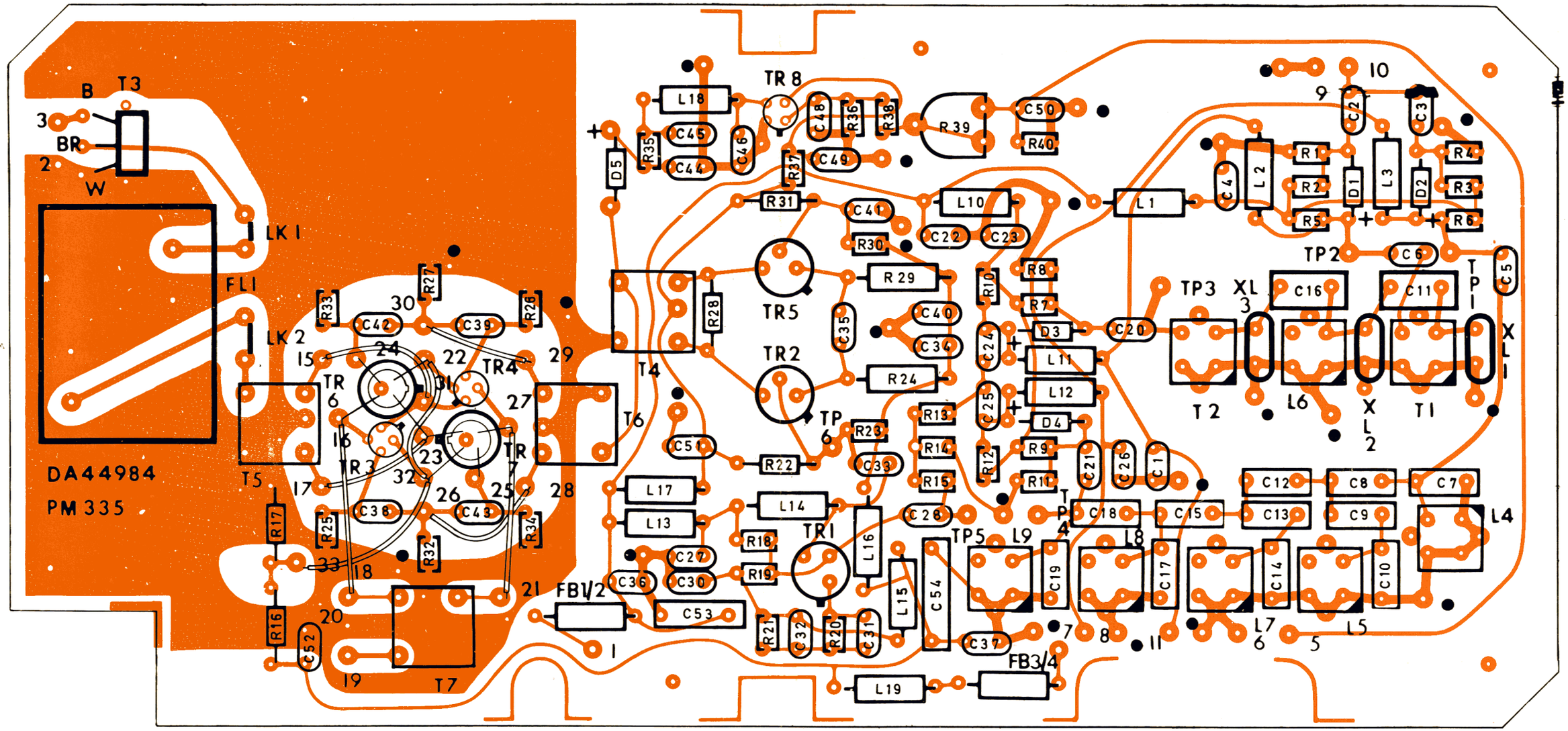
Mixer

6. The mixer is of the balanced bridge type and uses four N-channel insulated gate field effect transistors, TR3, TR4, TR6 and TR7. The local oscillator signal from T6 is capacity coupled to the gate of each transistor (via pin 30 to TR4 and TR6; via pin 26 to TR3 and TR7) whereas the RF input from the RF unit is coupled by transformer 17 to

the source of each transistor (via pin 16 to TR3 and TR6; via pin 27 to TR4 and TR7). The mixer output is taken via transformer T5 from the drains of the four transistors and is applied to a 35.4 MHz band-pass filter, FL1. Finally, the output from FL1, at the first intermediate frequency of 35.4 MHz, is applied to the second mixer board via transformer T3 and board pin 3.

Adjustments

7. Refer to Chapter 23, paragraphs 59 to 62, for details of adjustments to the First Mixer Board PM335.



RACAL

WOH 7049	DD44982 SHT 2
1	2

WOH 7049	DD44982 SHT1
1	2

Layout : First Mixer Board PM 335

Fig.9-1

TRANSISTORS

2N3866 - TR1,2&5
BSV81 - TR3,4,6&7
BFW10 - TR8

DIODES

IN4149 - D1,2,3,4&5

± 20% — TYPICAL DC VOLTAGES MEASURED WITH 20KΩ/V METER.

± 3dB — TYPICAL AC VOLTAGES MEASURED WITH HIGH-IMPEDANCE (>100MHz BANDWIDTH) OSCILLOSCOPE.

TOLERANCES AS ABOVE, UNLESS SPECIFICALLY STATED.

+12V — FB1 — FB2 — A

EARTH I.F. O/P TO FIRST I.F. BOARD (IMPEDANCE 200Ω)

W — BR — BK — T3 — 0V

INJECT TEST SIGNAL FOR FIRST I.F.

LK1 — FL1 — LK2 — Zin = 25Ω

T5 — 15 — 17 — 0V

35·400MHz
± 6·3KHz CRYSTAL FILTER

SWITCHING MIXER

B — -7V — C52 ·01 — R16 8·2K — R17 10K — 0V

33 — 32 — 31

TR3 — TR6 — TR4 — TR7

C38 ·001 — C42 ·001 — C39 ·001 — C43 ·001

R25 270K — R27 1K — R26 270K — R32 1K — R33 270K — R34 270K

16 — 24 — 23 — 22 — 30 — 26 — 25 — 27

18 — T7 — 19 — 20 — 21 — RF INPUT FROM R.F AMPLIFIER

ALTERNATIVE SIGNAL PATHS.
DEPENDENT ON THE DIRECTION OF THE L.O. WAVEFORM (POSITIVE OR NEGATIVE GOING).
LOCAL OSCILLATOR LEVEL ON PIN 30
SHOULD BE WITHIN THE RANGE 15-30Vp-p
AT ANY FREQUENCY FROM 35·415 MHz TO 65·4MHz

SIGNAL-TO-NOISE RATIO AT INPUT (R.F.) FOR 1μV EMF ≥ 10dB FOR CORRECT SIGNAL-TO-NOISE AT ANTENNA.

L.O. INPUT

29 — 0V — 28 — T6

METER DRIVE CIRCUIT (DRIVE LEVEL)

RECTIFIER D5.
L.P. FILTER C44,45,R35,L18.
SOURCE-FOLLOWER TR8. R39 REMOVES OUTPUT VARIATIONS DUE TO Vgs OF TR8.

BANDPASS FILTER (35·415 TO 39·4 MHz)

DIODE SHOWN IN 'OFF' STATE (ALL DIODE SWITCHES ARE IDENTICAL). THIS FILTER PROVIDES A DEEP NOTCH AT 35·4000 MHz ±6KHz.

+12V — L1 10 — C4 ·01 — 0V — +11V — TP2

8·5V — R2 1K — R5 22K — D1 — C2 ·01 — R1 2·2K — L2 10 — 0V

C6 ·01 — T1 — XL1 — C11 1p — L6 — XL2 — C16 1p — XL3 — T2 — 0V* — TP3 — C20 ·01 — D3 — R7 1K — R8 2·2K — R10 22K — L11 10 — C24 ·01 — 0V

2V

EARTH (VIA DIODE) WHEN MHz IS 0,1,2,3 (0-4MHz SELECT). (CONTROL VOLTAGE DERIVED BY LOGIC BOARD).

11 — C1 ·01 — 0V

BANDPASS FILTER (39·4 TO 65·4MHz) — * SWITCHED OFF

DIODE SWITCH SHOWN IN 'ON' STATE.

FROM H.F. LOOP BOARD LOCAL OSC. — 10

EARTH — 9 — 0V

750mV p-p

C3 ·01 — D2 — R3 1K — R6 22K — R4 2·2K — 0V — TP1 — C5 ·01 — L3 10 — 0V

C8 112p — C9 94p — C12 247p — C13 128p — C15 82p — C18 52p — C17 15p — C19 76p — TP4 — C21 ·01 — D4 — P9 1K — R12 22K — R11 2·2K — C25 ·01 — L12 10 — 0V

L4 — C7 56p — L5 — C10 33p — L7 — C14 100p — L8 — L9

750mV p-p

EARTH (VIA DIODE) TO SELECT 4-30MHz — 8

0·6V

C26 ·01 — 0V

MATCHING PAD

R13 10 — R15 10 — TP5 — 400mV p-p — C28 ·01 — R14 150 — 0V

AMPLIFIER

A — +12V — L13 10 — C27 ·01 — 0V — R18 4·7K — +11·5V — L14 1 — C33 ·01

-3·7V — R19 1K — R20 10 — C31 330p — R21 82 — C32 ·01 — C30 ·01 — L15 10 — -7V — B

B — -4·5V — L19 6·8 — FB3 — FB4 — 7

DIFFERENTIAL OUTPUT AMPLIFIER

A — +12V — ⚠ — C53 0·1 — C36 ·01 — L17 10 — 0V — C51 ·01 — 0V

R22 820 — TP6 — 2V p-p — -2V — R23 270 — TR1 — TR2 — TR5 — R28 1K — C35 ·01 — R24 47 — R29 47 — R30 270 — 0V — C41 ·01 — -2V — C14 ·01 — L16 10 — C40 ·01 — -7V — C54 1·0 — C17 ·01 — 0V

T4 — R31 820 — D5 — R35 4·7K — L18 10 — TR8 — R37 390 — C49 330p — C44 2·2p — C45 330p — C46 ·001 — 0V — C48 330p — R36 330 — R38 27K — R39 47K — R40 10K — C50 ·01 — 5 — METER OUTPUT TO METER BOARD. — 6 — EARTH

⚠ REFER TO MOD. No A9662

WOH 7049 | DC44984
C | 1 | 3 | 5 | 6 |

Circuit: First Mixer / Drive Amplifier PM335

1st. Mixer

Fig.9.2

CHAPTER 10

SECOND MIXER BOARD PM336

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Circuit: Second Mixer board PM336	10.2

CHAPTER 10

SECOND MIXER BOARD PM336

INTRODUCTION

1. The circuit diagram of the second mixer board is given at the end of this Chapter Figure 10.2.

2. The 35.4 MHz first IF output from the first mixer is applied to an amplifier stage, TR1, via board pin 13 and C1. The amplified output is applied via C8 to a further amplifier stage, TR5, and is also applied via C7 to a voltage controlled attenuator. This utilises two PIN diodes, D1, D2, and is controlled by the AGC 1 input at board pin 9 from the main IF/AF board. (In ISB versions AGC 2 from the ISB IF/AF board is applied to board pin 8).

PIN Diode Attenuator

3. The impedance presented to the 35.4 MHz IF signal by the PIN diodes is a function of the forward direct current passing through the diodes. When no forward current is allowed to flow the impedance is extremely high and this impedance is progressively reduced as the forward current is allowed to rise.

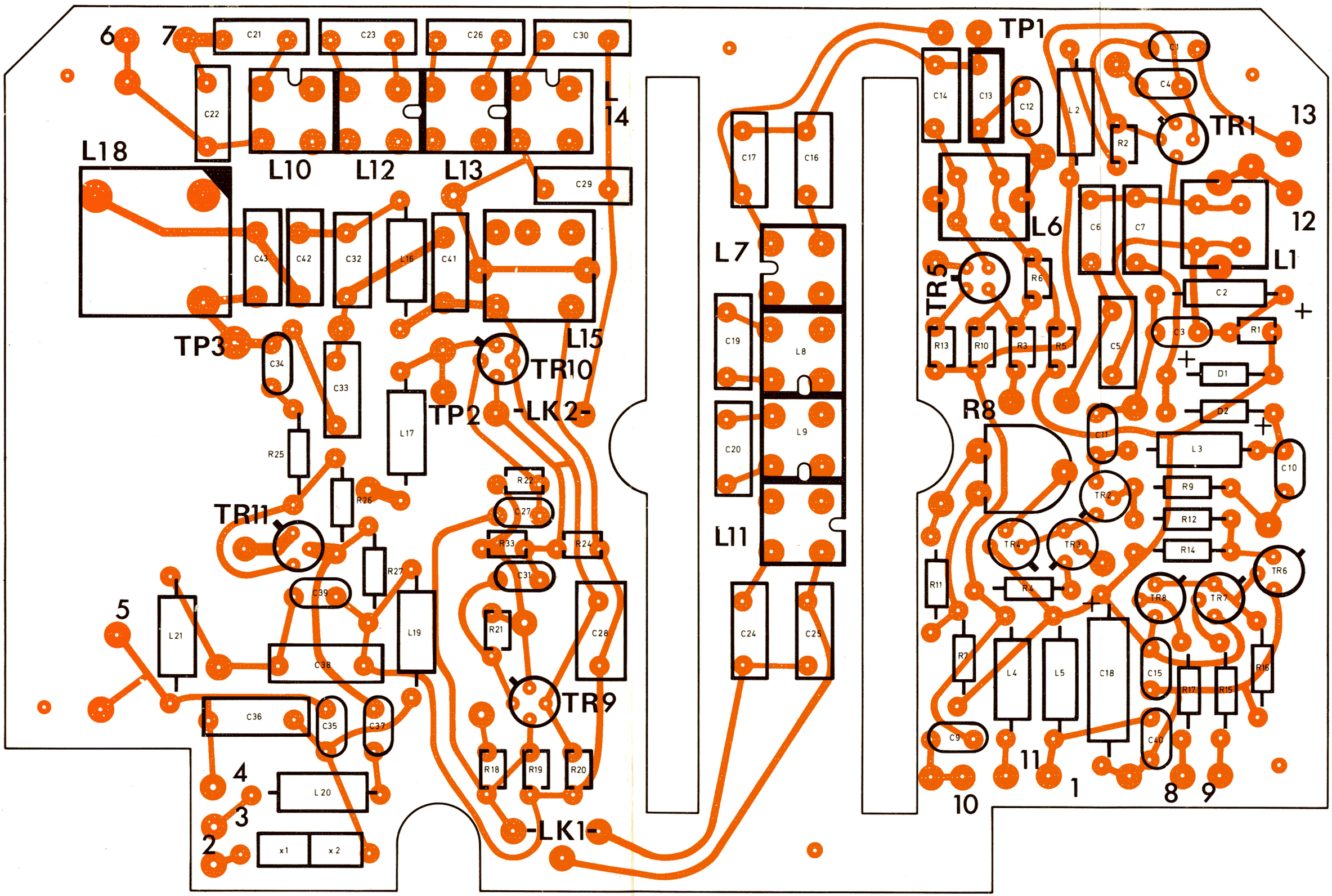
4. The AGC voltage output from the emitter follower TR7 (or, in ISB versions, the differential AGC output from TR7, TR8) is applied to the base of TR6. This stage controls the current flow through TR2 and TR4, and hence the current flow through the two PIN diodes, D1 and D2. Thus an increase in the AGC voltage causes an increased current to flow through the PIN diodes and the output from the tuned circuit of TR1 is reduced by the shunt effect of the parallel combination of D1 and D2 across the drain load of TR1.

Mixer

5. A cross-coupled balanced mixer circuit, TR9, TR10, produces the 1.4 MHz second intermediate frequency, this being the difference frequency between the 35.4 MHz first IF and the second mixer injection signal from the 34 MHz generator board. The 35.4 MHz output signal from TR5 is applied via a band-pass filter to the base of TR9 and the 34 MHz signal at board pin 7 is applied via a band-pass filter to the base of TR10. The output from the mixer is applied to a 1.4 MHz IF amplifier stage, TR11, which has a stage gain of approximately 10 dB, and the final output is applied to the IF filter board via pin 3.

Adjustments

6. Refer to Chapter 23, paragraphs 56 to 58, for details of adjustments to the Second Mixer Board PM336.

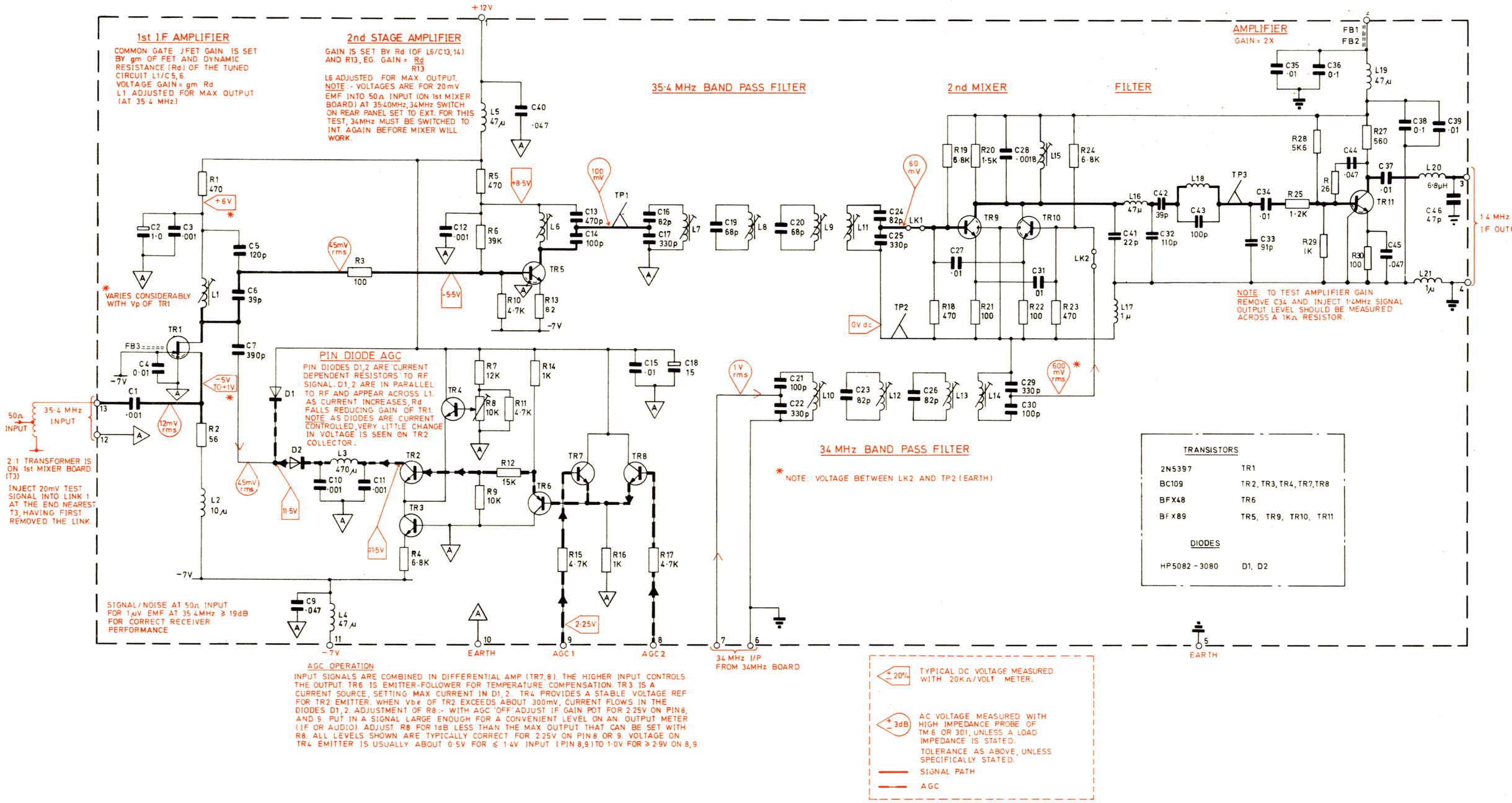


RACAL

WOH 7049	DA44987	WOH 7049	ED44985 Sht 2
2	3	4	5

Layout : Second Mixer Board PM.336

Fig. 10·1



WOH 7049	DC 44987
D 1 3 4 6 7	

Circuit: First IF Amplifier & Second Mixer PM336

Second Mixer

Fig.10.2

CHAPTER 11

IF FILTER BOARD PS367

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CHAPTER 11

IF FILTER BOARD PS367

INTRODUCTION

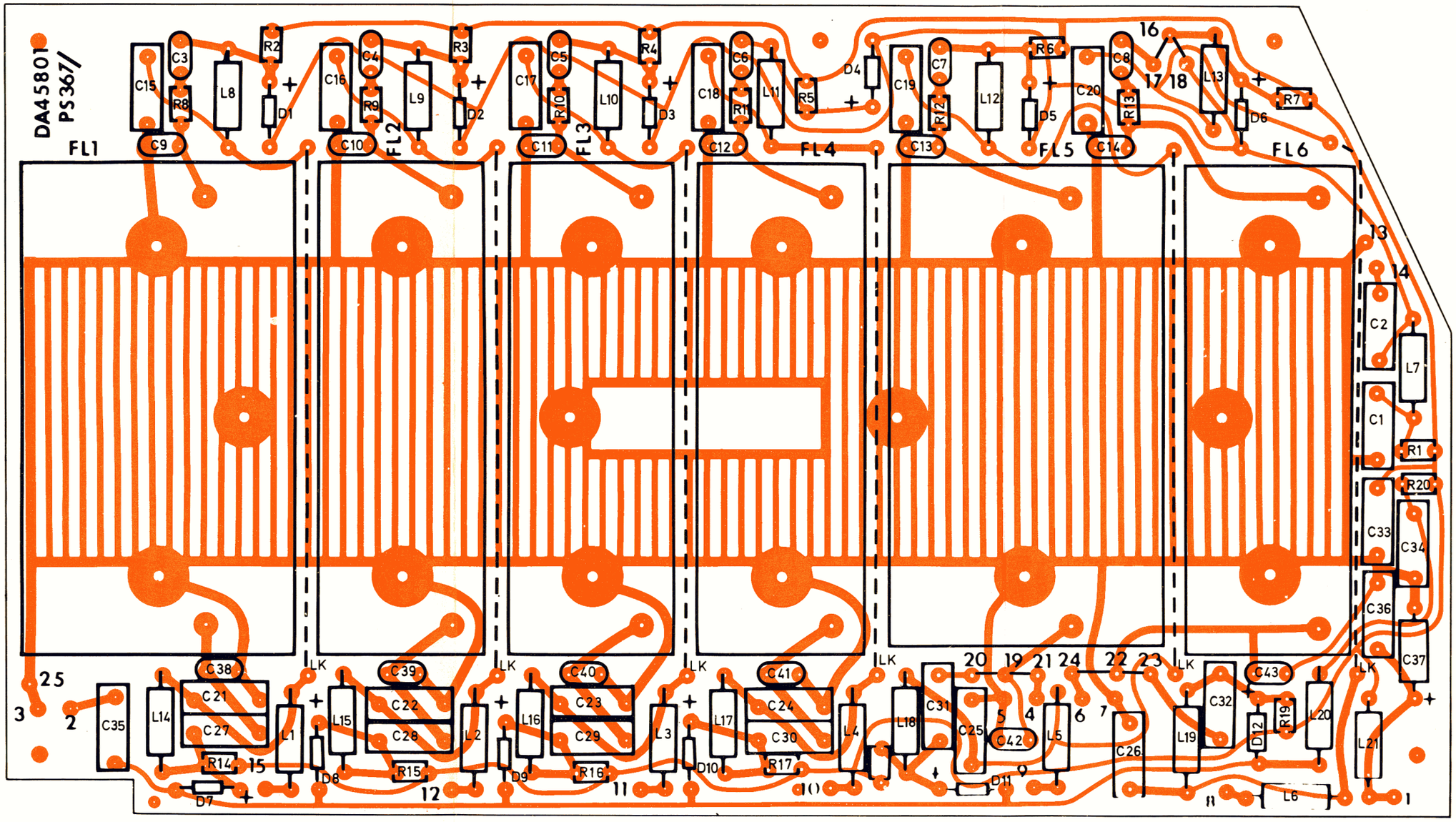
1. This board contains all the crystal filters which are used in the control of received signal selectivity. Up to six crystal filters may be fitted of which two may be SSB filters, where required (FL1 for USB, FL5 for LSB). Filter selection is effected by applying an earth to the appropriate selection line and the filtered output is taken via diode switches to a common output line. For ISB receivers, however, the output from FL5 (ISB/LSB) is routed separately, via LK1 and board pin 4, to the ISB IF/AF board. In receivers equipped with AFC, the FL6 position is used for a carrier filter; link LK2 bypasses the input switching and the output is routed to the AFC board via LK3 and board pin 6.

NOTE: Due to inversion in the receiver, a USB filter at FL1 has LSB characteristics and an LSB filter at FL5 has USB characteristics.

2. Since the selection circuit for each filter is the same, only one example is given, that of filter FL1. The circuit diagram of the board is given at the end of this Chapter Figure 11.2.

Selection Circuit

3. An earth from either the MODE switch (USB filter) or the FILTER switch (Symmetrical filter), as appropriate, is applied to board pin 15. This is routed via L1 and L8 to diode D1, and also via L14 to diode D7. Diode D1 becomes forward biassed and opens a path for the IF signal at board pin 14 to FL1 via capacitor C2, D1, C3 and R8. Diode D7 is also forward biassed and the output from FL1 is routed to board pin 2 via C27, D7 and C35. The remaining diodes, D2 to D6 and D8 to D12, are all reverse biassed and isolate the IF signal from the remaining filters, FL2 to FL6.



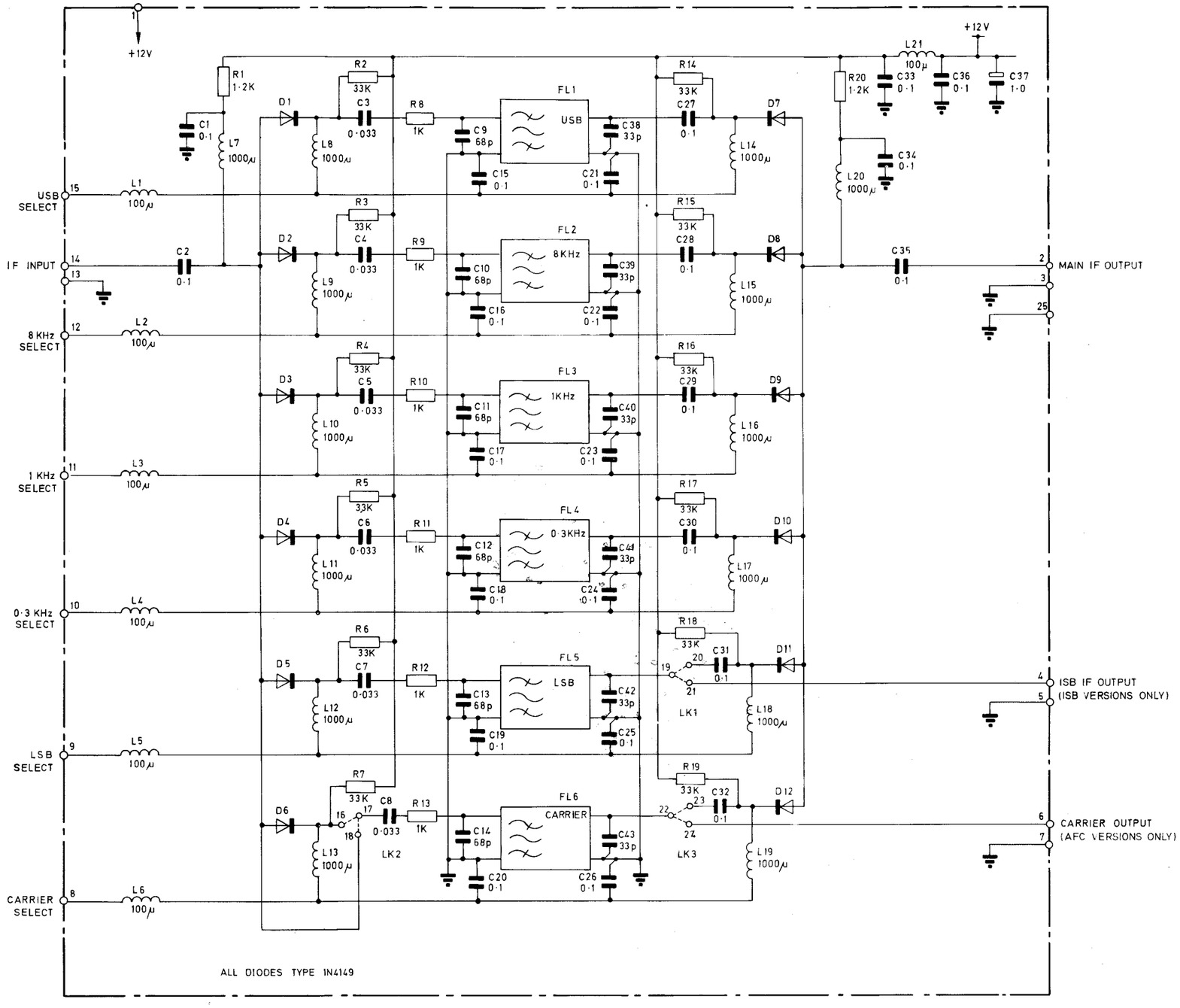
RACAL

WOH 7049	DD44964 SHT 2
1	

WOH 7049	DD44964 SHT 1
1	

Layout: Filter Board PS367

Fig. 11·1



NOTES
1. DUE TO INVERSION IN RECEIVER USB FILTER FL1 HAS LSB CHARACTERISTICS AND LSB FILTER FL5 HAS USB CHARACTERISTICS.
2. LINK PINS 19-20 FOR SSB ONLY, LINK PINS 19-21 FOR ISB.
3. LINK PINS 22-24 & PINS 17-18 ONLY WHEN CARRIER FILTER USED OTHERWISE LINK 22-23 & 16-17
4. FILTERS SHOWN ARE TYPICAL ONLY

RACAL

WOH 7049	DC45801
C 1 2	

Circuit : IF Filter Board PS367

Filter

Fig.11·2

CHAPTER 12

IF/AF BOARD PM364

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Layout: IF/AF board PM 364/3	12.3
Circuit: IF/AF board PM364	12.4

CHAPTER 12

IF/AF BOARD PM364

INTRODUCTION

1. Two IF/AF boards are used; the main IF/AF board PM364/1 and the ISB IF/AF board PM364/3. The ISB board is similar to the main board except that it contains no loudspeaker amplifier components. The circuit diagram of the boards is given at the end of the Chapter Figure 12.4.

2. The 1.4MHz i.f. signal from the Filter Board is applied to an integrated circuit gain-controlled amplifier, ML1. This device contains two amplifier sections which, in this application, are connected in cascade to provide high gain and a.g.c. range. The input signal is applied via C1 to pin 1 and the output from the first section, at pin 12, is applied via R3 and C7 to the input of the second section, at pin 10. The output, which is taken from pin 7, is applied via a band-pass filter and C12 to an i.f. output amplifier, TR2, TR4 and TR6. The output from TR6 is taken to the rear panel MAIN IF OUT socket via C23, R100 and board pin 2.

A.G.C. Detector and Amplifier Stages

3. A second output from amplifier TR2 is coupled by C19 to the a.g.c. detector TR7, TR9, and is also fed via C30 to the hand detector, TR11, switching amplifier stages ML3, ML4 and TR13 (para. 6). The positive output voltage from the a.g.c. detector is taken from the emitter of TR7 and is applied to the switched time constant capacitors, C13, C14, C16 and C20, via R20. The front panel a.g.c. switch, when set to SHORT, routes an earth to board pin 25 and this connects R13 across the series/parallel connected time constant capacitors (effective total capacitance approximately 25μF). When the a.g.c. switch is set to LONG the earth is transferred to board pin 26; R13 is disconnected and capacitors C14 and C16 are short circuited to produce a time constant capacitance of 66μF (parallel combination of C13 and C20).

4. ML2 is connected as a linear amplifier. The output at pin 6 is applied via diode D2 and board pin 29 to various points within the receiver and also via the LONG and SHORT positions of the a.g.c. switch to board pin 30. Transistor TR1 and variable resistor R4 provide a means of shifting the d.c. level of the a.g.c. voltage before it is applied to the i.f. amplifier stage, ML1. When the a.g.c. switch is set to OFF a positive voltage is applied to board pin 30 via the manual IF GAIN control.

Hang Detector

5. This circuit holds the level of the a.g.c. output voltage from ML2 following an interruption in the received transmission, for a period of approximately 2.5 seconds. The circuit is only operative when the a.g.c. switch is in the LONG position.

6. The i.f. output from TR2 is coupled to the base of detector TR11 via C19 and C30. The output from TR11 is applied to the inverting input of ML3 and the preset variable resistor R42 sets the voltage level applied to the non-inverting input such that the output at ML3 pin 6 is negative (clamped to approximately -0.7V by D7) when a received signal is present. This negative voltage is applied to the inverting input of ML4. The potential divider, R48, R49, sets the voltage applied to the non-inverting input of ML4 to approximately +7V and the resulting positive output, at ML4 pin 6, is applied to the base of TR13 via R53. Since this voltage is more positive than that applied to the emitter of TR13 (which is held at approximately +7V) the transistor is switched off and the resulting negative voltage at the collector of TR13 holds off TR3 via D9. Board pin 24 is taken to earth by the a.g.c. switch when set to LONG (as is pin 26).

7. When a break in the received transmission occurs the corresponding reduction in the emitter current of TR11 causes the voltage level applied to pin 2 of ML3 to fall below the preset voltage level applied to pin 3 (of ML3). The output from ML3 switches from negative to positive and capacitor C38 charges, via R45 and R46. Once the level of the exponentially rising voltage at ML4 pin 2 exceeds the level of the fixed potential applied to ML4 pin 3 (approximately +7V), the output of ML4, at pin 6, switches from positive to negative. TR13 conducts, the negative voltage applied to D9 is removed and TR3 conducts. The time constant capacitors C13 and C20 discharge via R17 and TR3 and the a.g.c. voltage output from ML2 falls exponentially to zero.

8. When the received transmission recommences, the emitter voltage of TR11 rises, the output of ML3 switches from positive to negative and C38 rapidly discharges via R46, D8 and the low impedance output circuit of ML3. The output of ML4 switches from negative to positive, both TR13 and TR3 are cut off and the a.g.c. voltage from TR7 charges the time constant capacitors, C13 and C20, via R20.

9. The operation of the hang detector circuit, as described above, and also where the duration of the break in the received signal is shorter than the hang time period, is shown in the waveform diagram, fig. 12.1.

A.M. and S.S.B. Detectors

10. The i.f. output from ML1 and the band-pass filter is coupled to a buffer stage TR8, via C12 and C15. The output from TR8, at TP4, is capacity coupled to both the a.m. detector, via C26 and the s.s.b. detector, via C29.

AL/5 11. The low distortion a.m. detector, TR10, is followed by a low-pass filter, L5, R37, C31. A similar filter follows the s.s.b. detector which consists of ~~a modified Foster-Seeley circuit~~, T1, D3 to D6, R43 and C33.

12. A diode switching arrangement, controlled by the MODE switch, is used to select the output from either the a.m. detector or the s.s.b. detector. In the AM position of the MODE switch, an earth is applied to board pin 7; this is routed to D11 via R52, the diode becomes forward biassed, and a path is opened for the output from the a.m. detector to the audio pre-amplifier via C37, D11 and C40. Diode D10 remains reverse-biassed and isolates the output from the s.s.b. detector.

13. For all remaining positions of the MODE switch, the earth is transferred to board pin 6. Diode D10 becomes forward-biassed and opens a path for the output from the s.s.b. detector whilst D11 becomes reverse-biassed and isolates the output from the a.m. detector.

Audio Pre-Amplifier

14. The output from the selected detector is applied to a high gain, impedance matching amplifier, TR14, TR15. The output, which is applied to the MODE switch and the preset u.s.b. line level control, via C41 and board pin 8, is muted by transistor TR16 when an earth is applied to board pin 10.

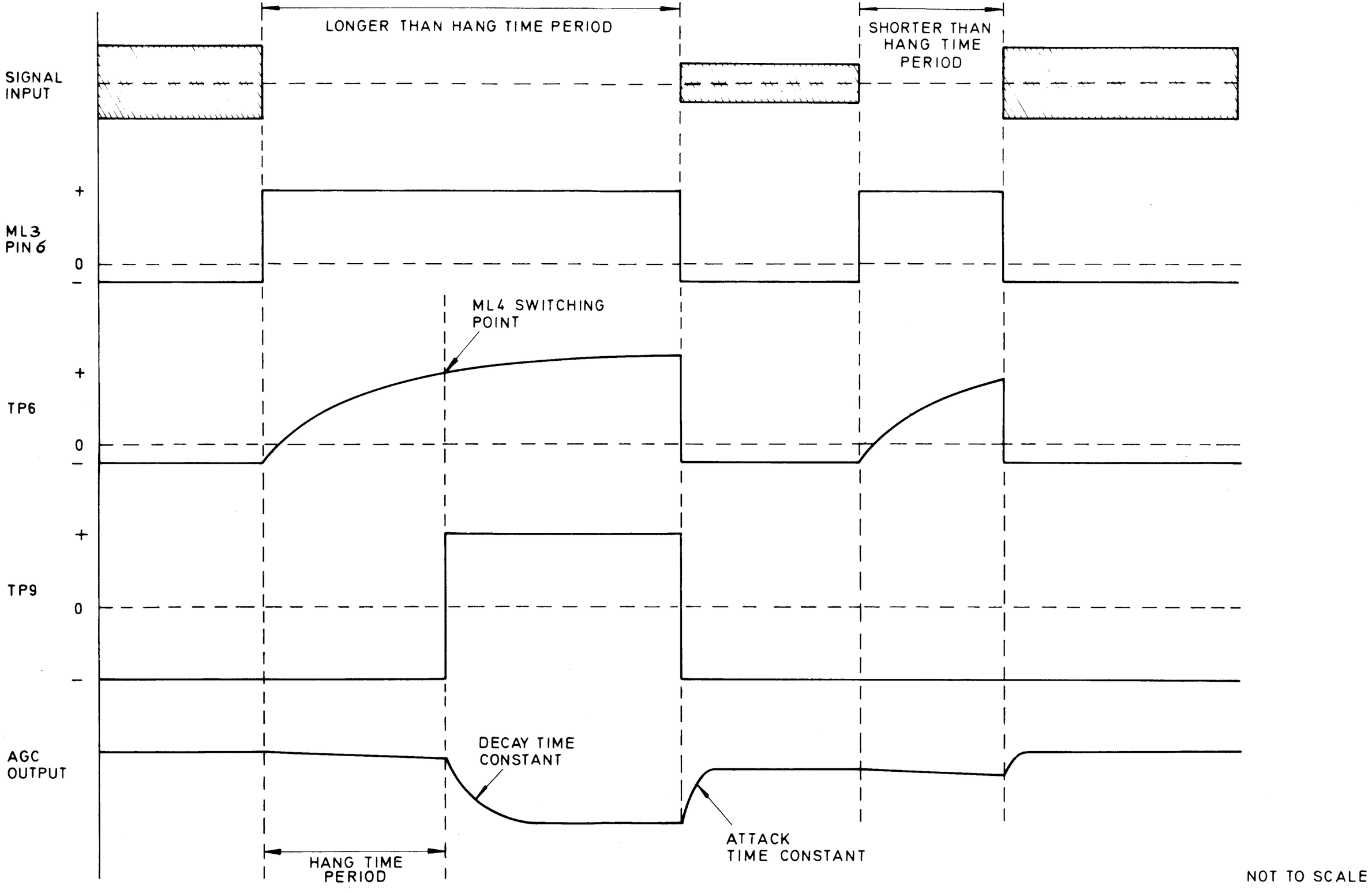
Audio Line Amplifier

15. The audio line amplifier consists of an integrated circuit linear amplifier, ML5, which drives the complementary output transistors, TR22 and TR23. The output signal, from the preset USB line level control, is applied to ML5 via board pin 11, C45 and a low-pass filter, R74 and C49. The audio line output is taken to the rear panel terminals via transformer T2 and board pins 15 and 16.

Loudspeaker Amplifier

16. The input to the loudspeaker amplifier is switched (MODE switch) to receive either the pre-amplifier output from the main i.f./a.f. board (u.s.b.) or that from the i.s.b./i.f./a.f. board (l.s.b.).

17. The direct-coupled amplifier comprises transistors TR17 to TR21, TR24 and TR25. The input from board pin 23 is applied to the input stage, TR17, via C42 and a low-pass filter, R69 and C47 with feedback components C46 and R72. This is followed by a further amplifier stage, TR18, with negative-feedback provided by C51. TR19 provides bias for the output transistors and R84 sets the quiescent current. Phase splitting is achieved by the use of complementary transistors, TR20, TR21, which drive the single-ended push-pull output stage, TR24, TR25. The amplifier output, at board pin 18, is taken direct to the rear panel loudspeaker terminal and via dropper resistors to the two headphone jacks and the internal loudspeaker.

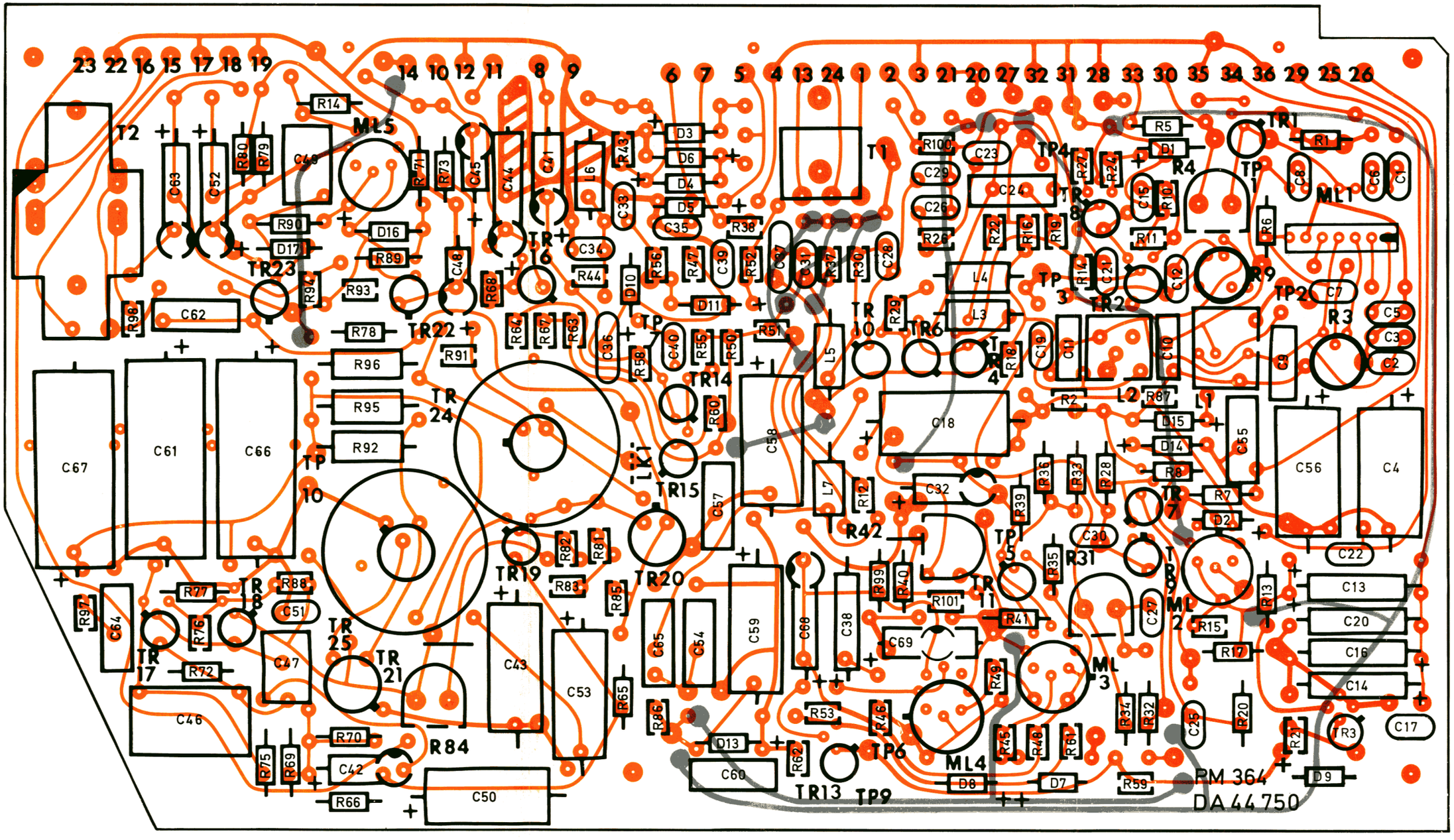


RACAL

WOH9318

Timing Diagram : AGC Hang Detector

Fig.12·1



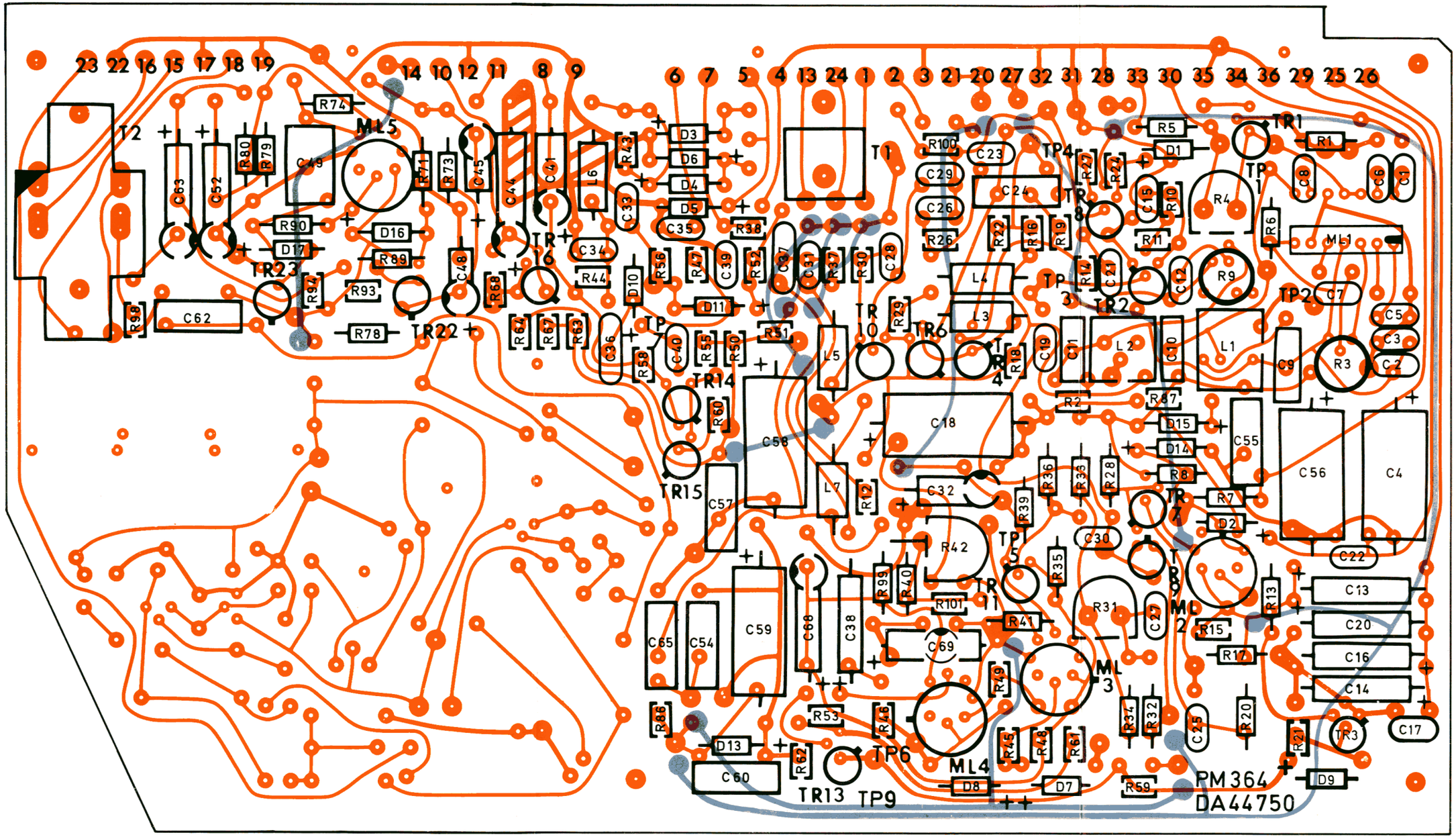
WOH 9318	DD 44748 SHT 3
1 5 7	

WOH 9318	DD 44748 SHT 2
1 5 7	

WOH 9318	DD 44748 SHT. 4
5 7	

Layout : Main IF/AF Board PM364/1

Fig.12.2



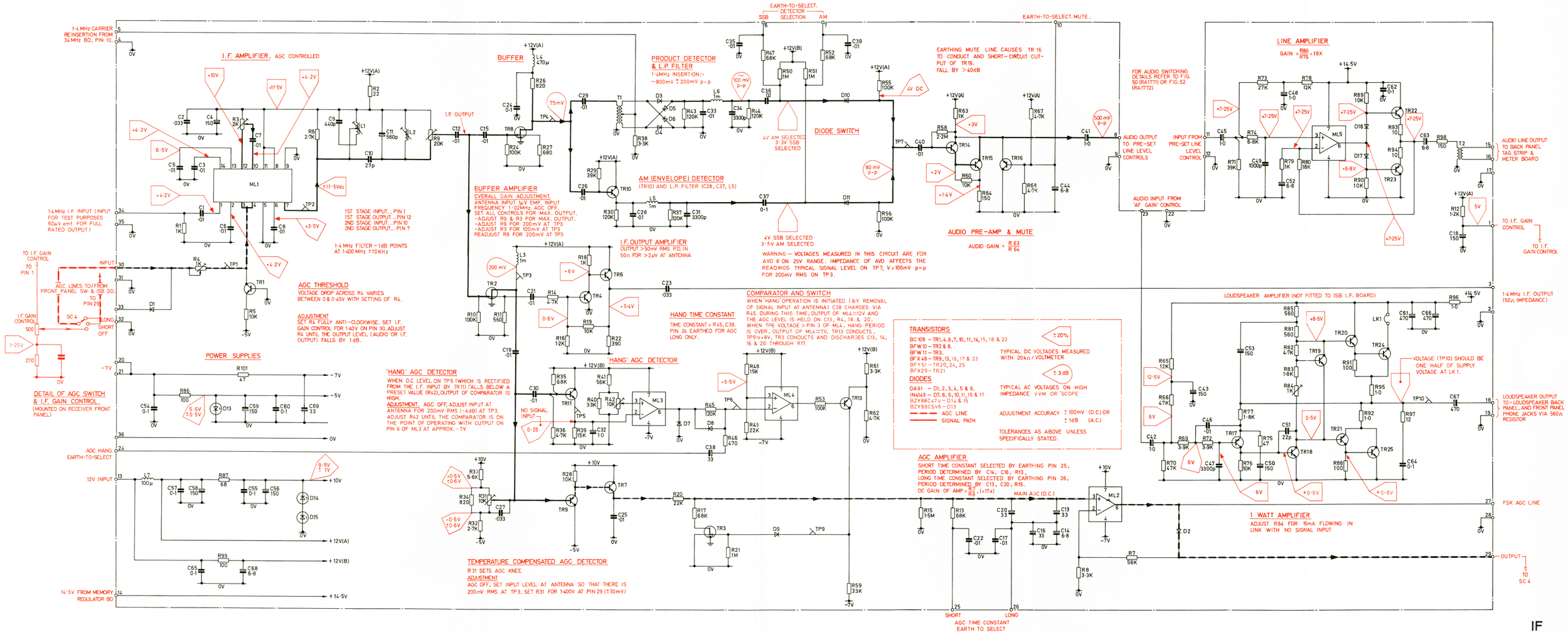
WOH9318	DD44748 SHT3
1	5 7

WOH9318	DD44748 SHT2
1	5 7

WOH9318	DD44750
4	7

Layout : ISB IF/AF Board PM364/3

Fig. 12.3



WOH9318 | EC44750/A/B/C/D
B | 1 | 2 | 3 | 5 |

Circuit : IF/AF Board PM364

IF

Fig.12.4

CHAPTER 12A

IF/AF BOARD PM674

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Layout: ISB IF/AF board PM674/2	12A.2
Circuit: IF/AF board PM674	12A.3

CHAPTER 12A

IF/AF BOARD PM674

INTRODUCTION

1. The IF/AF board type PM674, which was introduced by modification number A.8529, is a fully-interchangeable alternative to type PM364.

2. Two versions of the new board are used; the main IF/AF board PM674/1 and the ISB IF/AF board PM674/2. The boards are similar except that the ISB version does not have the loudspeaker amplifier stage. The circuit diagram is given in Fig.12A.3.

CIRCUIT DESCRIPTION

Main IF Amplifier

3. The 1.4 MHz IF signal from the filter board is applied to a two-stage integrated-circuit IF amplifier consisting of ML1 and ML2. The input of ML2 is fed from the output of ML1 via attenuator R11 and R12. AGC is applied to both amplifiers via R3 and R13. The output of ML2 is matched into a band-pass filter by TR1 and is then coupled via R23 and C13 to an IF amplifier consisting of TR2, TR3 and TR4. The output from TR4 is taken to the rear panel MAIN IF OUT socket (ISB IF OUT socket for ISB IF/AF board) via C24 and R35 .

AGC Detector and Amplifier Stages

4. A second output from amplifier TR2 is coupled by C19 to the AGC detector, TR7, TR8, and is also fed via C31 to the hang detector, TR10, switching amplifier stages ML4A, ML4B and TR11 (see para.6). The positive output voltage from the AGC detector is taken from the emitter of TR7 and is applied to the switched time-constant capacitors, C16, C17, C20 and C22, via R33. The front panel AGC switch, when set to SHORT, routes an earth to board pin 25 and this connects R30 across the series/parallel connected time-constant capacitors (effective total capacitance approximately 25 μF). When the AGC switch is set to LONG, the earth is transferred to board pin 26; R30 is disconnected and capacitors C17 and C20 are short-circuited to produce a time-constant capacitance of 66 μF (parallel combination of C16 and C22).

5. ML3A is connected as a linear amplifier. The output at pin 12 is applied via diode D2 and board pin 29 to various points within the receiver, and via the LONG and SHORT positions of the AGC switch to board pin 30. ML3B and associated components provide a means of shifting the d.c. level of the AGC voltage before it is applied to the IF amplifier stage, ML1 and ML2. When the AGC switch is set to OFF, a positive voltage is applied to board pin 30 via the manual IF GAIN control.

Hang Detector

6. This circuit holds the level of the AGC output voltage from ML3A, following an interruption in the received transmission, for a period of approximately 2.5 seconds. The circuit is operative only when the AGC switch is in the LONG position.

7. The IF output from TR2 is coupled to the base of detector TR10 via C19 and C31. The output from TR10 is applied to the inverting input of ML4A and the preset variable resistor R55 sets the voltage level applied to the non-inverting input, such that the output of ML4A pin 12 is negative (clamped to approximate -0.7 V by D8) when a received signal is present. This negative voltage is applied to the inverting input of ML4B. The potential divider, R61, R62, sets the voltage applied to the non-inverting input of ML4B to approximately +5.5 V and the resulting positive output, at ML4B pin 10, is applied to the base of TR11 via R65. Since this voltage is more positive than that applied to the emitter of TR11, the transistor is switched off and the resulting negative voltage at the collector of TR11 holds off TR5 via D9. Board pin 24 is taken to earth by the AGC switch when set to LONG (as is pin 26).

8. When a break in the received transmission occurs, the corresponding reduction in the emitter current of TR1 causes the voltage level applied to pin 1 of ML4A to fall below the preset voltage level applied to pin 2 (of ML4A). The output from ML4A switches from negative to positive and capacitor C38 charges, via R58 and R59. Once the level of the exponentially-rising voltage at ML4B pin 7 exceeds the level of the fixed potential applied to ML4B pin 6 (approximately +5.5 V), the output of ML4B at pin 10 switches from positive to negative. TR11 conducts, the negative voltage applied to D9 is removed and TR5 conducts. The time-constant capacitors C16 and C22 discharge via R34 and TR5, and the AGC voltage output from ML3A falls exponentially to zero.

9. When the received transmission recommences, the emitter voltage of TR10 rises; the output of ML4A switches from positive to negative and C38 rapidly discharges via R58, D7 and the low impedance output circuit of ML4A. The output of ML4B switches from negative to positive, both TR11 and TR5 are cut off and the AGC voltage from TR7 charges the time constant capacitors, C16 and C22, via R33.

10. The operation of the hang detector circuit, as described above, and also where the duration of the break in the received signal is shorter than the hang time period, is shown in the timing diagram, Fig.12.1, (Chapter 12). For the reference 'ML3 pin 6' read 'ML4 pin 12'.

AM and SSB Detectors

11. The IF output from TR1 and the band-pass filter is coupled to a buffer stage TR6, via C13 and C15. The output from TR6, at TP4, is capacity coupled to both the AM detector, via C27, and the SSB detector, via C29.

12. The low distortion AM detector, TR9, is followed by a low-pass filter, L5, R49, C32. A similar filter follows the SSB detector, which consists of T1, D3 to D6, R53 and C3· The 1.4 MHz carrier signal is applied via board pin 5.

13. Diode switching, controlled by the MODE switch, is used to select the output from either the AM detector or the SSB detector. In the AM position of the MODE switch, an earth is applied to board pin 7. This is routed to D11 via R64; the diode becomes forward biased, and a path is opened for the output from the AM detector to the audio pre-amplifier via C37, D11 and C40. Diode D10 remains reverse biased, and isolates the output from the SSB detector.

14. For all remaining positions of the MODE switch, the earth is transferred to board pin 6. Diode D10 becomes forward biased and opens a path for the output from the SSB detector, whilst D11 becomes reverse biased and isolates the output from the AM detector.

Audio Pre-Amplifier

15. The output from the selected detector is applied to a high gain, impedance matching amplifier, TR12, TR13. The output, which is applied to the MODE switch and the preset line level control, via C41 and board pin 8, is muted by transistor TR14 when an earth is applied to board pin 10.

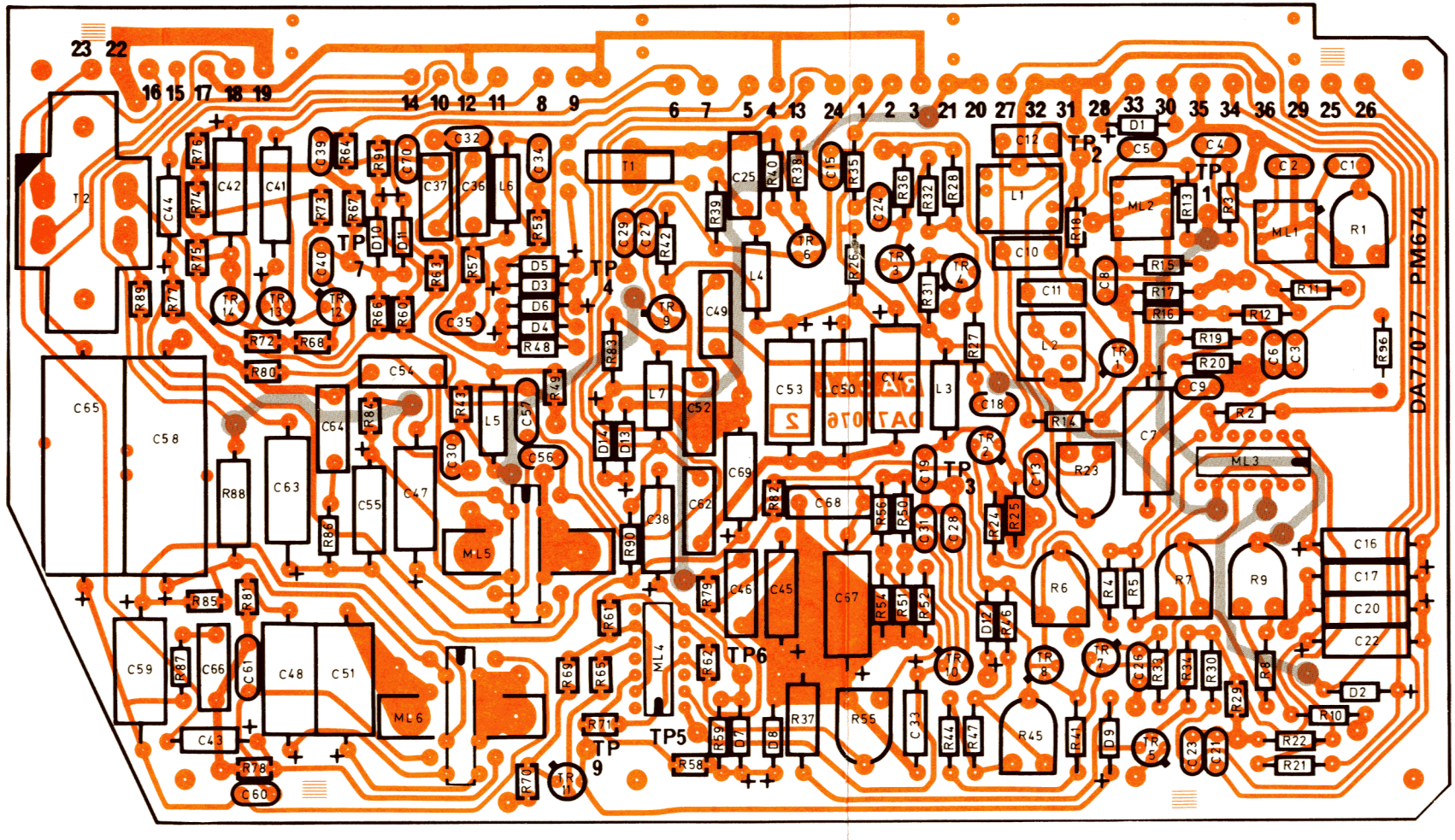
Audio Line Amplifier

16. The audio line amplifier consists of an integrated circuit linear amplifier, ML5 and associated components. The input signal, from the preset line level control, is applied to ML5 via board pin 11 and C44. The audio line output is taken to the rear panel terminals via transformer T2 and board pins 15 and 16.

Loudspeaker Amplifier

17. In SSB versions of the receiver, the output of the audio pre-amplifier, at board pin 8, is routed to the loudspeaker amplifier via the front panel AF GAIN control and board pin 23. For ISB versions only, the input to the loudspeaker amplifier is switched (MODE switch) to receiver either the pre-amplifier output from the main IF board (USB) or that from the ISB IF board (LSB).

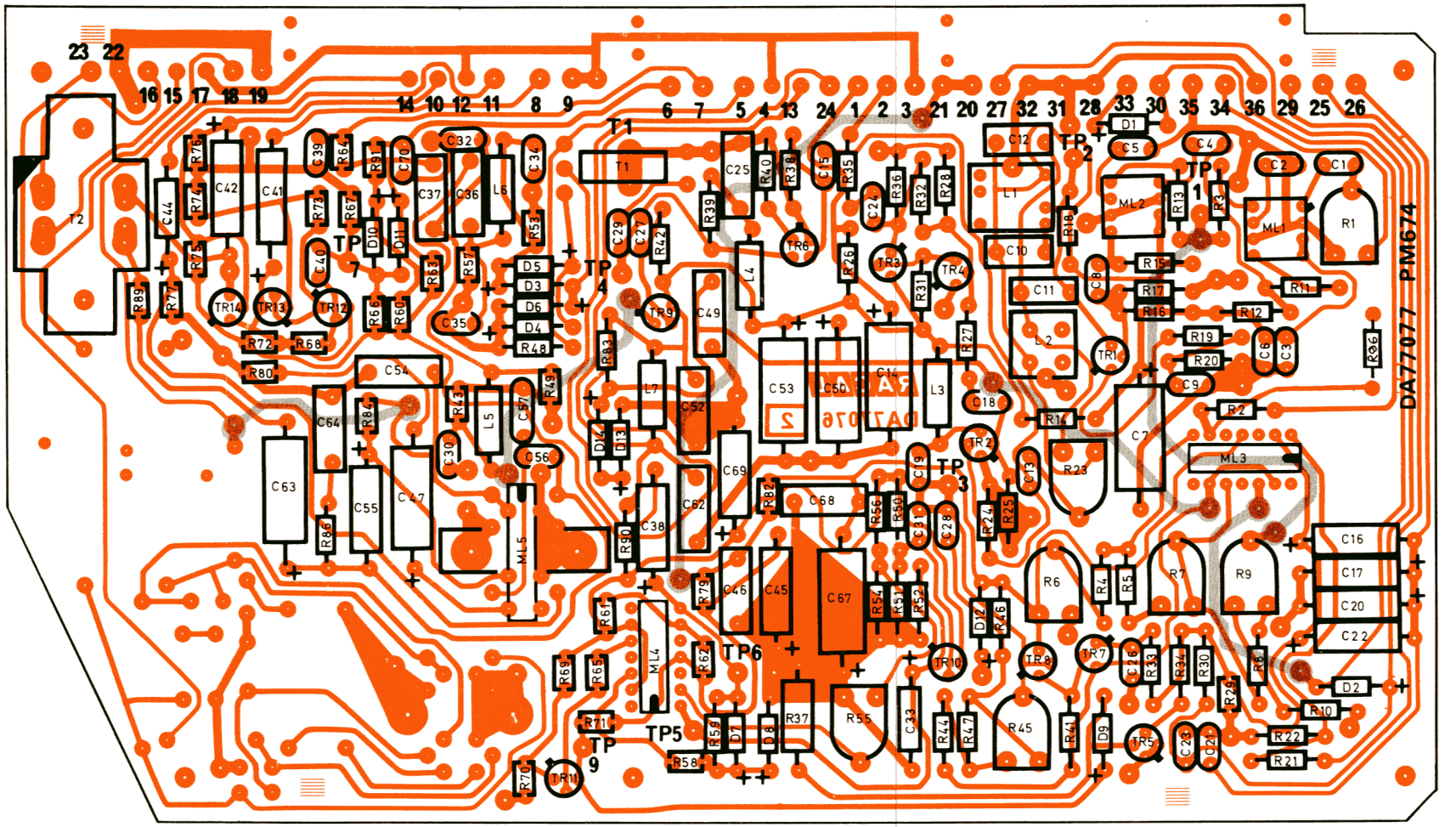
18. The loudspeaker amplifier consists of an integrated circuit amplifier, ML6 and its associated components. The amplifier output, at board pin 18, is taken direct to the rear panel loudspeaker terminal and the internal loudspeaker, and via a dropper resistor to the headphone socket.



RACAL
TH3004 | DA77077/A

Layout: Main IF/AF Board PM674/1

Fig. 12A.1



RACAL

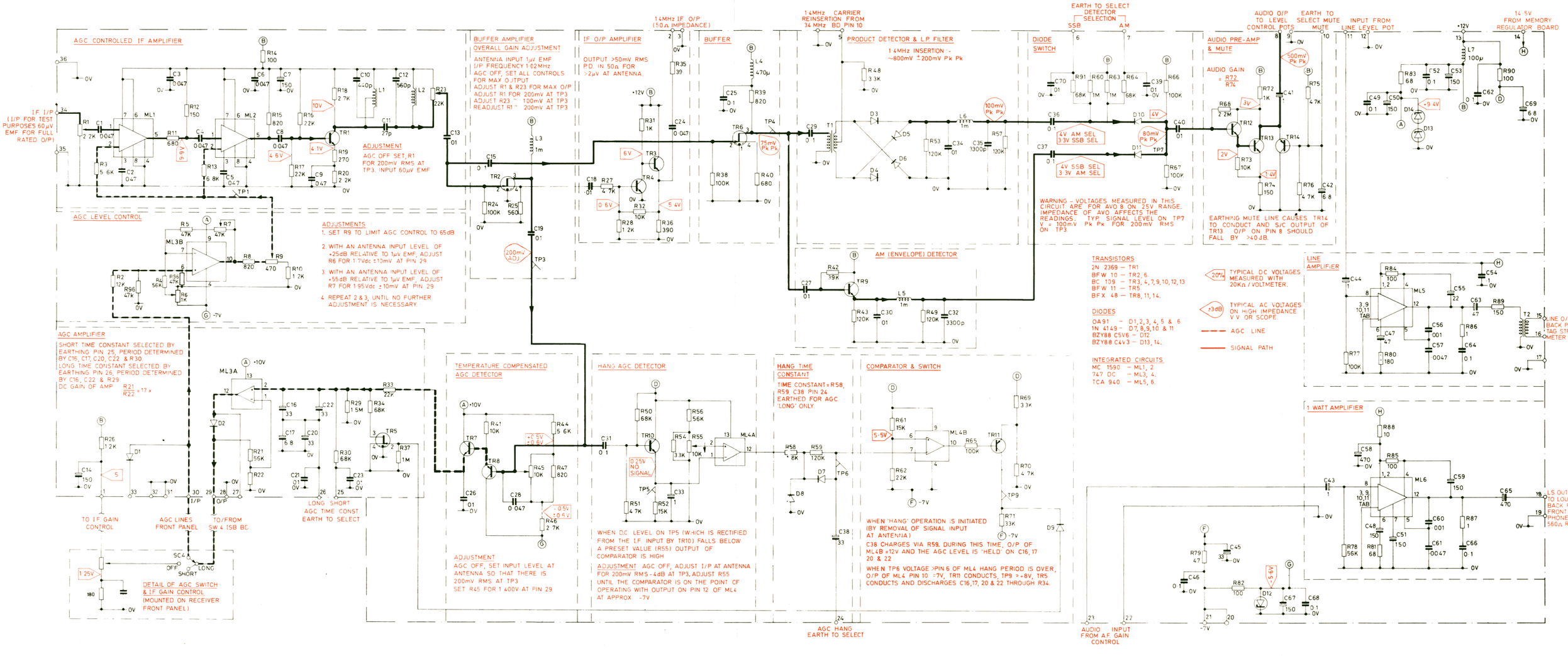
TH3004 | DA77077

Layout: ISB IF/AF Board PM674/2

Fig. 12A.2

Jan. 82 (Amdt. 5)

Jan. 82 (Amdt. 5)



RACAL
TH 3004 DC 77077
2 6

Circuit : IF/AF Board PM474

Fig. 12A.3

Jan 82 (Amdt 5)

CHAPTER 13

SHAFT ENCODER

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CHAPTER 13

SHAFT ENCODER

INTRODUCTION

1. The encoder produces two squarewave signals with a phase difference of 90°. The direction of turning is indicated by which waveform is "leading" the other. A circuit diagram and the layout of the encoder is given at the end of this Chapter.

Operation

2. The dark lines on the encoder disc break the optical circuit between the l.e.d. and the phototransistor. When the knob is turned the waveform at the output of the phototransistors is a sinewave.

3. This sinewave is converted to a squarewave by the first two comparators (R4 and R5 set the mark/space ratio to unity).

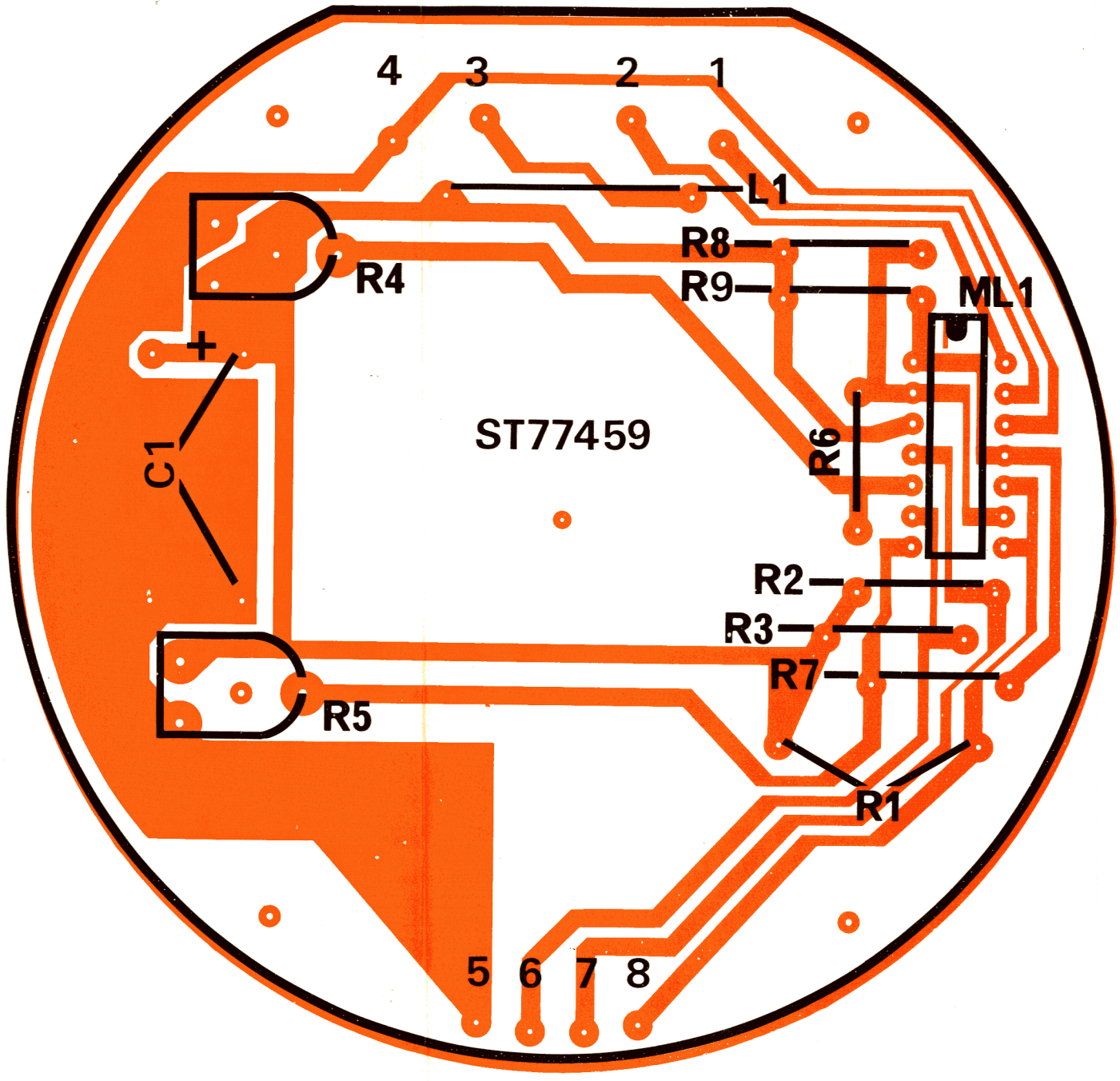
4. The resulting squarewave is used to drive the output comparators which provide an open-collector output to drive the display board. The forward voltage of the l.e.d's provides a fixed reference voltage for the output comparators.

5. The output voltage swing is 0 to +5.5V (pull-up resistors are on the display board).

6. The encoder shaft is damped by pressure from a felt pad and the amount of damping may be varied by means of the mechanical damping adjuster screw on the potentiometer board.

Adjustments

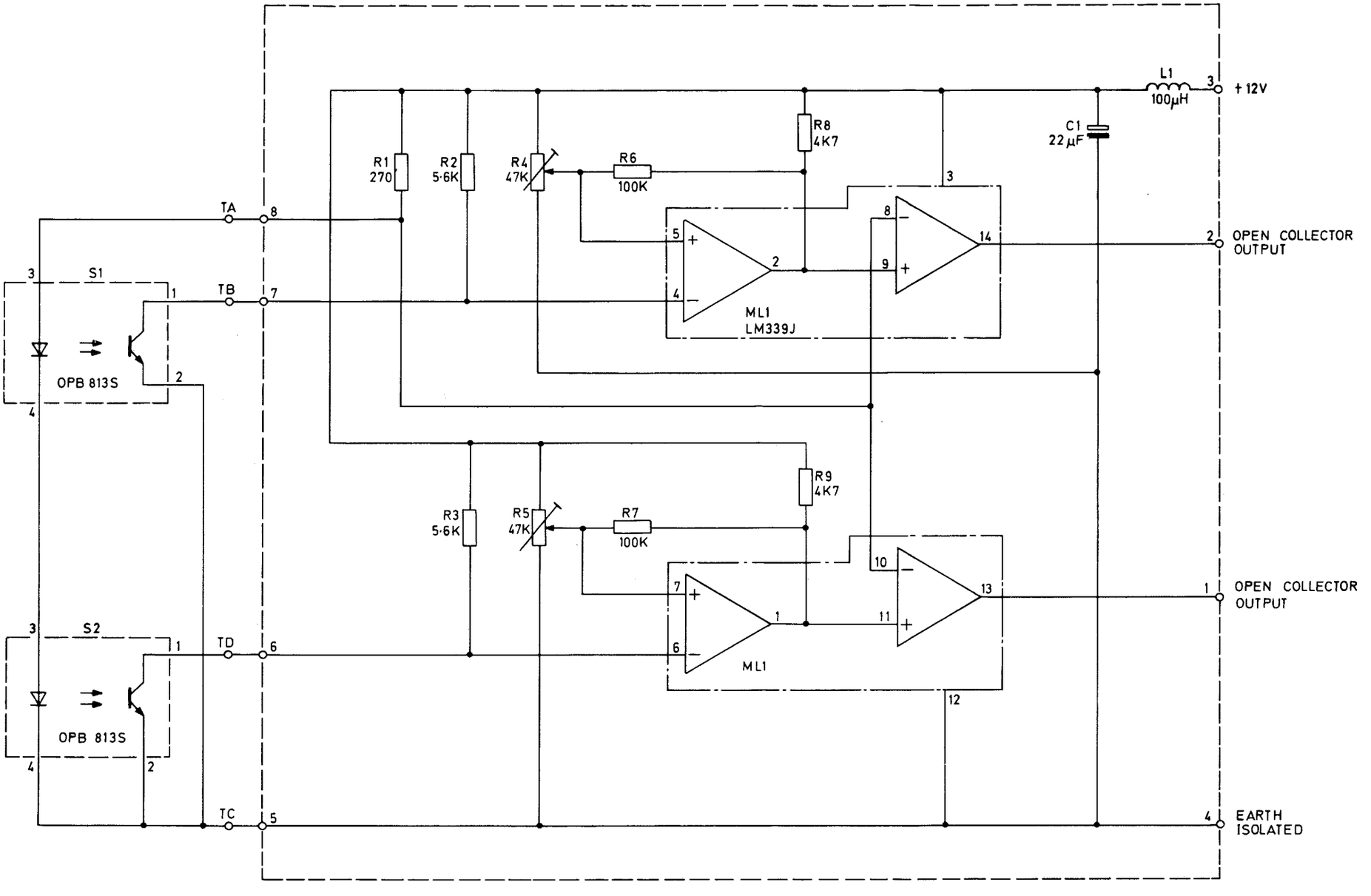
7. Refer to Chapter 23, paragraphs 13 to 15, for details of adjustments to the shaft encoder.



RACAL

WOH 7049	CA77458 / 3	13·1
1		1/2
WOH 7049	CA77458 / 2	13·1
1		2/2

Layout: Optical Shaft Encoder Fig. 13·1



RACAL

WOH 7049	CC77459
2	

Circuit : Frequency Optical Shaft Encoder

Fig. 13·2

CHAPTER 14

DISPLAY BOARD PM692

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CHAPTER 14

DISPLAY BOARD PM692

INTRODUCTION

1. The display board accommodates the digital frequency display, an interface with the shaft encoder and an out-of-lock indicator. A circuit diagram of the board is given at the end of this Chapter Figure 14.3.

Shaft Encoder Interface

2. The shaft encoder output (which is a square wave of 5V p-p) is applied to the x4 pulse multiplier and (after buffering) to the UP/DOWN line generator.

3. The output of the pulse multiplier is applied to the clock pulse generator monostable (ML3b) via an inverter. The monostable produces pulses of 5 - 20 μs duration.

4. If the D input of ML3b is held at '0', no clock pulses will be produced. This happends when the output of the clarifier rate inhibit circuit is zero - see table in Figure 35.

5. The generation of clock UP/DOWN pulses is shown in Figure 13.1.

Display

6. The display consists of seven light emitting diode display digits. The "latch" facility is not used, so that the digit displayed corresponds to the BCD input data.

7. The displays may be blanked by applying a '1' to pin 4. This may be done either to switch off all the displays - option 1 on memory board - in the "Channel" mode or to blank leading zeros on the MHz digits.

8. Blanking of the five least significant digits is done by a '1' on pin 41 (TR1 acts as a buffer) while the blanking of the MHz digits is done by ML12, ML13 (with TR2 and TR3 as buffers) in accordance with the table given on the circuit diagram, Figure 35 in Part 2 of the handbook.

Range Blanking

9. Whenever the 10 kHz digit changes G13 produces a 15-40ms pulse (Chapter 23, Appendix B) which is applied to the PM589 synthesis board. TR4 provides a TTL compatible output.

Pulse Doubler

10. G14 doubles the number of clock pulses for use on the MEDIUM tuning rate (Chapter 23, Appendix B).

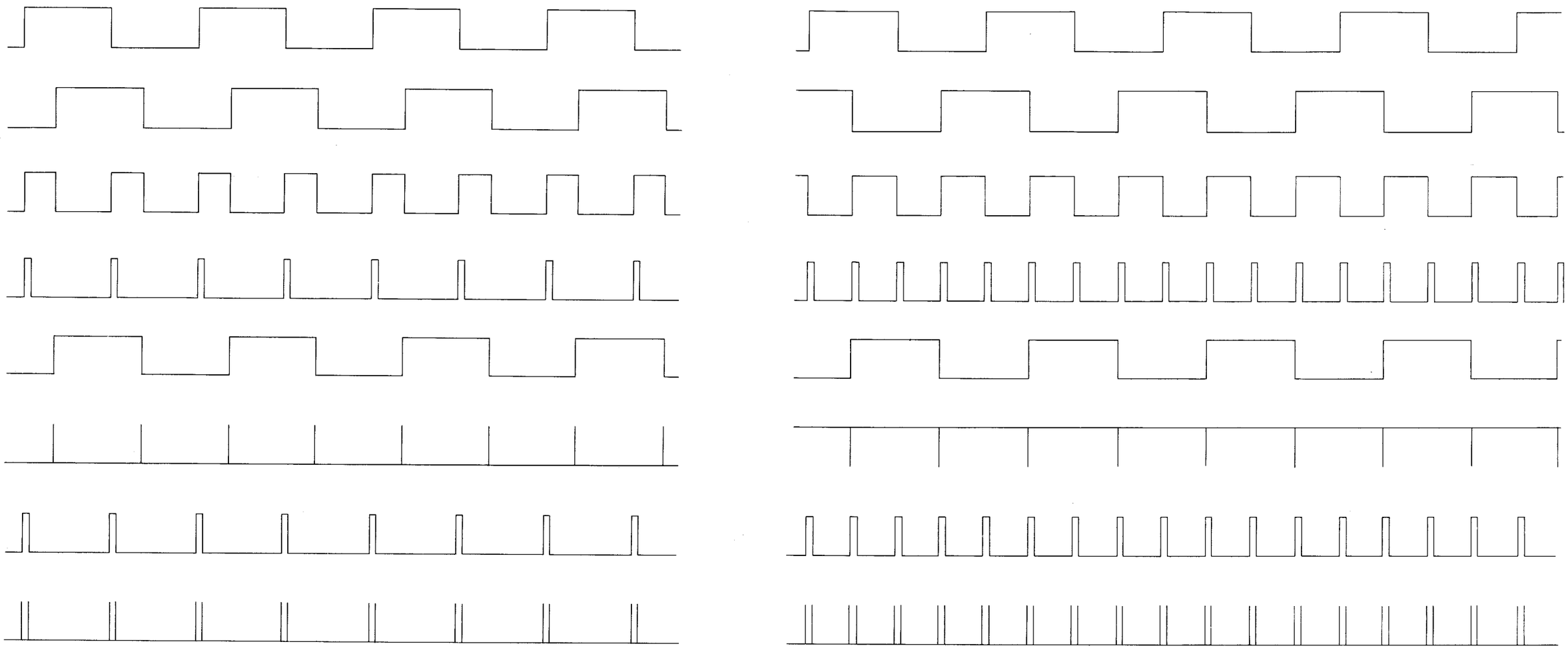
Out-of-Lock Circuit

11. The out-of-lock (OOL) inputs from the synthesiser are combined by diodes D3, D4 and D5. Any input that is '0' or pulsed is an indication that the relevant circuit is OOL and will light the OOL lamp by applying a '0' to the base of TR5.

12. To ensure that the OOL lamp remains off during tuning, the monostable ML4 produces pulses which hold TR5 off. At most normal turning rates, the output of ML4 will be a continuous '1' so the lamp will be permanently off while tuning takes place.

Power Supplies

13. The display circuits are fed from the +5V regulator on the AF and display regulator board.



COUNT DOWN

COUNT UP

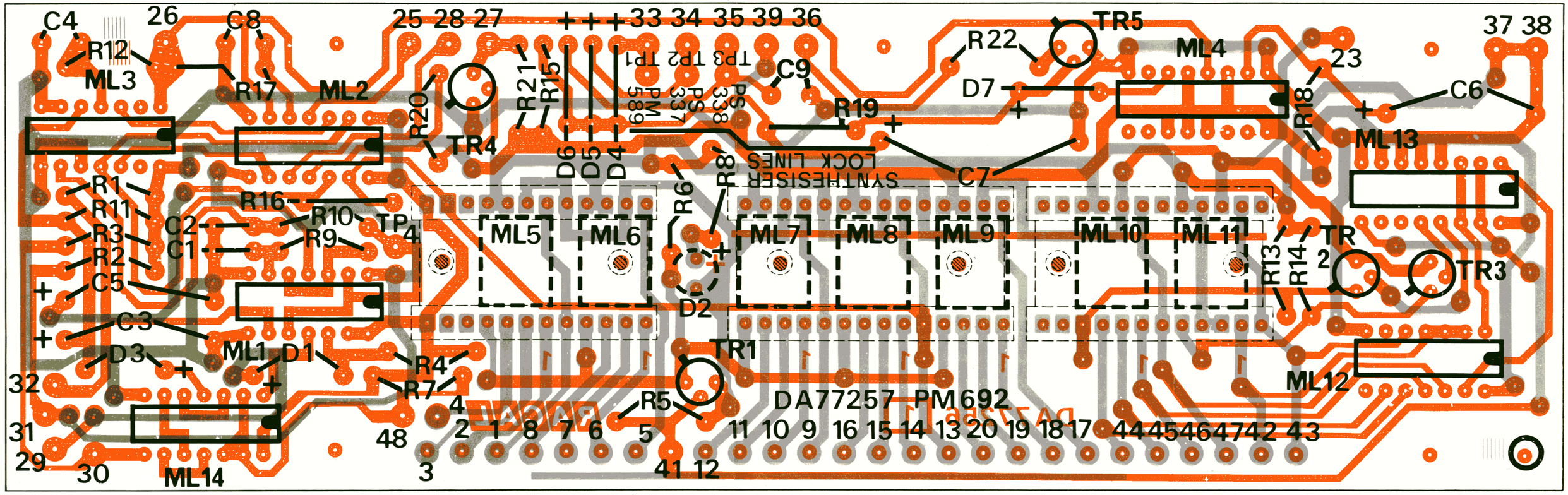
NOTE : 1. THIS DIAGRAM INDICATES THE TIMING OF THE WAVEFORMS ; WHEN DISPLAYED ON AN OSCILLOSCOPE THEY WILL DIFFER IN DETAIL FROM THOSE SHOWN.

2. PULSES ARE PRODUCED AT THE OUTPUT OF G10 BECAUSE THE EDGES OF THE WAVEFORM AT Q/ML3a AND ENCODER A DO NOT OCCUR AT EXACTLY THE SAME INSTANT (DUE TO THE DELAY IN ML3a/G10) THESE PULSES DO NOT AFFECT THE UP/DOWN COUNTING WHICH TAKES PLACE ON THE RISING EDGE OF CK1 OR CK2, AT WHICH TIME THE UP/DOWN LINE IS IN THE CORRECT STATE.

3. AS THE D INPUT OF ML3a IS DELAYED, THE INFORMATION CLOCKED INTO ML3a BY THE RISING EDGE OF G7 OUTPUT IS THAT PRIOR TO THE CHANGE IN A OR B WHICH CAUSED THE PULSE

Timing Diagram : Generation of Clock and Up/Down Pulses

Fig.14·1

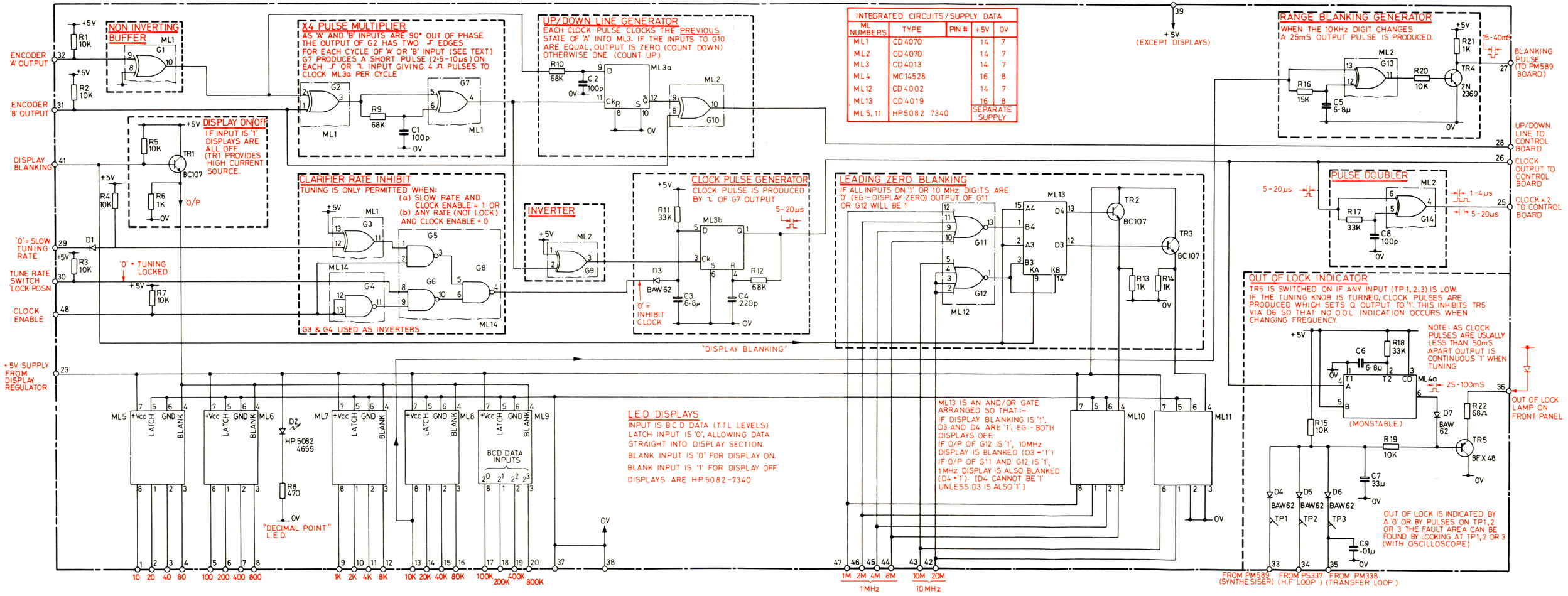


RACAL

WOH 7049	DA 77257	1/3	WOH 7049	DA 77255	3/3	WOH 7
1			1			1

Layout : Display Board
PM 692

Fig. 14.2



RACAL
WOH 7049 | DC 77257

Circuit: Display Board PM 692 Fig. 14·3

CHAPTER 15

DECODER BOARD PM694

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WARNING BEFORE WORKING ON THE DECODER BOARD PM694 OR THE MEMORY BOARD PM693 THE BATTERY MUST BE DISCONNECTED BY REMOVING THE BATTERY LINK ON THE DECODER BOARD PM694. FAILURE TO DO SO MAY RESULT IN DAMAGE CAUSED BY SHORTING POWERED CIRCUITRY TO GROUND.
DISCONNECTION OF THE BATTERY MAY RESULT IN THE LOSS OF STORED FREQUENCY INFORMATION.

CHAPTER 15

DECODER BOARD PM694

INTRODUCTION

1. The decoder board decodes the memory address from the CHANNEL switch position and the necessary control functions from the MHz Data. The circuit diagram of the board is given at the end of this Chapter Figure 15.2.

Memory Address Decoder

2. The selected channel number is indicated by a '0' on the appropriate line from the switch. This will produce an output suitable to drive the memory as indicated on the circuit diagram truth table.

Nines Complement Convertor

3. The MHz data is converted to 9's complement (truth table given on circuit diagram), buffered by the TTL buffer gates ML1, 3 and used to drive the HF loop (PS337) and Transfer loop (PM338) boards.

RF Board Filter Selection

4. The relays on the RF board are energised by transistors TR1 and TR2 and the TTL BCD-decimal open collector decoder ML14 decoder 7445. The 0-7 MHz control is provided by ML14, with the outputs joined in parallel where required.

5. When the MHz data is 8 MHz and above, the '1' applied to the D input of the decoder ensures that none of the 0-7 outputs can be selected.

6. The gates of ML4, ML5 and ML6 decode the 8-15 and 16-29 ranges and their outputs operate the relay drivers TR1 and TR2.

First Mixer Notch Filter Selection

7. The gates select which transistor, TR3 or TR4, is switched on; this transistor selects the appropriate notch filter on the first mixer board.

HF Oscillator Selection

8. Applying a '0' to one of the oscillator select inputs of the HF loop board switches on the appropriate oscillator. The transistors provide an open collector output from the decoding gates.

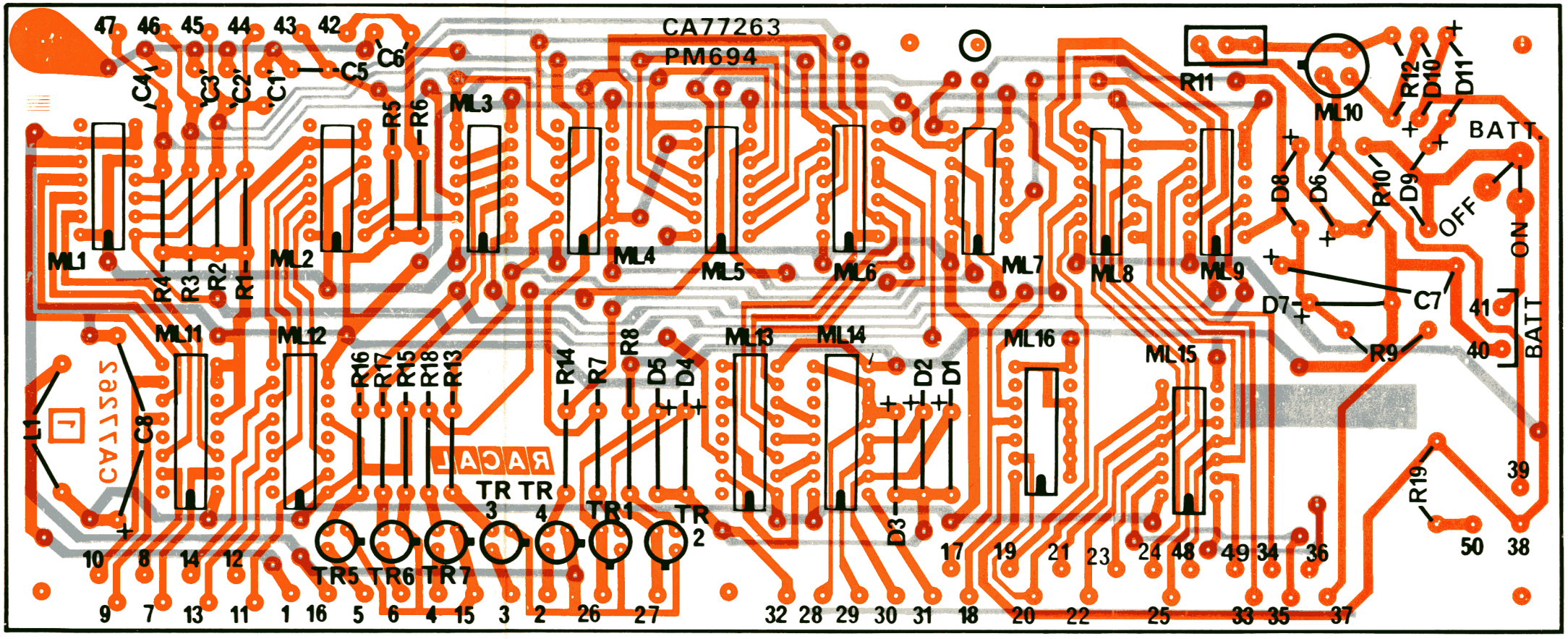
9. If the LO INT/EXT switch on the rear panel is set to EXT, no transistor can conduct (as all the emitters are at 5 μV so that no oscillator is selected.

Power Supply

10. The circuits which are supported by the internal rechargeable battery are fed from a separate power supply ML10.

11. The output of the IC regulator is fed through diode D10 (which prevents reverse current flowing when the battery supply is in use) to combine with the output of the battery. The diodes D9 and D11 in series with the battery ensure that the current from the regulator does not flow into the battery.

12. The standby battery input is used if long term storage is required (longer than the life of the internal battery). The input may take any voltage between 9V and 40V and maintain the memory (12V or 24V nominal battery - current drain 2-20 mA depending on voltage).



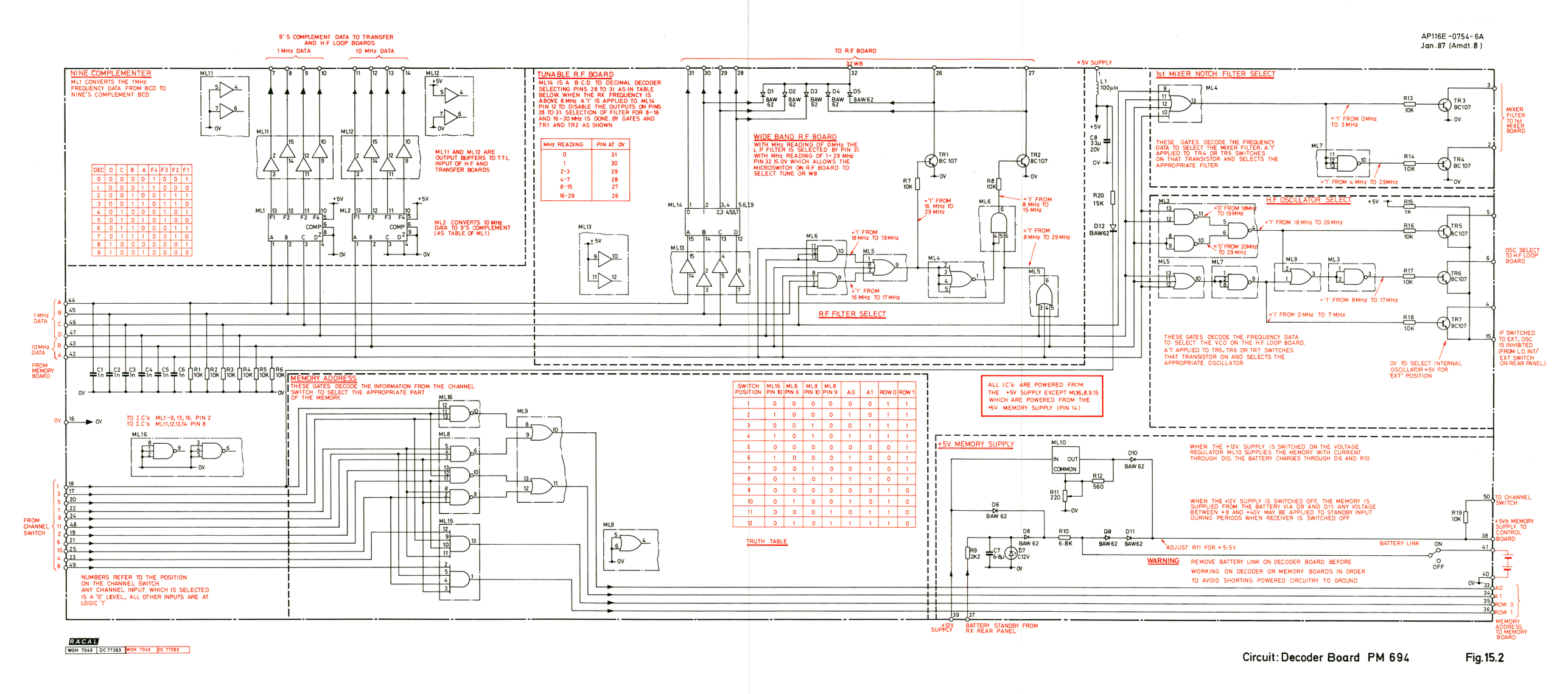
WOH 7049	CD77261/3	3/3
1		

WOH 7049	CD77261/2	2/3
1		

RACAL

WOH 7049	CD77261/4	1/3
1		

Layout : Decoder Board PM 694 Fig. 15.1



DEC | D | C | B | A | F4 | F3 | F2 | F1
0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1
1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0
2 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1
3 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0
4 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1
5 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0
6 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1
7 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0
8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1
9 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0

RACAL
WOH 7049 | DC 77263 | WOH 7049 | DC 77263

Circuit: Decoder Board PM 694 Fig.15.2

CHAPTER 16

MEMORY BOARD PM693

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Circuit: Memory board PM693	16.2

CHAPTER 16

MEMORY BOARD PM693

INTRODUCTION

1. The memory board consists of up-down counters and memory circuits for producing the frequency setting and storing it in one of 12 channels. A circuit diagram of the board is given at the end of this Chapter Figure 16.2.

Operation

2. The signals from the shaft encoder, after conversion to UP/DOWN and clock pulses on the display board, are used to drive the UP/DOWN counter.

3. The clock pulse selector selects the output of the pulse doubler on the display board whenever the tune rate is set to MEDIUM. This effectively applies two clock pulses for every step, producing the 20 Hz per step rate.

4. The clock pulses now have to pass through the clock gate G8. G8 is open when the output of G7 is '1'. This occurs when:

   (a) The MEMORY switch is set to TUNE .

   or

   (b) The MEMORY switch is set to CHANNEL and the output of the clarifier control circuit is '0', indicating that tuning has not exceeded the ±500 Hz tuning range.

5. Having passed through the clock gate the clock pulses are used to drive all the UP/DOWN counters and the divide-by-ten circuit. For every 10 input pulses, the counter goes to '0'. When the SLOW tuning rate is selected, the output of G12 will only go to '1' when Co is '0'. The Co input of the first UP/DOWN stage is, therefore, only '0' (enable) every 10 clock pulses in the SLOW rate. When MEDIUM or FAST rates are selected the output of G12 is always '1' enabling the first UP/DOWN counter. Thus the tuning rate in the MEDIUM and FAST is 10 times that in the SLOW mode.

6. The operation of the UP/DOWN counters is described both on the circuit diagram and in Chapter 23, Appendix B.

7. The function of gates G14, G21, G22 and G23 is to reset the least significant digits (10 Hz and 100 Hz) to zero when FAST tuning is selected and to enable ML21 so that counting is in 1 kHz steps in this mode.

8. The operation of the 10 MHz UP/DOWN counter is complicated by the need to operate on only 0, 1 and 2.

9. The outputs of the UP/DOWN counters (Q) are connected to the BIT inputs of the memory circuits. The inputs of the UP/DOWN counter (P) are connected to the BIT outputs of the memory circuits.

10. The memories are selected by three lines; Ao, Ai and CHIP SELECT. Ao and Ai are output by the decoder board and CHIP SELECT is derived from the two ROW lines from the decoder board. Ao, Ai and the ROW lines are set by the decoder board according to information from the CHANNEL switch.

11. Whenever the CHANNEL switch position is changed, a pulse will be produced by G17 and lengthened into a Read pulse by ML5.

12. This Read pulse is applied to the OR gate (G13 and G19) and hence to the Pe input of the UP/DOWN counters. (The other input to G18 produces a Read pulse after completing a Write cycle - giving an indication of what is stored).

13. When a '1' Read pulse is applied to the Pe input of the UP/DOWN counters, the data on the 'P' inputs (which is the contents of the selected memory channel) will be transferred to the Q output and hence to the synthesizer and digital display.

14. To LOAD a new frequency into a channel, a Write pulse is applied to the Write input of the memory circuits. This transfers the data at the output of the UP/DOWN counter (e.g. the frequency to which the receiver is set) into the memory channel selected by the channel switch.

15. The Write pulse is generated by ML5 when the memory key is turned to the spring-loaded LOAD position. This triggers ML5 (monostable) which produces a Write pulse, while G20 generates a "check" Read pulse at the end of the Write pulse.

16. The operation of the 10 MHz counter (which does not have a Pe input) is described on the circuit diagram.

17. The display on/off switch switches off the display when the memory key is set to CHANNEL mode in the OPTION 1 position of the link. For OPTION 11 the display remains ON all the time.

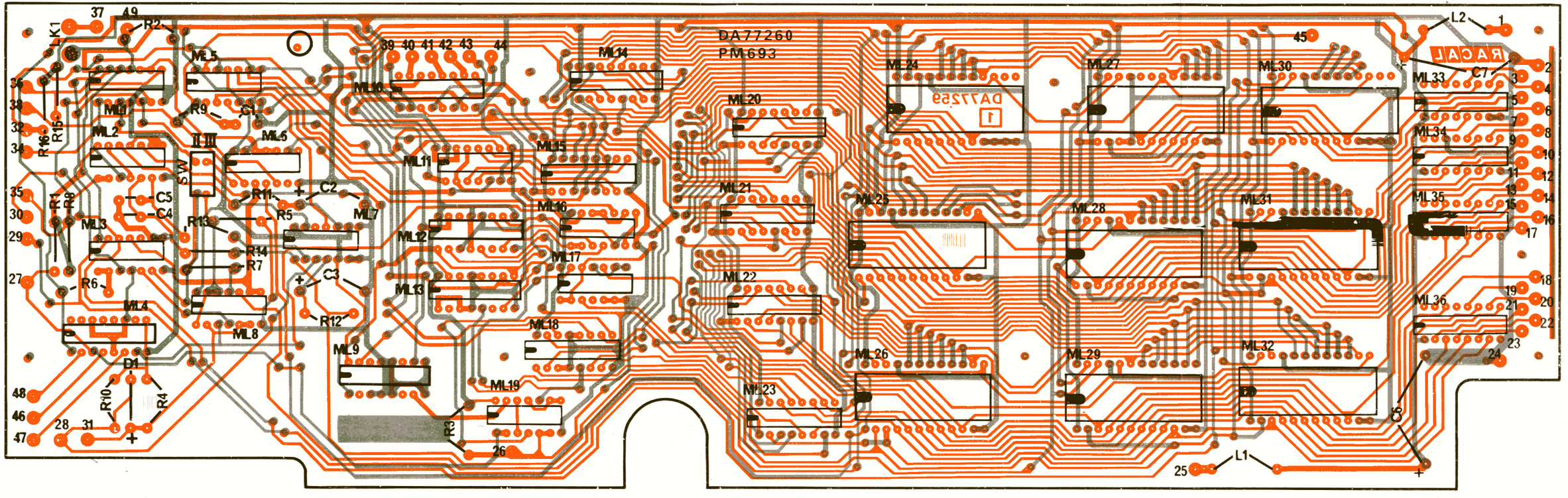
Power Off Storage

18. The board has two supplies for +5V. One of these drives the output buffers (type 4050) which drive the (relatively) high current TTL loads of the synthesizer and display. This is referred to as +5Vs, and when the receiver is switched off this supply falls to zero.

19. The other supply (+5Vb) is derived from two sources on the decoder board. When the receiver is switched on, a separate regulator on the decoder board provides +5.5V to this line, but when the receiver is switched off, the voltage is derived directly from the battery (approx. 4-5V).

20. Thus, when the a.c. supply fails, the battery will supply current to all the circuitry on the memory board (so maintaining the stored information) but the TTL buffers are not powered so that no current flows from the battery into the high current TTL circuits. This reduces the battery current to a few microamps.

21. To prevent discharging of the battery by R1, R3 or R6 the wiper of the tune rate switch is connected to ground via a transmission gate. When the a.c. supply is on, the input to G31 is '1' and the transmission gate is switched on, earthing the wiper of the rate switch. When the a.c. supply fails, the input of G31 is '0' which open-circuits the output of the transmission gate and the wiper of the switch. Thus no current can flow through R1, R3 or R6 whatever the switch setting.



RACAL

WOH 7049	DD77258/4	1/3
1		

WOH 7049	DD77258/5	2/3
1		

WOH 7049	DD77258/3	3/3
1		

Layout: Memory Board PM 693 Fig. 16.1

AP116E -0754-6A

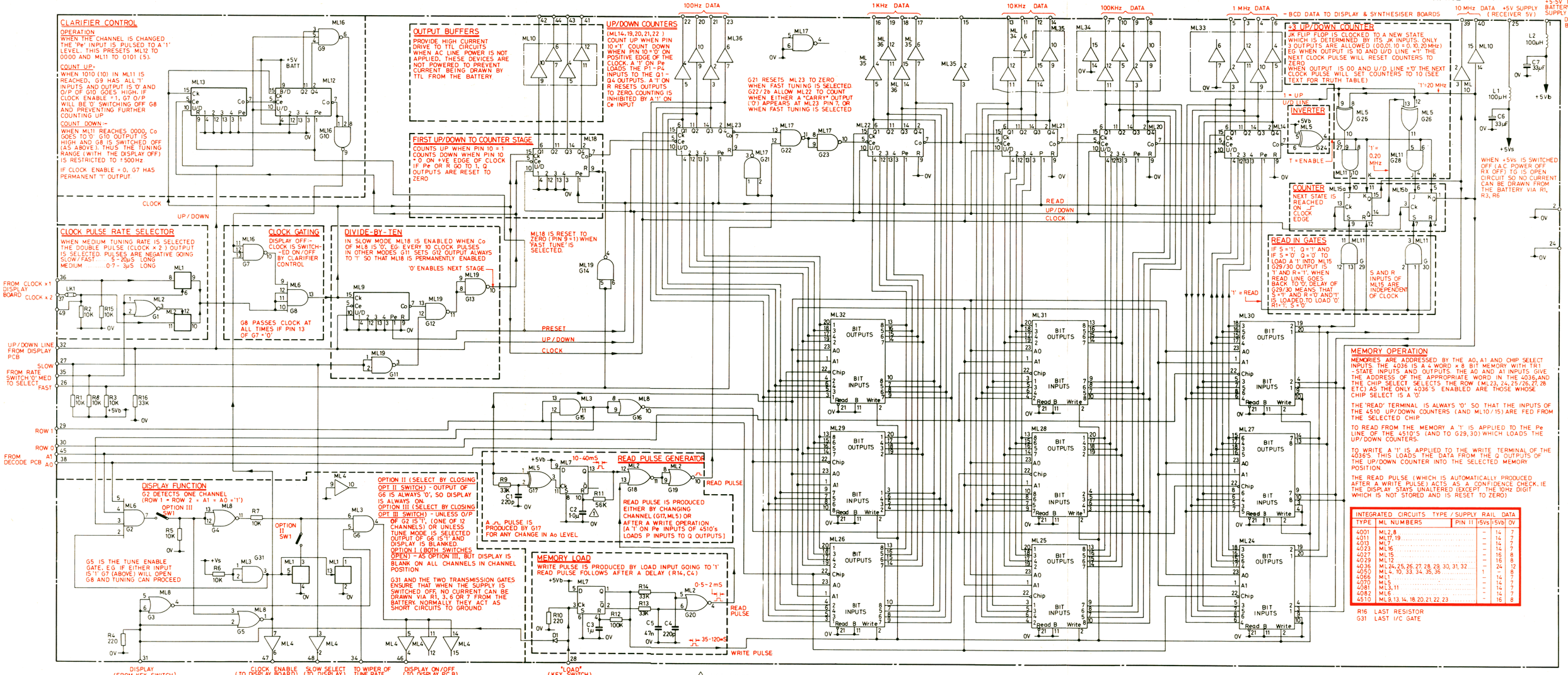


Fig.16.2

June 81(Amdt.4)

Circuit: Control & Memory Board PM693

Fig.16.2