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Colin Hinson

In the village of Blunham, Bedfordshire, UK.

PG52 MODULAR PULSE GENERATOR SYSTEM

Instruction Manual

Including the Main Frames PG52 PG52A and PG52B

ADVANCE

PG52 MODULAR PULSE GENERATOR SYSTEM

Instruction Manual

Including the Main Frames PG52 PG52A and PG52B

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Contents

Introduction

Section 1

The PG52 Pulse Generator is completely modular in construction, a system being assembled from the wide range of signal generating and processing units available, to produce the desired output waveform. Repetition frequencies up to 30 MHz and pulse widths down to 10nS can be obtained from this system and its versatility enables the production of innumerable complex pulse and ramp waveforms not obtainable from conventional pulse generators.

Different output modules will deliver up to 50V into 50Ω with a 10nS rise time, 10V into 50Ω with a 5nS rise time or 5V into 50Ω with a 1nS rise time. Another will provide 10V into 50Ω with variable rise and fall times.

The full flexibility of the system is obtained by driving this range of output modules from the clock, width or delay, gate or word generator waveform processing modules, to construct an unlimited range of pulse or ramp waveforms.

The modulation facility available for frequency, width or delay and output amplitude allows the system to be operated by remote control.

The plug-in units are all self-contained and require only d.c. power supplies, which are obtained from the main frame. Signal paths are made externally, through BNC/BNC connectors, to ensure maximum flexibility in interconnection. All such interconnecting signals are at a common interface level. The majority of functions are selected by push buttons, resulting in particularly convenient operation. While the main frame will take up to 8 modules, two or more frames can operate together to form the more complex systems.

The output modules and all interconnecting signals are protected against damage due to short circuit and all units use silicon transistors throughout, the clock and word generators also using integrated circuits, to ensure the maximum reliability in use.

In common with any modular system, the PG52 can be extended by the purchase of further modules as applications arise or as new modules offering additional performance become available.

2.1 SYSTEM

All modules are 2" in width and the main frame can contain up to 8 of these. The one exception is the PG52 P6 Power Output Module which is 4" wide, equivalent to two other modules.

The system consists of the following parts:–

		Earlier Version (see section 2.4)
PG52B M.F.	Case with integral power supplies	PG52 PG52A

Waveform generating or processing modules

PG52 P1A	Clock Generator Module	PG52 P1
PG52 P2A	Pulse Width or Delay Module	PG52 P2
PG52 P8	Word Generator Module	
PG52 P9	Gate Module	
PG52 P10	Trigger Module	
PG52 P12	Modulated Width or Delay Module	

Output Modules

PG52 P3A	Standard Output Module	PG52 P3
PG52 P4A	Variable Slope Module	PG52 P4
PG52 P6	Power Output Module	
PG52 P7	Fast Output Module	
PG52 P13	Modulated Output Module	

Accessories

PG52 P0	Blank Panel
PG52 P5	Passive Summing Module
PL 85	Summing Coupler
PL 81	7" BNC-BNC Connecting Lead
PL 43	BNC-BNC Connecting Lead
PL 39	Supply Lead (PG52 & PG52/A)
PL 86	" " (PG52/B)
TP 19	50Ω 2W BNC Termination
TP 21	50Ω 50W BNC Termination
PN 30163	Main Frame Instruction Manual
PN 30111	P1,P1A " "
PN 30112	P2, P2A, P12 " "
PN 30113	P3, P3A, P13 " "
PN 30114	P4, P4A " "
PN 30115	P6 " "
PN 30116	P7 " "
PN 30117	P8 " "
PN 30118	P9 " "
PN 30119	P10 " "

In addition to the relevant handbooks, each main frame is supplied with:–

1	PL 39 (PG52 or PG52A) or PL 86 (PG52B)
8	PL 81
2	PL 43

Each P3 and P4 module is supplied with

1	TP 19

Each P6 module is supplied with

1	TP 21

Each P7 module is supplied with

2	TP 19

A standard system consists of the following modules:

1	PG 52B	Main Frame
1	PG 52 P1A	Clock Generator
3	PG 52 P2A	Pulse Width or Delay Modules
2	PG 52 P3A	Standard Output Module
1	PG 52 P4A	Variable Slope Output Module
1	PG 52 P5	Passive Summing Unit

However, many applications will require a different complement of modules. The required complement should be specified when ordering and additional modules and accessories can be supplied on request.

Operating Temperature Range

0 to 40°C

All Modules are calibrated at approx. 20°C.

Approx. de-rating of frequency and time calibration where appropriate is 0.1% per °C.

2.2 MAIN FRAME

The PG52B Main Frame contains all the necessary power supplies to operate a full complement of any eight modules. Each module is retained in place by two captive screws and draws its power from the main frame via a printed circuit edge connector.

The Main Frame is the correct width for rack mounting and adaptors are available as optional extras if required.

POWER SUPPLY

100 to 130 or 200 to 260V
45 to 60Hz

Consumption depends on plug-in unit complement, typically 60VA. Maximum 150VA without P6 module 200VA with one P6 module.

DIMENSIONS

	17 in (430 mm) wide 8¾ in (223 mm) high 18½ in (470 mm) deep including handles.
Weight:	approx. 28 lbs. (12.8 Kg.) excluding modules. typically 45 lbs (20 Kg.) with 8 modules not including PG52 P6

The PG52 and PG52A main frames are identical to the PG52B in specification with the exceptions covered in Section 2.4.

2.3 BRIEF DESCRIPTION OF MODULES

For the full specification of each module, see the relevant section of the handbook.

PG52 P1 or P1A **Clock Generator**

This module provides the basic clock rates for the system. It covers the frequency range 0.1Hz to 30MHz in free-running, externally triggered or gated

modes. The trigger mode may also be triggered manually for single shot applications, or used as an aperiodic ÷ 10 or ÷ 100 count-down. A sweep facility alternatively allows the internal frequency to be controlled over any selected 10:1 range by an external input.

PG52 P2 or P2A **Pulse Width or Delay Generator**

This module is a variable pulse width generator, typically driven from a clock generator to determine the width of an output pulse or interposed between the clock generator and another PWD generator, to provide a delay between the clock and output pulses. It covers the range 25nS to 1Sec and while it is intended to be driven from a clock or any other system interface signal, the input trigger level can be varied to suit direct operation from other signal sources.

PG52 P3 or P3A **Standard Output Module**

This module provides outputs into 50Ω with rise and fall times typically 5nS. The positive and negative levels of the output pulse may be varied independently over the range 0 to +10V and 0 to -10V respectively. (i.e. 20V pk/pk). Attenuated ranges allow those levels to be reduced successively from 10V to 100mV.

A pulse invert facility allows both the generation of negative pulses and output duty cycles approaching 100%. The two input sockets allow the generation of output pulses from two independent sources.

PG52 P4 or P4A **Variable Slope Output Unit**

In addition to the independent 0 to +10V and 0 to -10V output level controls of the P3 module, this module has rise and fall rates adjustable from 1nS/V to 100mS/V with independent 10:1 controls for the positive and negative going edges. 20V signals can be generated into 50Ω with any slope from a 2 second ramp to a 20nS rise time.

Its dual input and invert facilities are similar to the P3.

PG52 P5 **Passive Summing Unit**

This module contains two independent resistive networks, one with two inputs and the other with three inputs which allow the analogue summation of pulses of different shape, amplitude or offset, but with some attenuation.

PG52 P6 **Power Output Module**

This module provides positive or negative voltage outputs of up to 50V into 50Ω. It has an unlimited duty cycle giving a maximum output power of 50W. It contains its own power supplies driven directly through the main frame from the incoming AC supply. It has dual input and invert facilities similar to the P3 module.

PG52 P7 **Fast Output Module**

This module provides simultaneous positive and negative output pulses of up to 5V into 50Ω with rise times of 1nS. A variable delayed start facility allows the generation of output pulse widths down to 10nS despite the minimum pulse width capability of 25nS of the P2 module. It also has a dual input facility.

PG52 P8 **Word Generator**

This module generates pulse patterns of up to 16 bits in length and can operate in a continuous or externally triggered cycle mode. The output can be switched to be in a non-return-to-zero form or, via a P2 module, in a return-to-zero form. A synchronising output signal is provided at the end of the word to allow modules to be encoded to extend the word length beyond 16 bits.

PG52 P9 **Gate Module**

This module contains two independent four input "OR" gates with the facility to invert any input or output. This flexibility allows the simulation of pulse addition, pulse blanking, set/reset bistables etc. and is invaluable in the build-up of complex pulse waveforms.

PG52 P10 **Trigger Module**

This multi purpose module provides more flexible facilities for triggering the system from external signals or from the internal 50Hz (60Hz) supply frequency. It has a slope and level selection control with a sensitivity of 500mV. In addition to the normal interface signal output it has an independent prepulse output of 1V into 50Ω and width variable from 25 to 200nS. A further ÷ 2 aperiodic count-down allows the generation of a 1:1 square wave at any frequency.

PG52 P12 **Modulated Width or Delay Module**

This module is similar to the P2A module but in place of the variable trigger lever facility, it allows an externally applied voltage to control the output pulse width over a 10:1 range, over-riding the function of the fine period controls.

PG52 P13 **Modulated Output Module**

This module is similar to the P3A module, but with only one pulse input facility. An externally applied signal can be switched to control the positive output level from 0 to +10V, or the negative level from 0 to -10V, or both, over-riding the function of the appropriate level controls.

2.4 COMPATIBILITY WITH EARLIER MODELS

Any of the listed range of modules can be used in a PG52 B main frame. The PG52 A main frame differs from the PG52B (i) in the details of its mechnical assembly and (ii) in not having a line frequency supply distributed to the plug in modules for the line trigger facility of the PG52 P10 Trigger module.

Any of the listed range of modules can be used in this frame. However the line trigger facility of the PG52 P10 module will be inoperative.

The PG52 main frame differs from the PG52A in not having a +5V power supply circuit for the PG52 P8 Word Generator. This module can however be used in the PG52 main frame if an adaptor is fitted to the module and the additional current loading limitation of section 3.3 is observed.

PG52 main frames and early PG52A main frames fitted with unperforated side covers, should have the right side panel replaced by a perforated version before a PG52 P6 power module is used.

The 'A' versions of the P1, P2, P3 and P4 modules, differ from the original version in having rotary rather than edge operated fine controls. The P1 and P2 also had both coarse and fine controls to cover each decade range while the P1A and P2A have a single control. In specifications and all other details the earlier modules are the same as 'A' version.

Unless specifically stated in this handbook reference to modules P1, P2, P3 or P4 shall apply to that module and its 'A' version.

2.5 PG52 P5 PASSIVE SUMMING UNIT

This module, being a purely passive unit, may either be used mounted in the case, or used externally if more convenient. It consists of two 50Ω resistive networks, enabling either two or three output pulses to be added together for waveform synthesis. The unit is intended for summing the outputs of the P3 module, but other signal sources may be used, for example, sinusoidal voltages or further DC offset.

Specification

Two-Input Network. Delta circuit between two inputs and one output socket. Input and output impedances are 50Ω provided that the output is terminated with 50Ω and each input has a source impedance of 50Ω. Output voltage is half the sum of the input voltages.

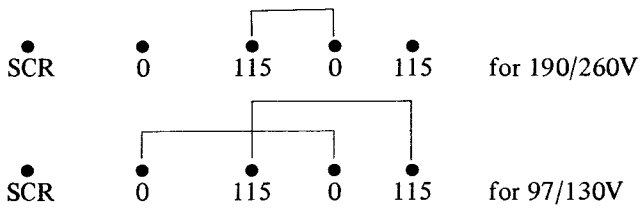
Three Input Network. Similar to two-input circuit, but output voltage is one-third the sum of the input voltages.

Peak Input Voltage. To be no greater than 10V.

3.1 POWER SUPPLIES

The instrument is designed to operate from 45 to 60Hz a.c. supplies in the range 100 to 130 or 200 to 260V. It is normally supplied with the supply transformer taps set for 200 to 260V operation. These taps should be checked before use and changed if necessary. A tap change switch is provided on the PG52B main frame, operated by a recessed knob on the rear panel.

To change the series-parallel primary windings of the PG52 or PG52A versions of the main frame from 200/260V to 100/130V the links on the lower row of solder taps on the supply transofrmer should be changed as follows:–



The cable form connections to the solder tags should not be changed.

Improved access is obtained to these connections if the screws holding the top bar at the rear of the instrument are removed and the rear tray pivoted back about the bottom bar. For this, the side covers must be removed in addition to the top and bottom covers.

If the instrument is operated from a 200/260V supply the correct a.c. supply fuse (FS1) is a 1A, size 0, slow blow type, Part No. 21619 (FS1 and FS7 are 1A, size 00, slow blow, Part No. 21014 in the PG52B). For 100/130V operation, this should be changed to a 2A, size 0, slow blow types, Part No. 20439. (2A, size 00, slow blow, Part No. 21301 in the PG52 B).

If a P6, Power Output module is to be used; a 5A, size 0 fuse, Part No. 21807, should be fitted as the Auxilliary fuse, F4, (FS4 and FS7 to be 4A, size 00, Part No. 5120 in the PG52B).

3.2 VENTILATION

The instrument is ventilated by a fan mounted on the back panel. The inlet and outlet areas at the rear side of the instrument must not be obstructed. The air filter must also be kept clean; it should be removed and washed in water when necessary. To maintain correct air circulation the instrument should not be operated without a full complement of modules or blank panels, PG52 P0.

These precautions are particularly important when a power Output module P6 is in use.

If the current loading (see section 3.3) is exceeded by plugging in an unwanted module to fill a space, the module can be inserted upside down, when the plug on the module will not engage in the socket of the main frame.

3.3 CURRENT LOADING

The internal +20V, -20V and + 5V supplies are each limited to 2A.

Any combination of plug-in modules can be used in one unit which does not exceed this 2A capability.

The maximum load imposed by each type of module is as follows:–

	+20V line	-20V line	+5V line
PG52A P1 or P1A	0.25A	0.15A	NIL
PG52A P2 or P2A	0.1A	0.05A	NIL
P3 or P3A	0.3A	0.3A	NIL
P4 or P4A	0.45A	0.45A	NIL
P5	NIL	NIL	NIL
P6	0.05A	0.05A	NIL
P7	0.35A	0.35A	NIL
P8	0.15A	0.05	0.3 in PG 52A or PG 52B
P8	0.45A	0.05	NIL with adaptor for PG52.
P9	0.15A	0.1A	NIL
P10	0.25A	0.25A	NIL
P12	0.1A	0.05A	NIL
P13	0.3A	0.3A	NIL

The rating of the P3, P4 and P13 modules include the 200mA load from each supply if the full +10V to -10V output capability is being used into a 50Ω load. The 1A output current of the P6 module is derived independantly.

It will be seen that the most likely combinations of 8 modules do not exceed the 2A limitation. However, if a number of P3 or P4 modules are used at one time the sum of the above loads does exceed 2A a closer analysis may show that the supply is not overloaded.

For this purpose assume that each P3 or P13 module takes a quiescent current of 0.1A and each P4 module one of 0.25A from each supply. The total quiescent current loading, plus the instantaneous peak output current, must not exceed 2A. The use of the attenuator of the P3 module does not relieve the load on the supply because the current is being delivered into the attenuator resistors if not into an external 50Ω load. However, if either of the fine level controls on any output unit is not at maximum, the load is reduced accordingly. Also, if the output pulses from a number of units are separated in time, the instantaneous peak output current is not the sum of the peak output currents.

If however, the power supply is overloaded, the supply line voltage may drop and the instrument not perform to specification or the corresponding 2A fuse of the main frame may blow.

For less exacting applications where variable amplitude, specified rise time and overshoot etc., are not required, the 10V outputs from waveform generating or

processing modules can be used directly into high impedance loads. (see section 3.6).

3.4 INTER-CONNECTION

The provision of all modules as separate units, allows them to be interconnected in a large number of configurations each with a different pulse generating function.

Typical inter-connection configurations are shown in section 3.6.

Any module can be mounted in any one of the eight positions of the main frame. The one exception being the Power Output Module P6 which can only be used in the right hand half of the frame. The power supplies are picked up by each module as it is plugged into place.

Signal inter-connection is carried out by 7" long BNC to BNC coaxial leads (PL81). Longer coaxial leads can be used if necessary, but where possible the modules should be so arranged in the main frame to avoid this, particularly if the minimum repetition periods and pulse widths are to be achieved.

The interface output models P1, P2, P8, P9 and P12, are each designed to drive up to 4 inputs. The outputs of the P1, P2 and P12 modules are available on two BNC sockets in parallel. BNC "T" adaptors should be used to provide further fan-out up to the maximum of 4. However the system cannot be used at its maximum frequency or minimum pulse widths with the full loading.

Typically each P1 or P9 Module will drive:–

any 4 modules up to 5MHz
any 3 modules up to 10MHz
any 2 P2, P3, P7, P9 or P12 modules up to 20MHz.
One P3, P7 or P13 modules up to 30MHz.

Typically each P2 or P12 modules will drive:–

any 4 modules to widths greater than 40nS.
any 2 modules to the minimum width of 25nS.

3.5 TERMINATION

The Output modules P3, P4, P6, P7 and P13 are designed to operate into a 50Ω load. Distortion of the output pulse may occur if the units are not correctly terminated. It may also occur if the load is not connected through a 50Ω cable such as the PL43. However, such distortion may be negligible from the Variable Slope Output P4 module if slow rise and fall rates are being used.

3.6 TYPICAL INTER–CONNECTION CONFIGURATIONS

The detailed operating instructions for each module are contained in the relevant handbooks.

The following series of examples show the techniques which can be used in interconnecting modules to obtain different functions. It is obviously possible to extend the different examples or combine them to achieve many complex functions. The details can only be left to the user to obtain the full benefit from the system suiting his particular requirements.

If more than 8 modules are required, two or more main frames can be interconnected via the normal BNC leads. The Passive Summing Unit P5 need not be mounted in the main frame as no power supplies are necessary; but can be free standing in front of the main instrument or remote from it.

In setting up a complex function, it is recommended that each unit is set in turn along the signal path, using the output test points to feed a CRO for examination. The CRO is often best triggered externally from the Clock Generator, P1, or first PWD, P2, signal if available, alternatively the Trigger pulse output of Trigger module, P10, can be used.(See section 3.6.2)

Particular care should be taken to avoid feeding a repetition period into a PWD which is equal to or less than the width set in the PWD. The unit will probably operate in a count-down mode which can be misleading. To avoid this trouble, it is easier to consider the clock rates in terms of period rather than frequency, allowing direct comparison with subsequent delay and width settings. Both period and frequency are coded on the Clock controls. However, in other applications this count-down facility can be used, with advantage (see section 3.6.12).

In most examples, the final output is taken through an output module into a 50Ω load to obtain a specified amplitude and waveshape. However, the normal interface output signal from any other module may be sufficient for many applications. This output is a source of approximately 50Ω impedance with an output e.m.f. of 0 to approximately +10V. The edges of this pulse are substantially square with a rise time less than 20nS.

However no interface output should drive into less than 500Ω (total resultant load on both output sockets on modules P1, P2, P10 or P13). The output wave shape is unspecified and the abberations will increase as the length of the coaxial lead from output to load is increased since this cannot be correctly terminated.

Alternatively an attenuated signal can be derived from an interface output into 50Ω if it is fed through a 470Ω to 50Ω divider network. The pulse can then be transmitted through 50Ω cable without further abberation. Alternatively a long cable may be fed via 470Ω providing it is terminated with 50Ω.

It should be noted that the Passive Summing unit P5, while intended to sum the output pulses from different sources, is a symmetrical delta network which can equally be used as a signal splitter. A pulse from one source can be split into two or three independent 50Ω loads with an attendant loss of amplitude (1/2 or 1/3).

3.6.1 SINGLE PULSE GENERATOR WITH DELAY (Fig. 1)

This straightforward arrangement is the equivalent of the conventional pulse generator.

The Clock Generator, P1, drives through two PWD, P2, modules in cascade into an output unit. These give the frequency, delay, width and amplitude controls respectively of the conventional instruments. The Standard Output, P3, and Variable Slope output, P4, are shown to illustrate the multiple output capability of the system. The Power Output, P6, or Fast Output, P7, modules can equally be used as output units to match any required application.

Waveforms are shown for normal and inverted outputs. From these it can be seen that positive or negative going pulses of any mark/space ratio can be obtained virtually from zero to infinity duty cycle. The 50Ω termination, TP19, is shown on the output to emphasise the need for correct termination of the cable if the output waveforms are not to be distorted.

The unused output socket from the Clock or first PWD module can be used as a prepulse to trigger a CRO. Alternatively the Trigger module, P10, can be interposed between the Clock and first PWD and used to generate an independent conventional prepulse.

3.6.2. SIMPLE DOUBLE PULSE GENERATOR (Fig. 2)

Firstly this example shows the use of the Trigger module, P10, inserted between the clock and first PWD to provide a conventional pre-pulse or Trigger pulse output. This output is shown in waveform E. and can be inserted into any system. Alternatively if a system has to be externally triggered such an external signal can be fed directly into a PWD module, P2, with its variable trigger level facility or via a Trigger module, P10, which has both a more sensitive input than the PWD and an inversion facility for selection of trigger from the positive or negative-going input slope.

Secondly this example shows the use of a summing coupler, PL85, to trigger a PWD module, P2, on the negative going transitions of two independent inputs. As in the double pulse facility of most conventional pulse generators, the second PWD (width) is initiated both at the clock period which initiates the first PWD (delay) and at the end of the delay period. Waveform C shows the generation of periods t3 at both the beginning and the end of period t2.

The spacing between the two periods t3 is limited by the necessary recovery time of the PWD generating t3. The PL85 is not suitable for use in this application with clock rates greater than 1MHz or with pulse separations less than 200nS.

3.6.3 DOUBLE PULSE GENERATOR AND INDEPENDENT WIDTH CONTROL (Fig. 3)

This example shows the addition of two output pulses in one Standard Output, P3, module to form a double pulse generator in which there is no limitation to the period between the two pulses. In fact as t3 is reduced or t2 increased, the pulses can be made to merge.

The SELECT INPUT A and B buttons on the output module can be used to remove each input pulse as required.

If the overlap capability of the pulses is not required, it may be more convenient to drive the input of the second PWD module from the output of the first rather than from the clock Gen. P1. This gives control of the waveform in terms of the first pulse width, the space and the second pulse width without interaction.

3.6.4 DOUBLE PULSE GENERATOR WITH INDEPENDENT WIDTH AND AMPLITUDE CONTROL (Fig. 4.)

This example shows the use of the Passive Summing Module, P5, to make a double pulse generator with independent control of the polarity and amplitude of each pulse. The clock drives two PWD chains as in the previous example but each chain independently drives an output unit. These two outputs are then added in a summing unit.

It should be pointed out that the use of the summing unit limits the maximum output voltage of each pulse into 50Ω, to 2.5V; allowing for the need for 50Ω back termination of the summing unit and its inherent 2.1 attenuation.

The effect of reducing t3 or increasing t2 is to make one pulse 'climb' on top of the other when they overlap.

A variety of waveforms can be produced in this manner, particularly if one or both of the output units are P4 Variable Slope Output Modules. However, in this case the P4 modules should be fed to the P5 module through a 50Ω series resistor to maintain the back termination for the P5.

3.6.5 TRIPLE PULSE GENERATOR (Fig. 5)

This example shows the use of the trigger level controls on the PWD, P2, unit to determine the time at which the pulse is initiated. A Clock drives a Variable Slope Output Module, P4, set to give a negative going ramp from +5V to -5V, which is the trigger level range of the PWD. This ramp signal is fed as the input to 3 PWD units. The trigger level control of each thus determines the point at which the pulse is initiated. Thus three pulses are generated with independent control of their width and relative position on the ramp.
If the ramp slope is altered the relative positions of the three pulses change in proportion. To obtain the three pulses out on one line, one standard ouput module is used to combine two of them (D and E to F). This combined pulse with its amplitude set to 0 to +10V, is combined with the third pulse C in the final output unit to give the required waveform. This form of combination is necessary because each output module is limited to two inputs.

Alternatively, similar triple pulse generation can be obtained using 5 or 6 PWD in the conventional way, extending the techniques given in examples 2,3 and 4 above.

The variable trigger level facility can also be used either to control the trigger point on any slowly varying waveform such as a sine wave, or to avoid spurious multiple pulsing where there is more than one transition through the normal trigger level, due to a ring or other unwanted distortion on a waveform.

3.6.6 SWEEP FREQUENCY GENERATOR (Fig. 6)

This example shows the sweep facility of a Clock Generator, P1, Module.

A clock drives through a PWD, P2, into a Variable Slope Output, P4, Module.

The output of this unit is set to be a slowly rising ramp voltage which feeds the sweep input of a second clock. Thus the output signal taken through a second PWD and a Standard Output, P3, module is of pulses of fixed width whose frequency increases and decreases with the slow ramp voltage. The range of frequency modulation is determined by the amplitude of the sweep voltage.

Any alternative signal can be used as the sweep input voltage (e.g. a dc line can be used for remote frequency control).

This technique of frequency modulation can of course be extended to modulation of width or delay or of amplitude, using the P12 and P13 modules.

3.6.7 PULSE BURST GENERATOR (Fig.7)

This example uses two Clock Generators, P1, modules. The first determines the frequency at which burst occur. This drives a PWD, P2 which determines the duration of the burst by driving the gate input of the second Clock. This second clock determines the frequency of pulses within the burst and in turn drives a second PWD which determines the width of the pulses. The final output is taken from a Standard Output Module.

The clock (and hence the first output pulse in a burst) always starts in synchronism with the application of a gate pulse. At the end of a gate pulse the clock output is clamped positive and cannot generate a spurious output pulse. The Clock (not the PWD) is gated and any output pulse initiated in the PWD is not foreshortened by the closing of the gate pulse. Thus as the burst period t2 or the repetition period within the burst t3 is varied, an integral number of complete pulses will be generated, corresponding to the relationship between the two periods.

Section 3.6.9 shows an alternative method of deriving the burst period using two PWD modules in place of a clock.

3.6.8 SERIAL WORD GENERATOR (Fig. 8)

The Word Generator P8, can be used driven directly from a clock and into an output module to provide a non-return-to-zero waveform cycling through any required pulse pattern up to 16 bits in length. Alternatively a return-to-zero waveform can be obtained by inserting a PWD module between the Word Generator and Output module.

The example in fig. 8 shows the extension of a non-return-to-zero waveform beyond 16 bits by cascading two word generators. The last bit output of each generator is used to start the other. It may be necessary to switch one generator momentarily from external start to repeat to initiate the cycle.

A 24 bit word is shown as the sum of 16 bits on one generator with 8 bits on the other but the total could be split in any convenient form (e.g. 12 + 12 bits).

The total word length could be extended beyond 32 bits, almost indefinately by adding more word generators in the chain. Their outputs would then best be summed in a Gate Module, P9, before feeding an output module. A Gate module should also be used (with all used inputs and the output set to invert) to sum R.Z. outputs from two or more word generators and then the Gate module used to drive a PWD for the generation of return-to-zero waveforms beyond 16 bits in length.

3.6.9 WORD BURST GENERATOR (Fig.9)

This example shows the use of a dc coupled external start for a word generator module.

The clock generator provides a clock signal for the word generator and determines the bit rate.

Two PWD's are cross-coupled to form a lower frequency multivibrator which determines the burst rate, the period between bursts being the sum of the two periods, t1 and t2. The two phases of this multivibrator output, A and B, are used to gate the clock (synchronising the clock pulses to the burst rate) and initiate a further PWD which in turn determines the period of the word burst (the number of complete words in the burst). It will be seen that the work generator will complete any words initiated during the period t3.

If a single word only is required at the slower rate, the period t3 can be reduced to less than 1 clock period or the external start input to the word generator be ac coupled internally. In the latter case the third PWD need not be used and the external start taken from A.

It should be noted that many other applications can use the technique of cross-coupling two PWD modules to form a multivibrator if a clock is not available.

3.6.10 4 BIT PARALLEL WORD GENERATOR (fig.10)

This example shows the operation of a number of Word Generators, P8, in parallel to produce a serial sequence fo 4 bit parallel words. A common clock signal is fed to all Word Generators, P8, in parallel. The system

shown produces a continuous pattern with one of the Word Generators, P8, set to 'Repeat' and its Last Bit output used as 'Start' for the other three. All four generators should then be set to the same word length.

Each of the four outputs is shown fed through an output module and it is appreciated that this involves the use of more modules than can be accommodated in one main frame. Two frames can be used, with normal front panel interconnection, or another external clock source used. Alternatively the Word Generator interface signals can be used directly if they are suitable.

The example shows a system on 'Repeat' but it is equally possible to operate all four Word Generators, P8, from a common external start signal. Similarly, the RZ output can be used if each word output is fed via a PWD module P2 to the output module.

The width of each PWD should be set to the same value.

3.6.11 TRINARY STATE WORD GENERATOR (Fig.11)

This shows a special application of the operation of two Word Generators, P8, in parallel to produce a 3-state output word (i.e. the level of each bit can be set as +, 0 or -). The two Word Generators P8, are set to the same word length and the last bit output of one, operating in its repeat mode, is used as the 'start' of the other so that the two operate in synchronism. The word output of one is taken directly through an output module with its output levels set to give a +ve pulse. the word output of the other is taken via another output module set to invert, and its output levels set for a negative pulse. The two resultant output signals are added in a Passive Summing Unit, P5. Thus the state of each pulse position in the word can be set:—

(i) to +, by setting the appropriate toggle switch on the first P8 module for a 'mark' (bits 2 and 4).

(ii)to OV, by setting neither toggle switch to 'mark' (or by setting both to mark).

(iii) to -, by setting the appropriate toggle switch on the second P8 module to 'mark' (bits 6 and 8).

3.6.12 COUNT DOWN FACILITIES

a) If very slow clock rates are required, it is possible to feed one clock into a second which is on its 'trigger divide' mode. This allows the 10 sec. repetition period of the first clock module, to be extended to 100 or 1000 sec. Obviously further Clock modules can be cascaded to extend the period further.

b) If it is required to synchronise a system to an external signal, it is often better to feed the signal directly into a PWD, P2, module rather than as 'trigger' into a Clock Generator, P1, module. The PWD has the variable trigger level facility and can also be set to a periodic count-down of any number up to 10. For further division (10 or 100) the output of the PWD can be fed to a Clock module on its 'trigger divide' function. Overall periodic division ratios of 20, 30, 40-90, 100, 200, 300-900, 1000 can be obtained.

c) If the 50Hz supply, isolated and stepped down to a suitable voltage, is used as the trigger input, count down facilities can be used to derive slow clock rates with the accuracy of the supply frequency (e.g. A PWD set to approx. 90mS, will count-down by 5 and, followed by a clock on ÷ 10, will give a reasonable accurate 1 second clock. Alternatively a second PWD, following the first but set to approx. 550mS, will divide by a further 6 and then followed by a clock on ÷ 100, an overall ratio of 3,000 is obtained. (i.e. one pulse per minute).

Similar techniques can be used at higher frequencies to derive periods based on an external crystal standard frequency.

3.6.13 LONG DELAY PERIODS (Fig. 12)

The maximum width or delay period which can be generated from a P2 module is 1 sec. This limit can be extended almost indefinitely with the arrangement shown in fig. 12.

The basic system which allows generated periods up to 8 seconds, requires a PL85 Summing Coupler, a P9 Gate Module and a P1 Clock Module. The gate module is cross-connected and switched as shown to form a set/reset bistable. A positive start signal is applied directly at B or, if necessary, generated from a negative going transition into a P2 PWD module as shown. This reverses the bistable, sending C high and gating the clock on. The output D of the clock, originally positive, goes low for a period which can be set up to 8 seconds by the clock rate (i.e. the first part of its normal 4:1 mark space output cycle on its low frequency ranges).

The positive transition at the end of the 8 second period is differentiated by the PL85 coupler to reset the bistable and hold the system locked off, until the next start signal is applied. The PL85 is not used in its conventional mode but the signal from the clock is applied to the output lead while the gate is driven from the input lead. This allows a positive transition to be passed by the internal diode and capacitor coupling rather than the normal negative going transition which is used to trigger a PWD. The 8 second output can either be taken from the clock or from either side of the bistable as required.

For periods longer than 8 seconds, the output of the first clock is used to drive a second clock which is set to External trigger and divide by 10 or 100. This is also gated by the bistable and the PL85 is driven from this second clock instead of the first. Thus the first clock is allowed to run for 8 or 80 cycles, each of which can be of 10 seconds duration, generating periods of 80 or 800 seconds.

3.7 USE OF THE PASSIVE SUMMING UNIT

This module contains two independent resistive networks.

3.7.1 THE TWO INPUT NETWORK

This is a symmetrical delta circuit between the two input sockets and the output socket.

To maintain a 50Ω system, to eliminate distortion and preserve the correct voltage ratios, both inputs must be fed from sources of 50Ω output impedance. Thus the Standard or Modulated Output Modules, P3 or P13, should be used on the 5V or lower ranges, not on the 10V direct range which has a low output impedance. If the Variable Slope Output, P4, module or any other low impedance source is used, a 50Ω series resistor should be inserted in the line at the source. If at any time, one input is disconnected and the other input require at the output undistorted, a 50Ω termination such as TP19 should be connected on the unused input. When the output is terminated in 50Ω the input and output impedances of the network are also 50Ω. The output voltage of the network at any instant is half the sum of the two input voltages.

The peak input voltage at either input socket should not exceed 10V.

3.7.2 THE 3 INPUT NEWTORK

This is a symmetrical 4 port network, allowing the summation of three input signals on one output.

It is similar to the two input network. Each input should be fed from a 50Ω source impedance and the input and output impedances are 50Ω as in 6.1 above.

The output voltage at any instant is one third of the sum of the input voltages.

The peak input voltage on any input should not exceed ±10V.

3.7.3 DISTORTION

This module is compatible with the output modules P3, P4 and P13. No extra overshoot is introduced and the rise time is degraded by less than 1nS.

3.7.4 GENERAL USE

This network can be fed from any signal source not exceeding ±10V peak. It can be used to build up complex waveforms from separate pulse, sine and other waveforms. If more than three inputs are required and the subsequent attenuation can be accepted, one network can be fed into another.

Alternatively it can be used as a power divider, to split a signal from one 50Ω source into two or three 50Ω loads without distortion but with attenuation. The input should be applied to one input socket and the outputs taken from the output socket and the other input socket or sockets.

4.1 MAIN FRAME PG52

The main frame contains the power supply circuits and the sockets which distribute the supplies to the 8 module positions, and the circuit is shown in fig. 16.

This series/parallel primary windings of the supply transformer, T1, are driven from the incoming supply through the on/off switch, S1, fuses, FS1 and FS7, and the supply range switch, S2. The latter automatically connects the two windings in series for use on 200/260V supplies or in parallel for 100/130V supplies. The two 26V secondary windings drive identical 20V rectifier and stabiliser circuits which are linked at their outputs to give the 20V and -20V lines. A 12V secondary winding drives a similar circuit to derive the +5V line. A further 50V winding provides an ac supply to all 8 module positions.

The +20V circuit is described in detail. The bridge rectifier, MR7, is followed by the reservoir capacitor, C1, with its discharge resistor, R21. The unstabilised dc supply is fed through the fuse, FS2, to the stabiliser circuit which is mounted on the printed circuit board. A zener diode, MR5, is the reference diode. The voltage across MR5 is compared with a proportion of the output voltage determined by R5, R28 and R19, at the base-emitter junction of VT5. Any inequality is amplified by VT5 and transferred through emitter follower, VT3, to the final series stabiliser element: the emitter follower, VT7, correcting the output voltage. VT1, with MR1 and R3, provides a high impedance current source to feed VT5 and MR5, giving VT5 a high voltage gain. MR3 detects the voltage across R9 which carries the output current. If this current exceeds 2A, MR3 conducts to cut off VT1 and reduce the output voltage This overload circuit protects VT7 against heavy peak overload currents of short duration which would not blow fuse, F2. R28 is used to set the output voltage to +20V and C3 provide a low output impedance to the rapid changes of load current imposed by the modules. VT7 is mounted on the rear panel as a heat sink.

The -20V and +5V stabiliser circuits are similar to that described for the +20V supply. The positive side of the -20V supply is linked to the negative side of the +20V supply as the common OV point. The negative side of the +5V supply (OV, 5) is linked to this OV point via R58. The two OV lines are only joined directly within a module, reducing common earth return paths.

The terminal board, TB1, is mounted behind the 8 sockets, SKA to SKH, for the modules and acts as a star point from which the sockets are fed. C5, C6, C11 and C12, decouple the supplies at this point and prevent interaction between the individual modules.

The incoming ac supply is also distributed through separate fuses, FS4 and FS6, and the terminal block, TB2 to SKE, SKF, SKG and SKH. This is for use in the Power Module, P6, which has its own power supplies. It is linked from TB2 to SK8 and a fuse link fitted in FS4 and FS7 only when required.

A fan with its dual windings connected across the primary windings of T1, is used to increase ventilation and prevent the instrument from overheating on full load.

The circuit of the PG52A main frame is identical to that of the PG52B with the following exceptions.

(i) The fuses, FS6 and FS7, in the neutral of the supply are not fitted.
(ii) The supply range switch, S2, is not fitted; the windings of the transformer being linked directly for the range required.
(iii) The 50V secondary winding is not included.

The circuit of the PG52 main frame has the above differences from the PG52B and the +5V circuitry is also omitted.

5.1 ROUTINE MAINTENANCE

The only regular maintenance necessary is the cleaning of the air filter on the back tray of the instrument. This should be removed and cleaned in water when necessary.

The fan motor bearings need no regular maintenance.

5.2 FAULT LOCATION

The modular construction of the instrument allows fault location by substitution. Any module suspected of being at fault can be replaced by another module to confirm the suspected fault to be within one module. Full or partial failure of all modules is probably due to a fault in the common power supply or its distribution in the main frame. The fuses should be checked and also the potentials on the +20V and -20V lines. A fault within one module, taking excessive current from one of the lines, can overlead the line and reflect on the performance of the other modules.

When a fault is localised within the power supply or any one module, the faulty part can be returned to the factory for repair or further investigation can be carried out in with the help of the relevant circuit diagram and circuit description. Component replacement in any module may require it to be recalibrated.

5.3 FUSE REPLACEMENT

There is direct access to the fuse holders on the main frame (rear panel of PG52 and PG52A and front panel of PG52B). The correct replacement fuse links are as follows:—

PG52 and PG52A			Rating	Advance Pt. No.	Note
FS1	(Supply)	200/260V	1A Size 0	21619	Slow blow
		100/130V	2A "	20431	type
FS2	(+ 20V)		2A "	21180	
FS3	(-20V)		2A "	21180	
FS4	(Aux. supply)		5A "	12807	Only fitted for PG52 P6.
FS5	(+ 5V)		2A "	21180	PG52A only

PG	52B		Rating	Advance PT. No.	Note
FS1	(Supply L)	200/260V	1A Size 00	21041	Slow blow
FS7	(Supply N)	100/110V	2A "	21301	type.
FS4	(Aux supply L)		4A "	5120	Only fitted
FS6	(" " N)		4A "	5120	for PG52P6
FS2	+ 20V		2A "	25088	
FS3	- 20V		2A "	25088	
FS5	+ 5V		2A "	25088	

5.4 ACCESS

Access to the main frame components is obtained by removing the top and bottom covers. These slide back when the fixing covers have been removed from the front and back edges.

Improve access to the power supply components is obtained by hinging down the back panel after removing the two screws which hold the top bar to the side panels and slacking off those on the bottom bar. It is first necessary to remove the rear trim bars and slide out the side panels to gain access to these four screws. On the PG52B it is also necessary to remove the two screws fixing the transformer to the side member and the struts between the back panel and rear support bars.

5.5 POWER SUPPLIES

R28 adjusts the +20V line potential, R24 the -20V line potential, and R56 the +5 line potential. These can be adjusted from the front of the instrument if some of the modules are removed from the right hand side of the instrument, the +20V and -20V presets being accessible through holes in the +5V stabiliser board.

Each line should be set to within 200mV of nominal. The 100Hz ripple should be less than 10mV pk/pk at full load of 2A. Each line should not change more than 250mV as the load current is changed from 0.1 to 2A.

Any fault should be cleared from the +20V line before the +5V line because a current is taken from +20V to supply the reference zener of the +5V stabiliser. The +5V line should be measured with respect to its own ground, OV(5) as a small voltage drop appears across R58 until OV(5) is linked directly to OV within a P8 module.

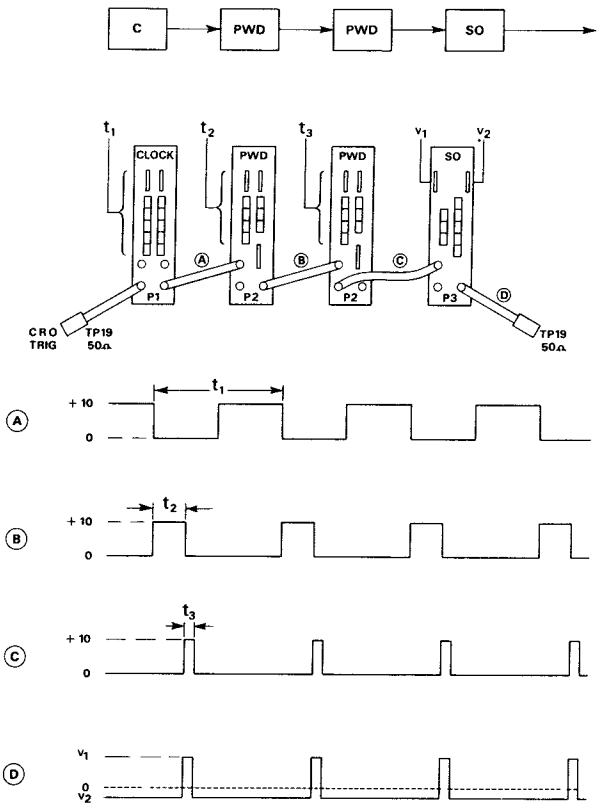


Fig. 1 SINGLE PULSE GENERATOR WITH DELAY

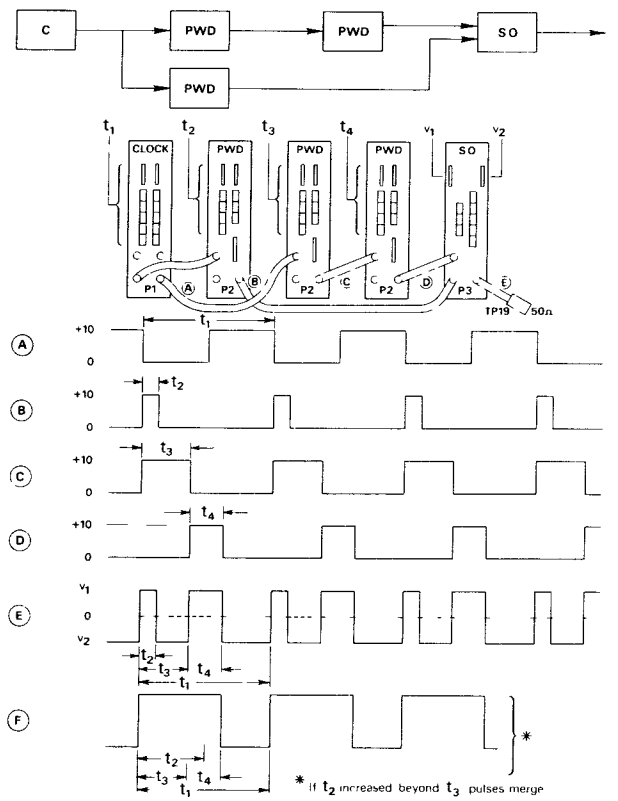


Fig. 3 DOUBLE PULSE GENERATOR WITH INDEPENDENT WIDTH CONTROL

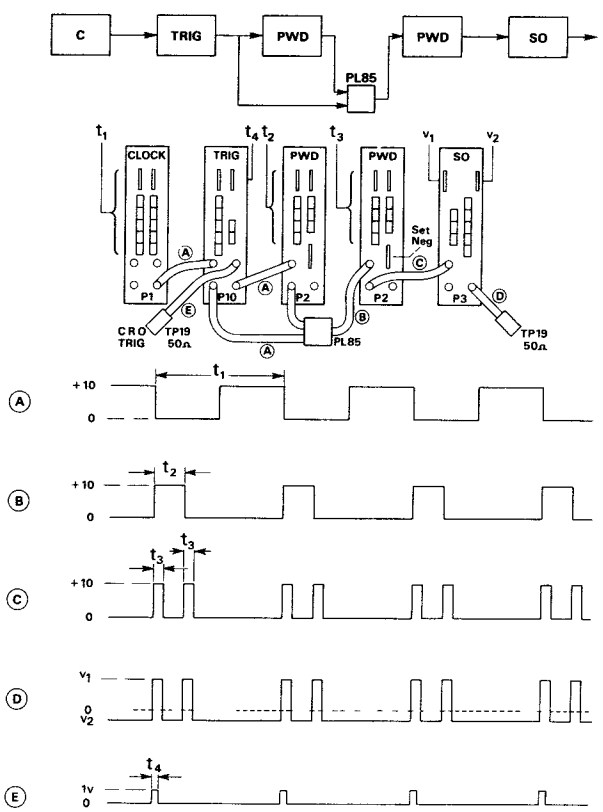


Fig. 2 SIMPLE DOUBLE PULSE GENERATOR

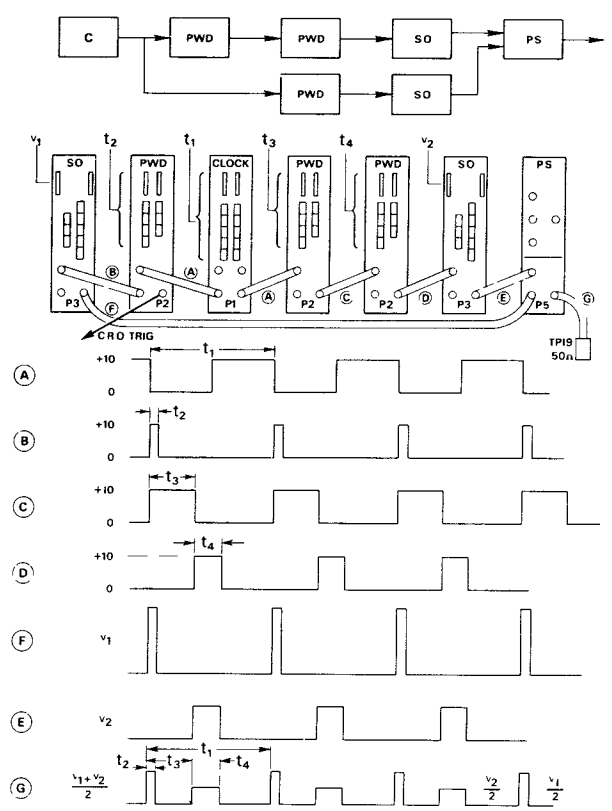


Fig. 4 DOUBLE PLUSE GENERATOR WITH INDEPENDENT WIDTH AND AMPLITUDE CONTROL.

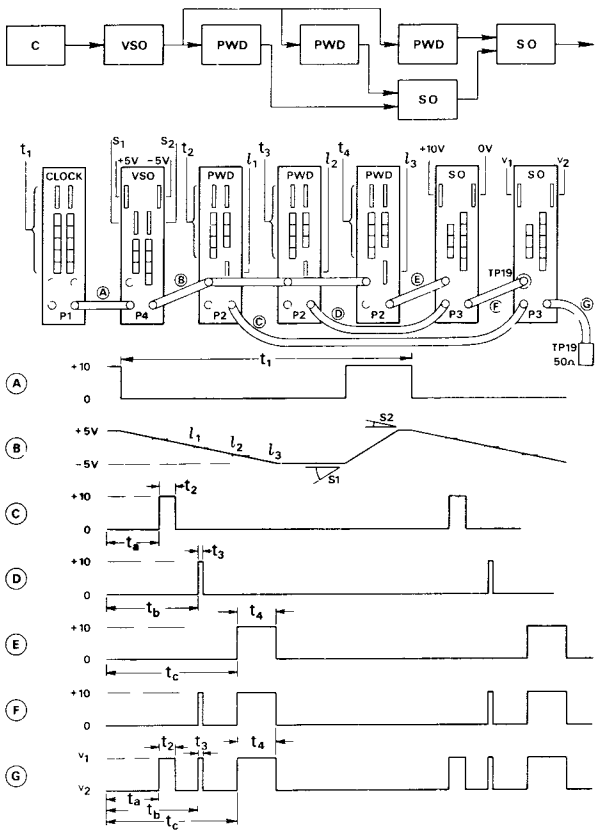


Fig. 5 TRIPLE PULSE GENERATOR

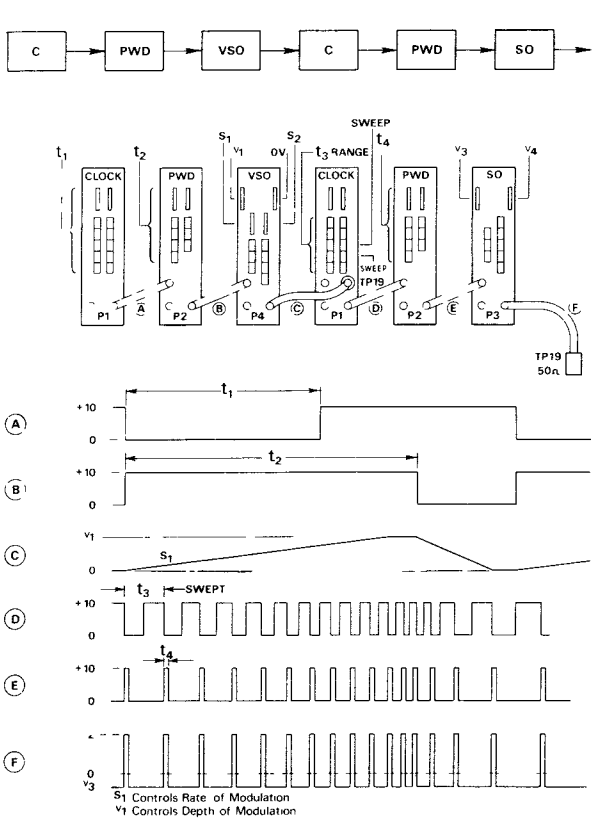


Fig. 6 SWEEP FREQUENCY GENERATOR

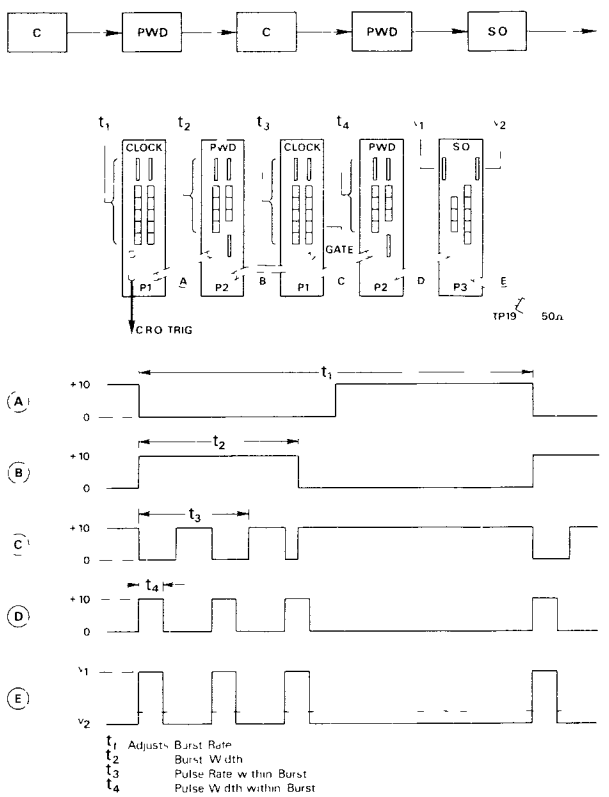


Fig. 7 PULSE BURST GENERATOR

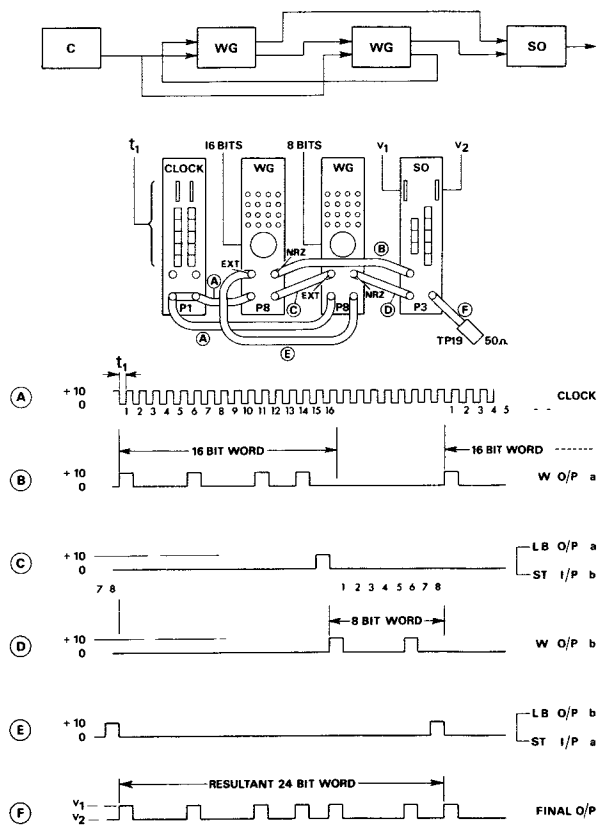


Fig. 8 SERIAL WORD GENERATOR

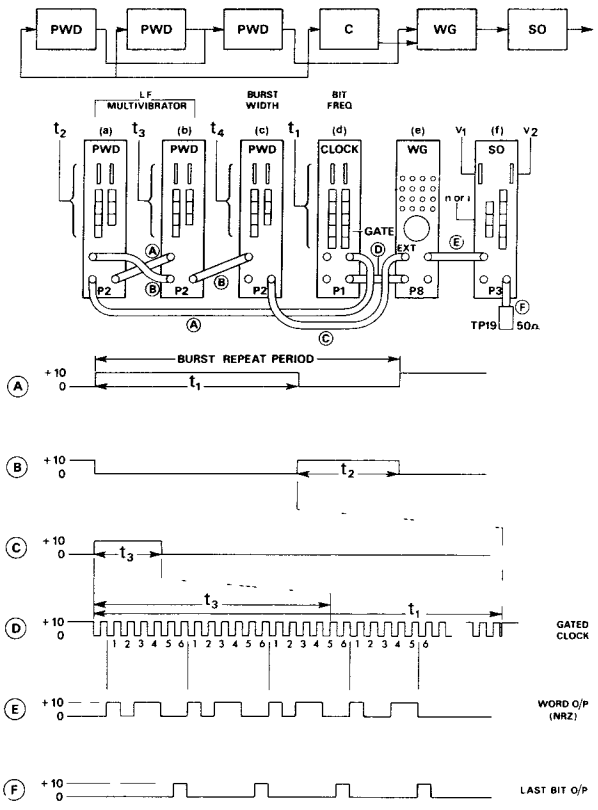


Fig. 9 WORD BURST GENERATOR

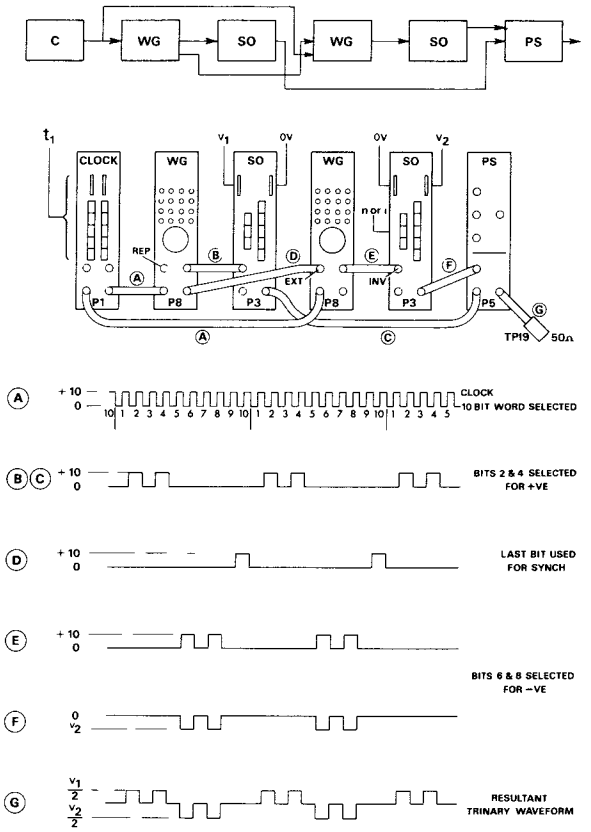


Fig. 11 TRINARY STATE WORD GENERATOR

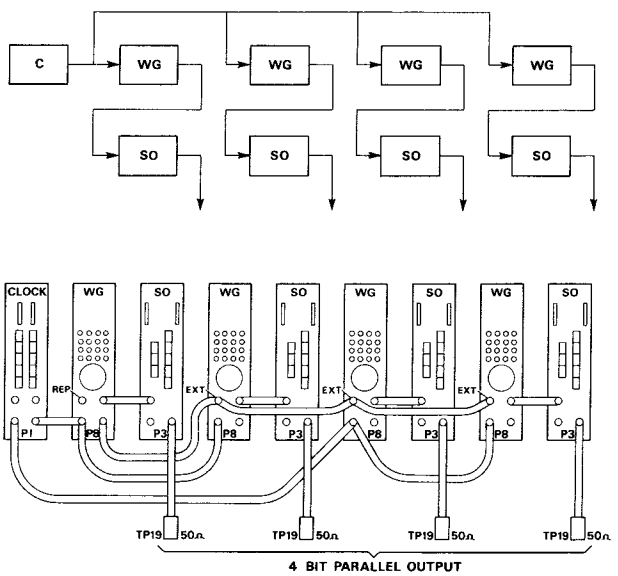


Fig. 10 4 BIT PARALLEL WORD GENERATOR

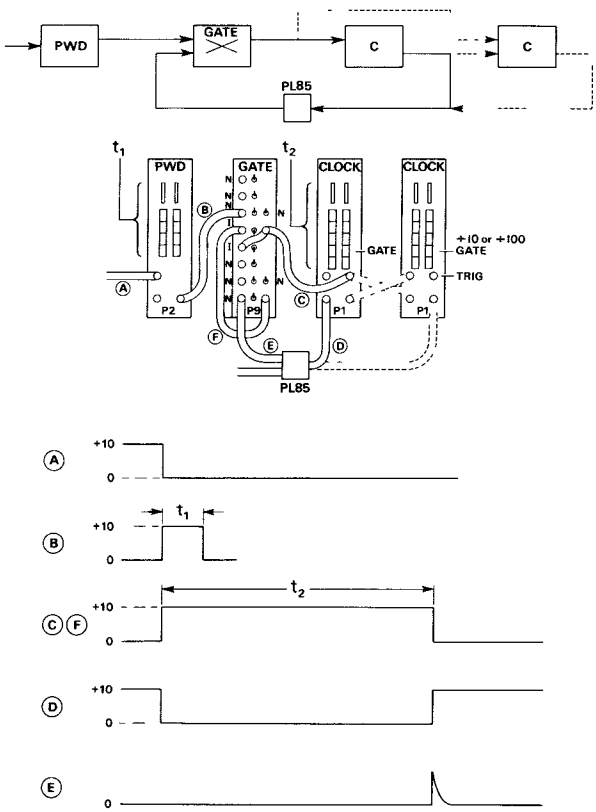
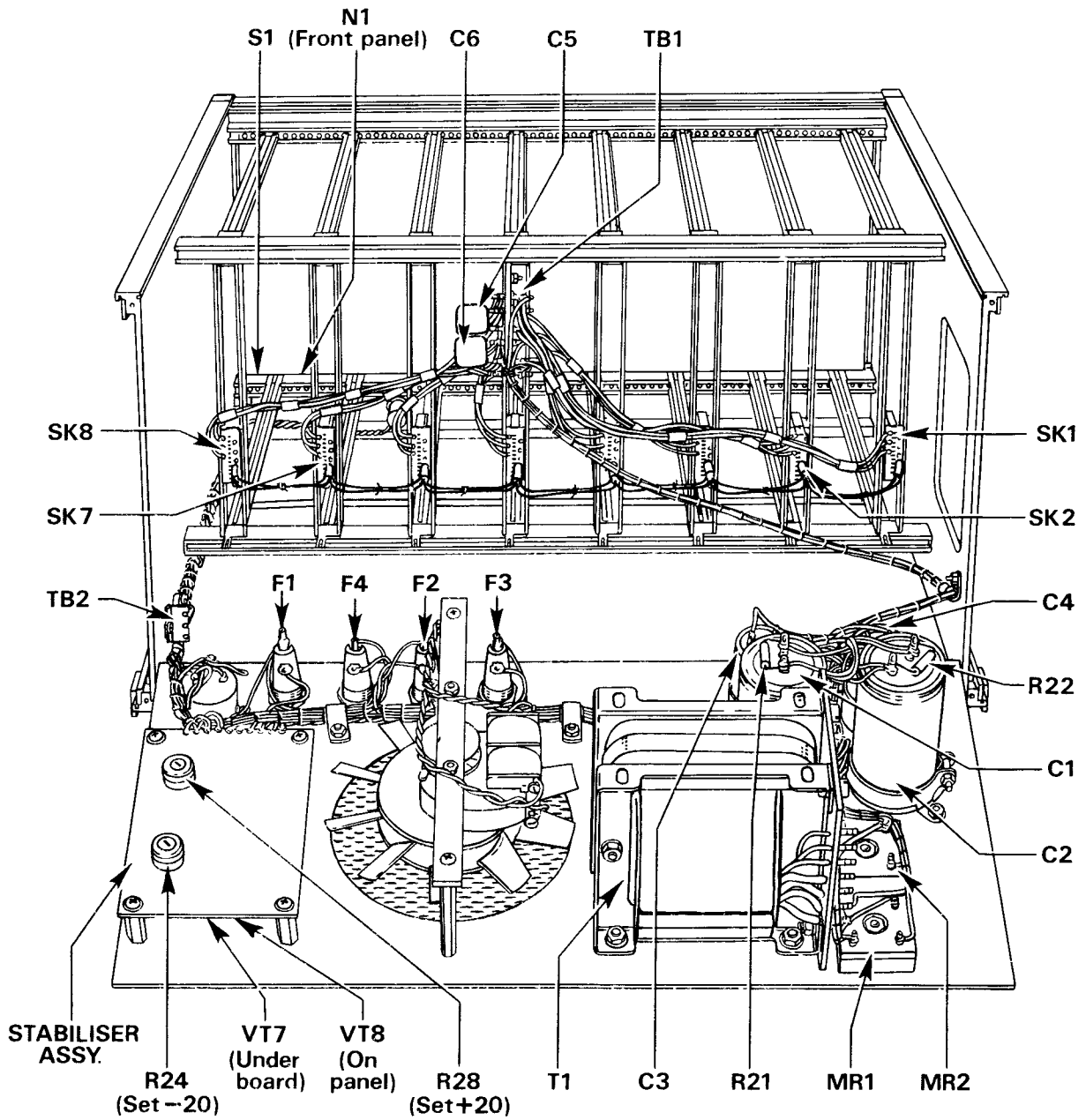


Fig. 12 LONG DELAY PERIODS



Note PG52A includes:

i. 5V Stabilizer Assembly fitted above assembly shown.
ii. C51 alongside C1.
iii. C54 alongside C3.
iv. MR51 alongside MR1.
v. F5 alongside F3.

Fig. 13 COMPONENT LAYOUT (REAR VIEW) PG52 AND PG52A.

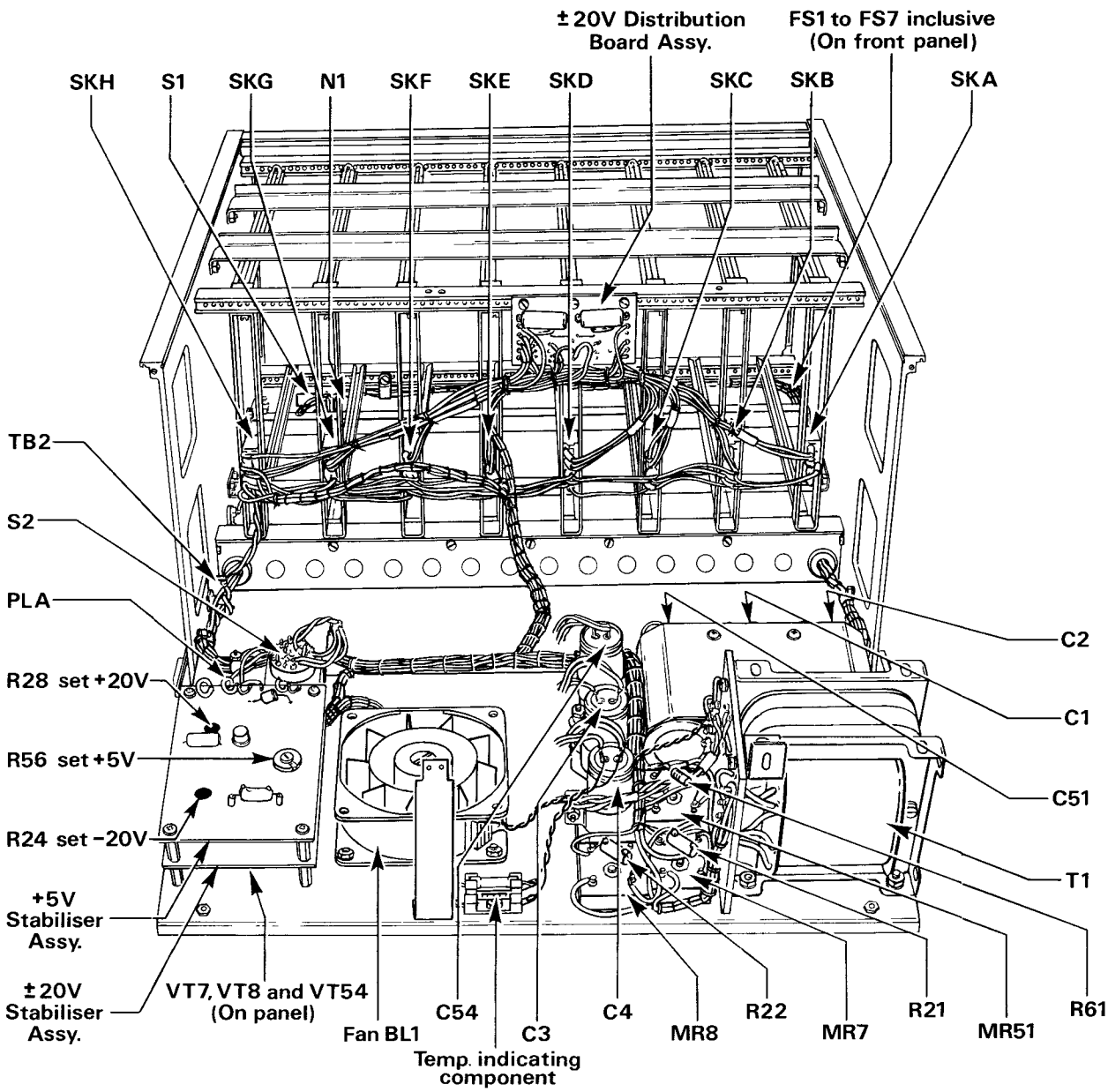


Fig. 14 COMPONENT LAYOUT PG52B

PULSE GENERATOR PG52/A

Ref	Value	Description	Tol%±		Part No.
RESISTORS					
R51	1.2KΩ	Cr. Carbon	5	1/8W	2087
R52	10Ω	Cr. Carbon	5	1/8W	2259
R53	10Ω	Cr. Carbon	5	1/8W	2259
R54	3.9K	Cr. Carbon	5	1/8W	312
R55	120Ω	Cr. Carbon	5	1/8W	735
R56	470Ω	Cont.Pot.Plessey MPD.PC.			28524
R57	680Ω	Cr. Carbon	5	1/8W	309
R58	10Ω	Cr. Carbon	5	1/8W	2259
R59	0.56Ω	RWV4-J	5		18005
R60	180Ω	Cr. Carbon	5	1/8W	1517
R61	1KΩ	Cr. Carbon	5	½W	18550
R62	120Ω	Cr. Carbon (A.O.T.)	5	1/8W	735
CAPACITORS					
C51	4000μF	Elect.		40V	4851
C52	100μF	Elect.		10V	21620
C53	.01μF	G.P. Ceramic			22395
C54	1250μF	Elect.		25V	19215

Ref	Value	Description	Tol %	Part No.
TRANSISTORS				
VT51		2N 3906		21533
VT52		2N 3904		24146
VT53		2N 3053		4039
VT54		2N 3055		3813
DIODES				
MR51		1 B 20 K 20 Texas		2829
MR52		MS 4 H AEI		20422
MR53		1N 914		23802
MR54		ZF 3.3 Zener		4034
MR55		Z 3 B 62 CF Zener		28764
MR56		MS 4 H AEI		20422
FUSES				
F1				
F2				
F3				
F4				
F5		2A B/L. L.1055		21180

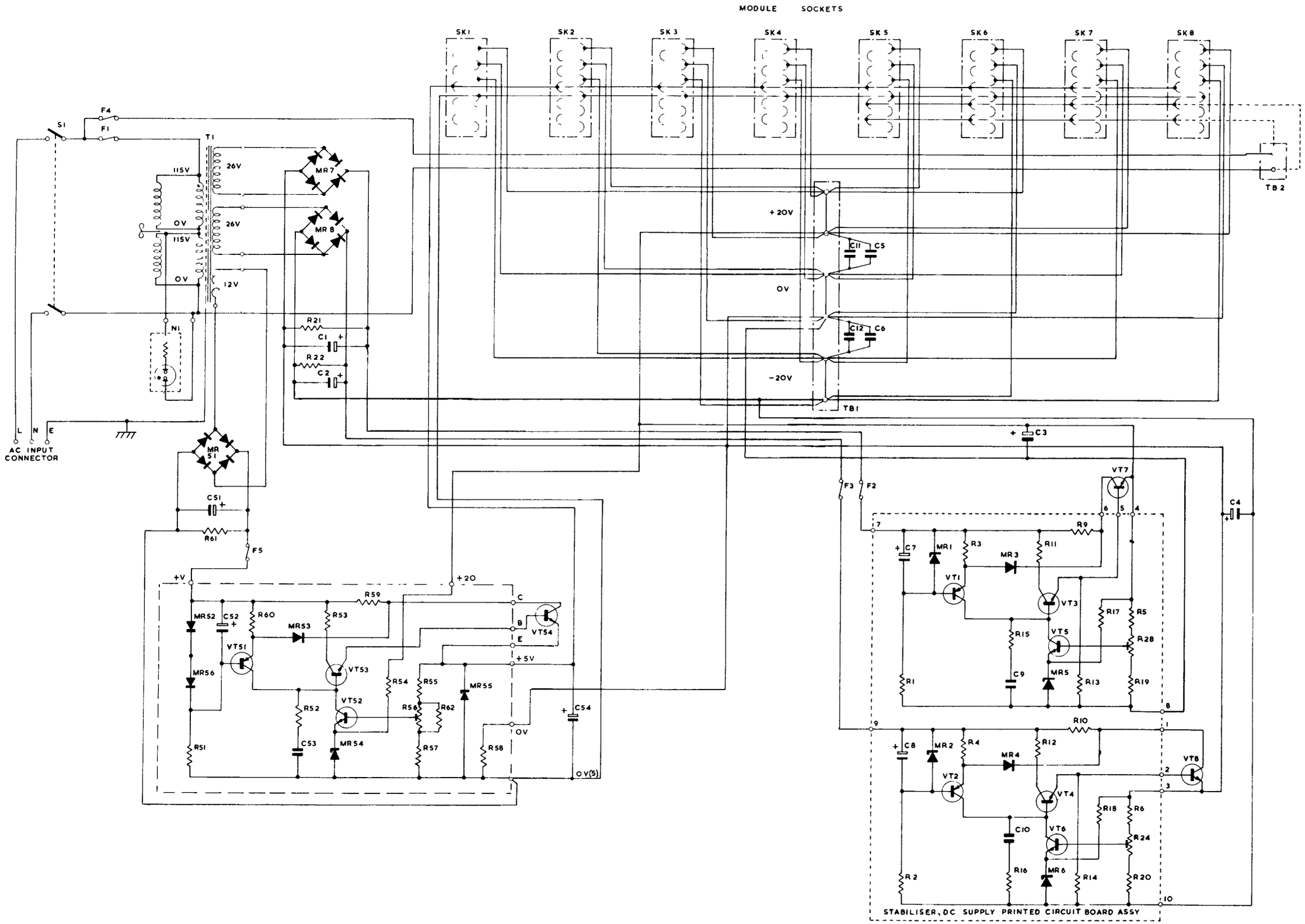


Fig. 15 CIRCUIT DIAGRAM PG52A

PG52B MAIN FRAME

Ref	Value	Description	Tol%±		Part No.
RESISTORS					
R1	4k7		5	1/8W	386
R2	4k7		5	1/8W	386
R3	1k		5	1/8W	384
R4	1k		5	1/8W	384
R5	3k3		5	1/8W	1638
R6	3k3		5	1/8W	1638
R7		Not fitted			
R8		Not fitted			
R9	1Ω		5	6W	239
R10	1Ω		5	6W	239
R11	33Ω		5	1/8W	2931
R12	33Ω		5	1/8W	2931
R13	15k		5	1/8W	315
R14	15k		5	1/8W	315
R15	10Ω		5	1/8W	2259
R16	10Ω		5	1/8W	2259
R17	3k3		5	1/8W	1638
R18	3k3		5	1/8W	1638
R19	1k8		5	1/8W	310
R20	1k8		5	1/8W	310
R21	2k2		5	6W	599
R22	2k2		5	6W	599
R23	1k	Plessey MPD/PC			26870
R24	1k	Plessey MPD/PC			26870
R51	1k2		5	1/8W	2087
R52	10Ω		5	1/8W	2259
R53	10Ω		5	1/8W	2259
R54	3k9		5	1/8W	312
R55	120Ω		5	1/8W	735
R56	470Ω	Plessey MPD/PC			28524
R57	680Ω		5	1/8W	309
R58	10Ω		5	1/8W	2259
R59	.56Ω		5	6W	18005
R60	180Ω		5	1/8W	1517
R61	1k		5	1/8W	18550
R62	120Ω	A.O.T.	5	1/8W	735
CAPACITORS					
C1	4000μF			40V	4851
C2	4000μF			40V	4851
C3	1250μF			25V	19215
C4	1250μF			25V	19215
C5	.1μF		+80 -20	30V	19647
C6	.1μF		+80 -20	30V	19647
C7	200μF			10V	20782
C8	200μF			10V	20782
C9	.01μF		25	250V	22395
C10	.01μF		25	250V	22395
C11	1μF		10	160V	2364
C12	1μF		10	160V	2364
C51	4000μF			40V	4851
C52	100μF			10V	21620
C53	.01μF		25	250V	22395
C54	1250μF			25V	19215

Ref	Value	Description	Part No.
TRANSISTORS			
VT1		2N 3702	19840
VT2		2N 3702	19840
VT3		2N 3053	4039
VT4		2N 3053	4039
VT5		2N 3706	18252
VT6		2N 3706	18252
VT7		2N 3055	3813
VT8		2N 3055	3813
VT51		2N 3906	21533
VT52		2N 3904	24146
VT53		2N 3053	4039
VT54		2N 3055	3813
DIODES			
MR1	3V3	Zener	4034
MR2	3V3	Zener	4034
MR3		1N 914	23802
MR4		1N 914	23802
MR5	6V2	Zener	4032
MR6	6V2	Zener	4032
MR7		Texas 1B40K20	17763
MR8		Texas 1B40K20	17763
MR51		Texas 1B40K20	17763
MR52		0A202	2917
MR53		1N 914	23802
MR54	3V3	Zener	4034
MR55		Zener Z3B62CF	28764
MR56		0A202	2917
MISCELLANEOUS			
T1			A1/35161
BL1		Crouxet Type 340/S	4899
S1			25352
S2			30329
N1			1165
SKA			25301
SKB			25301
SKC			25301
SKD			25301
SKE			25301
SKF			25301
SKG			25301
SKH			25301
PLA			30180
FUSES			
FS1		SLO-BLO (240V supply) 1A	21014
FS2		2A	25088
FS3		2A	25088
FS4		SLO-BLO (240V supply) 1A	21014
FS5		2A	25088
FS6		4A	5120
FS7		4A	5120

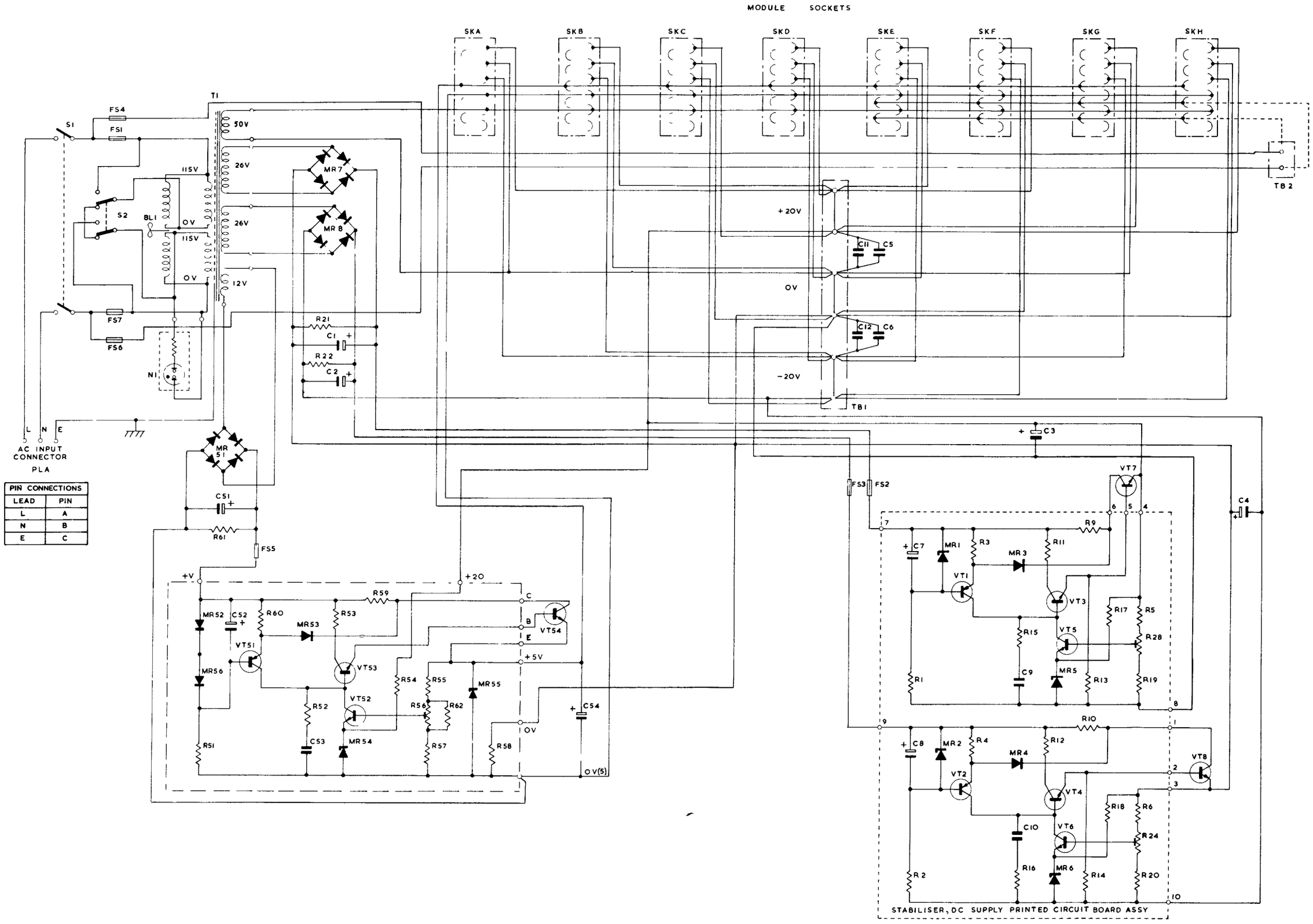


Fig. 16 CIRCUIT DIAGRAM PG52B

PG52 P5 PASSIVE SUMMING

Ref	Value	Description	Tol%±	Part No.
RESISTORS				
R501	100	Electrosil TR6	1	23507
R502	100	Electrosil TR6	1	23507
R503	100	Electrosil TR6	1	23507
R504	100	Electrosil TR6	1	23507
R505	100	Electrosil TR6	1	23507
R506	100	Electrosil TR6	1	23507
R507	100	Electrosil TR6	1	23507
R508	100	Electrosil TR6	1	23507
R509	100	Electrosil TR6	1	23507
R510	100	Electrosil TR6	1	23507
R511	100	Electrosil TR6	1	23507
R512	100	Electrosil TR6	1	23507

Ref	Value	Description	Part No.
SOCKETS			
SK501	50	Greenpar GE35027 BNC	1222
SK502	50	Greenpar GE35027 BNC	1222
SK503	50	Greenpar GE35027 BNC	1222
SK504	50	Greenpar GE35027 BNC	1222
SK505	50	Greenpar GE35027 BNC	1222
SK506	50	Greenpar GE35027 BNC	1222
SK507	50	Greenpar GE35027 BNC	1222

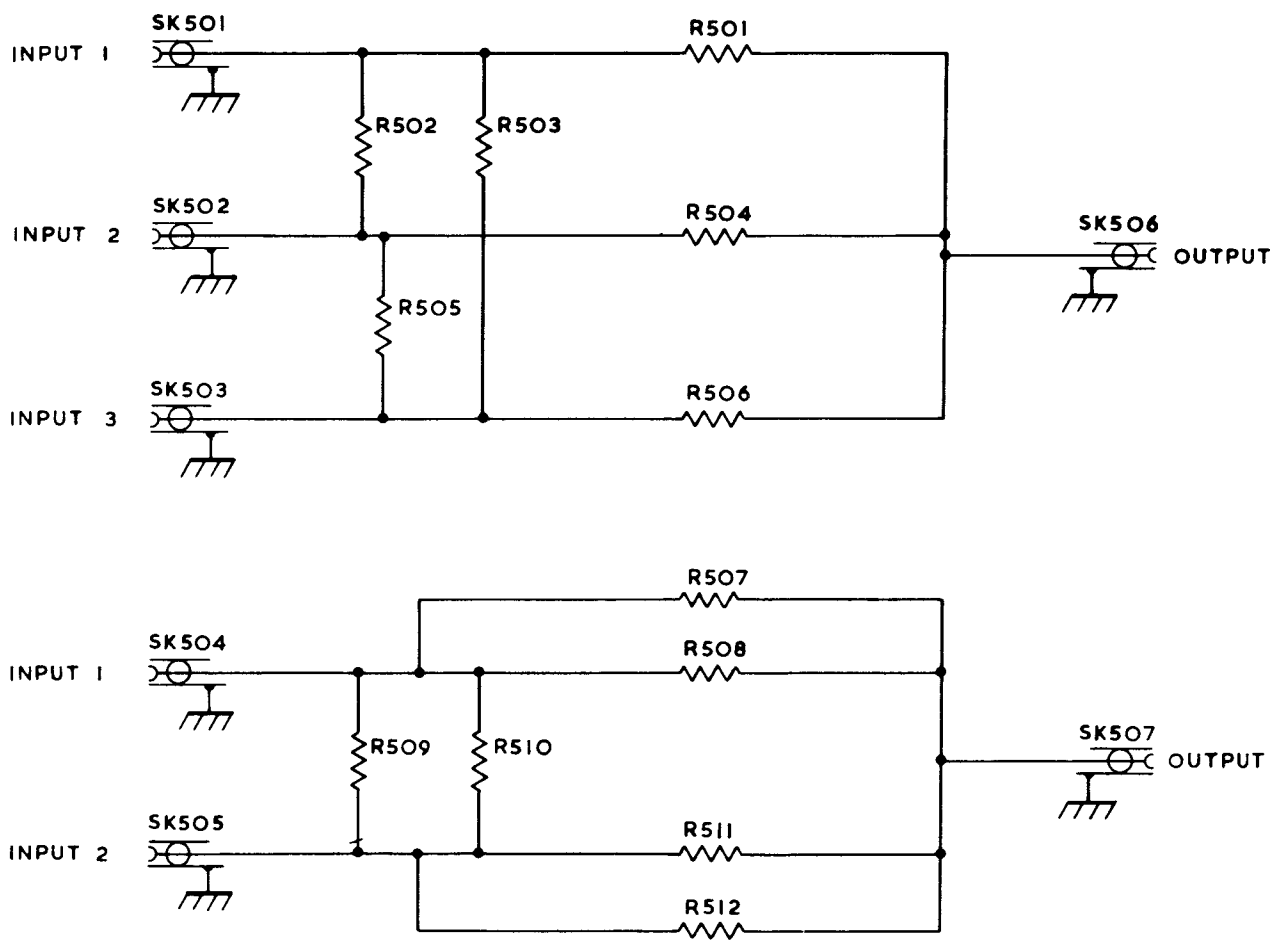


Fig. 17 CIRCUIT DIAGRAM P5

Guarantee and Service Facilities

Section 7

This instrument is guaranteed for a period of one year from its delivery to the purchaser, covering the replacement of defective parts other than tubes, semiconductors and fuses. Tubes and semiconductors are subject to the manufacturers' guarantee.

We maintain comprehensive after sales facilities and the instrument can, if necessary, be returned to our factory for servicing. The type and serial number of the instrument should always be quoted, together with full details of any fault and the service required. The Service Department can also provide maintenance and repair information by telephone or letter.

Equipment returned to us for servicing must be adequately packed, preferably in the special box supplied, and shipped with transportation charges prepaid. We can accept no responsibility for instruments arriving damaged. Should the cause of failure during the guarantee period be due to misuse or abuse of the instrument, or if the guarantee has expired, the repair will be put in hand without delay and charged unless other instructions are received.

OUR SALES, SERVICE AND ENGINEERING DEPARTMENTS ARE READY TO ASSIST YOU AT ALL TIMES.

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Raynham Road
Bishops Stortford
Herts.
Tel. 0279 55155

Printed in England

Manual Part No. 30163

Supplement for
PG52P1 and PG52P1A
Clock Generator Modules

ADVANCE
INSTRUMENTS (Sales Dept.)

Raynham Road Bishop's Stortford Herts England
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Division of ADVANCE ELECTRONICS LIMITED

Contents

Introduction

Section 1

This module provides the basic clock rates for the PG52 Modular Pulse Generator system. It covers the frequency range 0·1Hz to 30MHz. Free running, externally triggered or gated modes of operation are provided. The trigger mode can be used as an aperiodic ÷10 or ÷100 divider or initiated manually for single shot applications. A sweep facility alternatively allows the internal frequency to be controlled over any selected 10:1 range by an external input voltage.

The PG52P1A differs from the PG52P1 only in having a rotary fine control in place of edge-operated controls. The information in this handbook applies to both versions unless specifically stated.

This handbook supplement should be read in conjunction with the main frame and system handbook, Pt.No.30163.

Specification

Section 2

A single width, 2", module operating within a PG52, PG52A or PG52B main frame.

Frequency Range
0·1Hz to 30MHz continuously, in switched decade ranges with uncalibrated fine control.

Accuracy
±5% at decade steps.

Sweep
Selected decade frequency range can be swept by an input voltage of approx.+1V to +8V.
Input resistance >1K.

Gate
Output signals up to 5MHz can be gated on, by an input signal of >+5V and off by <+0·1V. The clock starts synchronously with the gate signal.
Maximum rise and fall time of input signal 1μS.
Minimum OFF signal width 0·5μS.
Input resistance >1K.

Trigger

The module may be triggered up to 10MHz by a +6V external signal or by push button.
The 'Trigger divide' facility allows input frequencies up to 2MHz to be divided by 10 or 100 before triggering.
Input resistance >1·5K.

Outputs
Two parallel output sockets provide the standard system interface signal of +10V.
A C.R.O. test point is provided.

The following description covers the detailed function and control of the module while the typical uses of the module within the system are covered in the handbook for the main frame and system.

3.1 NORMAL INTERNAL OPERATION

(a) Select the frequency/period units required, MHz/μS, KHz/mS, or Hz/Sec on the left hand bank of push buttons.

(b) Se'ect the required multiplying factor X10, X1 or X0.1 on the right hand bank of push buttons.

NOTE: The three FREQUENCY/PERIOD units buttons and the TRIG. button are inter-locked and pressing any one will release the others. Similarly, the three multiplying factor buttons are interlocked.

(c) The GATE and SWEEP buttons should not be depressed.

(d) With the fine control at the top of the panel in the CAL position, the output signal will be at the selected frequency/period within the calibration accuracy of ±5%.

Operation of the fine control away from the CAL position will increase the frequency (decrease the period) at least over a decade range (3:1 on 10MHz/0·1μS range).

The intermediate scale marks of the fine control of the PG52P1A are to allow the control to be reset rather than provide calibration. The PG52P1 has two edge operated controls with coarse and fine function.

3.2 SWEEP MODE

When the SWEEP button is depressed, the fine FREQUENCY/PERIOD control becomes inoperative. The frequency/period can now be controlled over the appropriate decade range (3:1 on 10MHz/0·1μS range) by the application of a positive voltage to the GATE/SWEEP input socket. At approximately +1V the frequency/period will be the calibrated value and the decade sweep completed at approximately +8V. The frequency/period can be swept beyond the decade range but erratic operation may result before the output signal is finally blocked off by excessive signal. The use of this facility is also discussed in section 3.6.6 of the handbook for the system.

3.3 GATE MODE

When the GATE button is depressed, no output signal is present (output level stays at approximately +10V). The application of a positive signal to the GATE/SWEEP input socket will initiate the output signal. The first negative going transition of the output signal occurs when the gate signal is applied and subsequent transisitons at the frequency as set. (The negative going transitions trigger a PWD/P2 module). When the gate signal returns to 0V, the output signal immediately returns to approximately +10V (this will not spuriously trigger a PWD/P2 module).

The output of a PWD/P2 module is normally used as a gate signal. Any other signal greater than +8V D.C. can be used. The "off" level should not be more positive than +100mV.

The rise and fall times of the gate signal should be less than 1μS. If a fast rise time is employed, the first output pulse occurs within 250nS of the application of the gate signal. Accurate gating of signals above 5MHz cannot be achieved. The minimum off signal width is 0·5μS.

The input resistance is greater than 1K.

The input socket is protected against excessive input signals up to + or -20V peak.

3.4 EXTERNAL TRIGGER MODE

Operation of the trigger button disables the internal clock With the multiplying factor selected as DIRECT, the output will switch at the frequency of any signal applied to the trigger input socket, a positive going input giving a negative going output transition.

With factors of ÷10 or ÷100 selected, the input frequency up to 2MHz will be divided by the appropriate factor using the internal digital divider circuitry. The output mark/space ratio then will be 1:4.

The trigger input is directly coupled and will operate from DC to 10MHz. The nominal input trigger point is +4V and it is recommended that the input signal drive is between 0 and +8V. Protection is provided against signals up to ±20V peak. The unit can be triggered from any low frequency sinusoid or other waveforms which cross the trigger point only twice per cycle. The input resistance is greater than 1·5K.

It is possible to use the gate facility together with external trigger. On direct trigger, the output will follow the trigger input when the gate signal is present and remain at +10V when the gate signal is absent. On trigger, ÷10 or ÷100, the dividers will be reset to their zero state for approx. 5μS when the gate signal is removed and will then continue to count. The output signal, however, remains clamped at +10V until the gate signal is re-applied, when it will follow the divider output.

3.5 MANUAL TRIGGER – SINGLE CYCLE

With the TRIGGER and DIRECT buttons depressed, a single output pulse will be generated each time the MAN. button is depressed. The latter button has a direct spring return.

3.6 OUTPUT

The standard system interface output signal is provided through two paralleled output sockets, i.e. an approximate 0 to +10V waveform from a low source impedance (less than 100Ω). It is intended to drive the inputs of other modules but it can alternatively feed any other load of impedance >500Ω. Beyond this, the output current is limited and the waveform may be seriously distorted. However, the module is protected against short circuits but should not be run continuously in this condition.

The output is also fed through a 5·6K resistor to a front panel test point. This is intended to allow a C.R.O. to examine the output waveform while the module is connected in a system.

The duty cycle of the output waveform in the normal operating mode is either approximately 1:1 or 1:4 dependent on which frequency range is selected.

The module is powered from the +20V and the -20V supplies in the main frame.

4.1 MULTIVIBRATOR AND DIVIDERS

The basic clock generator consists of an emitter-coupled multivibrator, the frequency of which can be controlled over a 10:1 range by amplitude control of the emitter excursion and controlled in decade steps by the value of capacitor switched into circuit. It is formed by VT107 and VT108. C110 and the trimmer capacitor, C131, form the timing capacitor on the MHz x 10 range, all other capacitors being disconnected. The excursion of the collector voltage of VT107 is limited between +6·2V (defined by MR118 through MR114) and the output of the emitter follower VT106, through MR112. As the wiper of the fine control potentiometer, R160, is taken more positive, its potential is transferred through VT105 and VT106 to reduce this excursion and hence the emitter excursion of VT107 and VT108, so increasing the frequency. In the PG52P1 (but not the P1A) a further fine control, R165, modifies the wiper potential of R160.

As the MHz x 1 and MHz x 0·1 ranges are selected, C116 and C117 are added to the timing capacity (via S108b and S109a) reducing the frequency accordingly. On the kHz x 10 range, C118 is added as the timing capacitor. On this and all the faster ranges, the multivibrator output from VT109 is fed directly via S104a and S108a, to the output amplifier. However, on the kHz x 1 and kHz x 0·1 ranges, C118 remains in circuit holding the frequency of the multivibrator at 10kHz while S108a directs its output signal through one or both of the decade dividers, IC101 and IC102, giving the required frequency at the output. Each complete decade divider is an integrated circuit in one dual-in-line package and is followed by an output buffer emitter follower, VT110 or VT111.

Similarly on the Hz ranges, S106a switches C119 into circuit defining the frequency of the multivibrator in the 10Hz range while the decade dividers are switched into circuit to give outputs of 1Hz and 0·1Hz. It should be noted that while the output of the multivibrator is an approximate square wave, the output of the decade dividers has a 1:4 mark/space ratio. Thus the output of the module will be 1:1 on the MHz x 10, MHz x 1, MHz x 0·1, kHz x 10 and Hz x 10 ranges, and 1:4 on the other ranges.

R161, R162 and R163 are switched into circuit on the MHz, kHz and Hz ranges respectively, to give fine control of the emitter current of VT107 and VT108, thus acting as calibration presets for those ranges.

4.2 OUTPUT STAGE

The output signal from the multivibrator or the decade dividers is fed via S104b to the emitter-coupled pair, VT114 and VT115. The output from the collector of VT115 is fed through the zener diode, MR122, to operate VT117 as a saturated switch. The 0 to +10V collector voltage swing of this stage is buffered by the emitter followers, VT118 and VT119. These provide a low output impedance drive to the two output sockets, SKC and SKD, and are protected against accidental short circuit of the output by R153, R155, R156 and R157.

4.3 SWEEP

When this function is selected, S102 connects the gate/sweep input socket SKA in place of the fine control potentiometer, R160. This allows the sweep input signal to control the multivibrator frequency over the frequency range selected by the push buttons. MR104, MR105 and MR106 with R103, protect the circuitry against excessive input signals.

4.4 GATE

When the gate function is selected, S101 operates. If the input signal on SKA is positive; the transistor switch, VT104, is turned on. MR111 is reverse biased and the circuit operates normally.

When the input signal drops to 0V, VT104 is turned off. Its collector potential rises, MR111 conducts reverse biassing MR110 and taking the multivibrator control voltage on the emitter of VT106 more positive than the potential of MR118, thus inhibiting the multivibrator action.

The positive signal on the collector of VT104 is also transferred through the emitter of VT116 to the base of VT115, turning off the latter transistor irrespective of the base potential on VT114. The output voltage is thus clamped at its positive level.

The final effect of turning off VT104 is to turn on VT112 momentarily through C122. This pulse is transferred through C123 to give a short positive pulse at the collector of VT113 which resets both decade dividers to their '0' state.

When the gate is opened by returning the input signal positive, VT104 is turned on again, removing the clamp from the multivibrator and from the output stage and allowing the normal operation to start in synchronism with the gate signal.

4.5 TRIGGER

When 'trigger' is selected, S104a disconnects the output of the multivibrator and connects in its place the output of a separate trigger circuit. This circuit is a Schmitt trigger formed by VT101 and VT102. It can be driven either by an input signal on SKB or, in a 'single shot' mode, by the push button, S103.

The modular construction of the PG52 allows fault location by substitution. Any module suspected of being at fault can be replaced by another module to confirm the suspected fault to be within one module. Full or partial failure of all modules is probably due to a fault in the common power supply or its distribution in the main frame. The fuses should be checked and also the potentials on the +20V and −20V lines. A fault within one module, taking excessive current from ont of the lines can overload the line and degrade the performance of the other modules.

When a fault is localised within the power supply or any one module, the faulty part can be returned to the factory for repair or further investigation can be carried out with the help of the relevant circuit diagram and circuit description. Component replacement in any module may require it to be recalibrated.

The circuitry of the module is all solid-state and as such should require no regular maintenance. Stiff action of the push button switches can be overcome by the sparing use of a switch lubricant.

5.1 ACCESS

Access to the circuitry of each module is easily obtained by removing the two covers. Any module can be operated out of the main frame on a suitable extension lead. The necessary plug and sockets are from the STC ISEP range, plug type 12 - 212 - 110, Advance Pt. No. 26459 socket type 13 - 302 - 201, Advance Pt. No. 25301.

5.2 FAULT LOCATION AND CALIBRATION

Faults within this module can be localised by checking the various functions. Correct operation on the external trigger mode when internal clock operation is faulty points to a fault in the multivibrator. Faulty operation on trigger but not on internal mode, points to the trigger circuit. Correct operation on the Hz x 10 and kHz x 10 ranges with faults on the Hz x 1, Hz x 0·1, kHz x 1 and kHz x 0·1 ranges points to a fault on the decade divider circuitry or range switching. The module should only require setting up and re-calibration if components are changed.

After checking the incoming +20V and −20V line potentials to be correct within 200mV, the following calibration sequence should be carried out:−

(1) Select MHz x 1 range, adjust R164 if necessary to obtain an output signal. Adjust R161 for correct output frequency at 'CAL' end of fine control.

(2) Rotate fine control to max. frequency position. The output frequency should be between 11MHz and 13MHz. The factory preset potentiometer, R159, should be adjusted to correct this frequency. Return the fine control to 'CAL'.

(3) Select MHz x 10. Adjust C131 for correct output frequency. Select MHz x 1 range, adjust R164 if necessary to obtain an output signal. Adjust R161 for correct output frequency at 'CAL' end of fine control.

(4) Check frequency on MHz x 0·1 range. This should be within specification. C116 and C117 are selected to be of the required ratio and R161 controls both the MHz x 1 and the MHz x 0·1 range.

(5) Select kHz x 10 range and adjust R162 for the correct output frequency.

(6) Select the Hz x 10 range and adjust R163 for the correct output frequency.

(7) Set R164 to obtain a satisfactory output signal over the whole of the 1 to 10MHz range and from 10 to 30MHz on the 10MHz range.

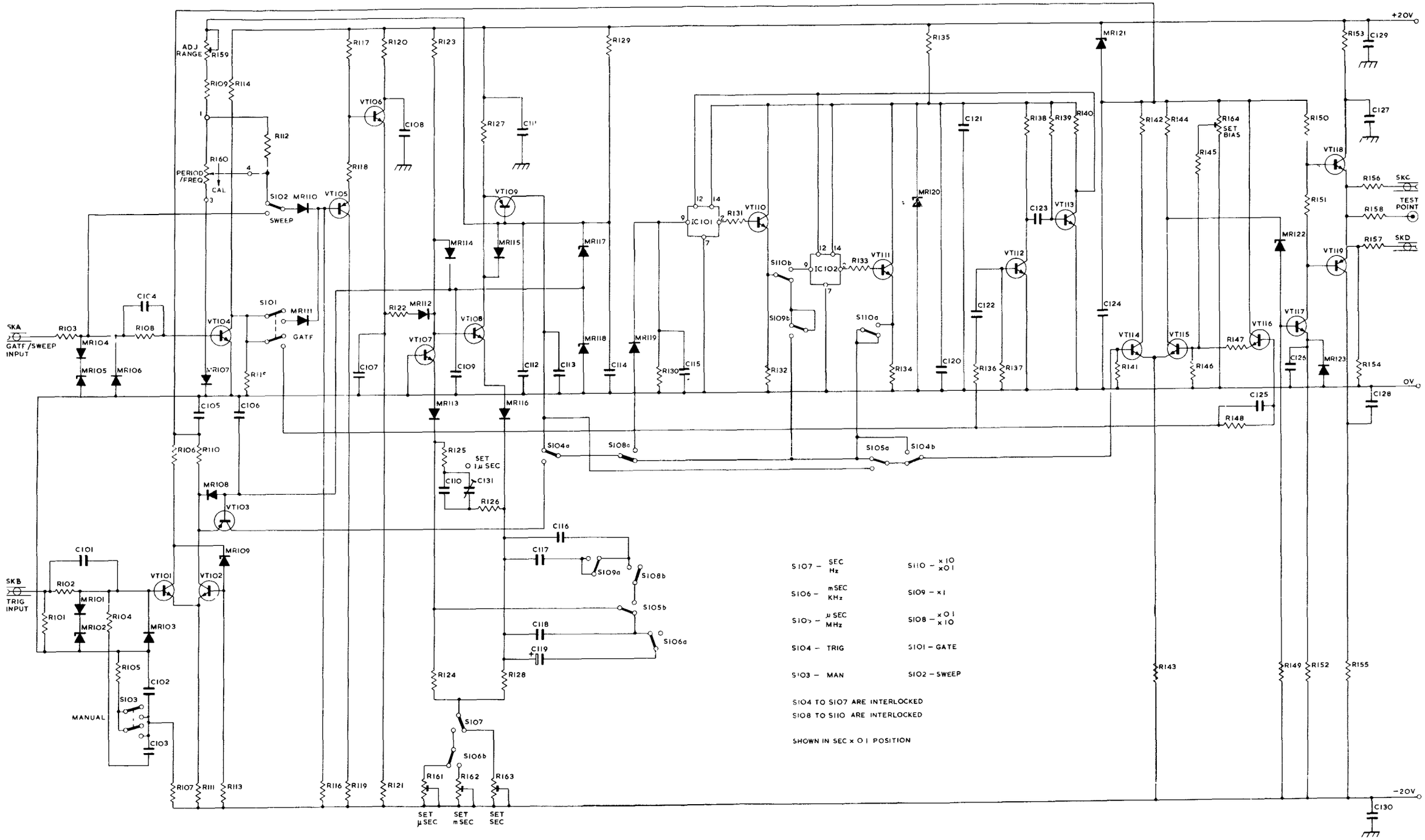
CLOCK GENERATOR

Ref	Value	Description	Tol%±		Part No.
RESISTORS					
R101	10k	Cr. Carbon	5	1/8W	11503
R102	1.5k	Cr. Carbon	5	"	385
R103	560	Cr. Carbon	5	"	308
R104	6.8k	Cr. Carbon	5	"	313
R105	220	Cr. Carbon	5	"	304
R106	100	Cr. Carbon	5	"	11504
R107	1M	Cr. Carbon	5	"	766
R108	8.2k	Cr. Carbon	5	"	927
R109	1.2k	Cr. Carbon	5	"	2087
R110	270	Cr. Carbon	5	"	2716
R111	1.2k	Cr. Carbon	5	"	18551
R112	1k	Cr. Carbon	5	"	384
R113	10k	Cr. Carbon	5	"	11503
R114	5.6k	Cr. Carbon	5	"	787
R115	5.6k	Cr. Carbon	5	"	787
R116	100k	Cr. Carbon	5	"	319
R117	4.7k	Cr. Carbon	5	"	386
R118	330	Cr. Carbon	5	"	1894
R119	220	Cr. Carbon	5	"	304
R120	220	Cr. Carbon	5	"	304
R121	22k	Cr. Carbon	5	"	1544
R122	39	Cr. Carbon	5	"	3010
R123	2.7k	Cr. Carbon	5	"	311
R124	2.7k	Cr. Carbon	5	"	311
R125	5.6	RRC LX	10		26453
R126	5.6	RRC LX	10		26453
R127	1.5k	Cr. Carbon	5	1/8W	385
R128	3.3k	Cr. Carbon	5	"	1638
R129	470	Cr. Carbon	5	½W	18546
R130	270	Cr. Carbon	5	1/8W	2716
R131	100	Cr. Carbon	5	"	11504
R132	2.2k	Cr. Carbon	5	"	425
R133	100	Cr. Carbon	5	"	11504
R134	2.2k	Cr. Carbon	5	"	425
R135	150	RWV4-J	5		19085
R136	6.8k	Cr. Carbon	5	1/8W	313
R137	4.7k	Cr. Carbon	5	"	386
R138	1k	Cr. Carbon	5	"	384
R139	3.3k	Cr. Carbon	5	"	1638
R140	150	Cr. Carbon	5	"	301
R141	120	Cr. Carbon	5	"	735
R142	100	Cr. Carbon	5	"	11504
R143	1.5k	Cr. Carbon	5	½W	18552
R144	220	Cr. Carbon	5	1/8W	304
R145	1.2k	Cr. Carbon	5	"	2087
R146	330	Cr. Carbon	5	"	1894
R147	330	Cr. Carbon	5	"	1894
R148	2.7k	Cr. Carbon	5	"	311
R149	3.3k	Cr. Carbon	5	"	1638
R150	470	Cr. Carbon	5	"	1373
R151	22	Cr. Carbon	5	"	723
R152	560	Cr. Carbon	5	1W	19040
R153	330	Cr. Carbon	5	1W	19037
R154	1k	Cr. Carbon	5	1/8W	384
R155	560	Cr. Carbon	5	1W	19040
R156	33	Cr. Carbon	5	½W	18532
R157	33	Cr. Carbon	5	½W	18532
R158	5.6k	Cr. Carbon	5	1/8W	787
R159	470	Cont. Pot Plessey MPD/PC			28524
R160	4.7k	Cont. Pot.			A4/30127
R161	1k	Cont. Pot Plessey MPD/PC			26870
R162	1k	Cont. Pot Plessey MPD/PC			26870
R163	1k	Cont. Pot Plessey MPD/PC			26870
R164	2.2k	Cont. Pot Plessey MPD/PC			24561

Ref	Value	Description	Tol%±		Part No.
CAPACITORS					
C101	10pF	G.P. Ceramic			22364
C102	.047μF	Lemplac 1212k			2793
C103	.01μF	G.P. Ceramic			22395
C104	47pF	G.P. Ceramic			22372
C105	0.1μF	Lemlac	+80 -20	30V	19647
C106	0.1μF	Lemlac	+80 -20	30V	19647
C107	220pF	G.P. Ceramic			22379
C108	0.1μF	Lemlac	+80 -20	30V	19647
C109	0.1μF	Lemlac	+80 -20	30V	19647
C110	27pF	Lemco 1106R Insul.	5		18454
C111	0.1μF	Lemlac	+80 -20	30V	19647
C112	0.1μF	Lemlac	+80 -20	30V	19647
C113	5.6pF	G.P. Ceramic			22361
C114	0.1μF	Lemlac	+80 -20	30V	19647
C115	100pF	G.P. Ceramic			22376
C116	470pF	Suflex Polystyrene Type H5	2½	30V	26444
C117	4700pF	Suflex Polystyrene Type H5	2½	30V	26445
C118	.047μF	Mullard Polyester C296 AA/A	10	160V	792
C119	47μF	Kemet K47J15K	10	15V	4456
C120	0.1μF	Lemlac	+80 -20	30V	19647
C121	25μF	C426 AR/F25		25V	20776
C122	1000pF	G.P. Ceramic			22387
C123	5600pF	G.P. Ceramic			22394
C124	0.1μF	Lemlac	+80 -20	30V	19647
C125	68pF	G.P. Ceramic			22374
C126	0.1μF	Lemlac	+80 -20	30V	19647
C127	0.1μF	Lemlac	+80 -20	30V	19647
C128	0.1μF	Lemlac	+80 -20	30V	19647
C129	0.1μF	Lemlac	+80 -20	30V	19647
C130	0.1μF	Lemlac	+80 -20	30V	19647
C131	12pF	Trimmer Mullard COO4EA/12E			26446

CLOCK GENERATOR (cont.)

Ref	Value	Description	Tol%±	Part No.
DIODES				
MR101		1N 916		1949
MR102		Zener 4.7V		4073
MR103		1N 914		23802
MR104		1N 916		1949
MR105		Zener 12V		4031
MR106		1N 914		23802
MR107		1N 914		23802
MR108		1N 916		1949
MR109		Zener 8.2V		3798
MR110		1N 914		23802
MR111		1N 914		23802
MR112		BAY 71		27571
MR113		BAY 71		27571
MR114		BAY 71		27571
MR115		BAY 71		27571
MR116		BAY 71		27571
MR117		Zener 2.7V		21002
MR118		Zener 6.2V		4032
MR119		1N 914		23802
MR120		Zener 3.6V		3814
MR121		Zener 8.2V		3798
MR122		Zener 8.2V		3798
MR123		1N 916		1949
TRANSISTORS				
VT101		BSX 20		23307
VT102		BSX 20		23307
VT103		BSX 29		25740
VT104		BSX 20		23307
VT105		2N 3906		21533
VT106		BSX 20		23307
VT107		BSX 27		24118
VT108		BSX 27		24118
VT109		BSX 29		25740
VT110		BSX 20		23307
VT111		BSX 20		23307
VT112		BSX 20		23307
VT113		BSX 20		23307
VT114		BSX 28		25739
VT115		BSX 28		25739
VT116		BSX 20		23307
VT117		BSX 28		25739
VT118		2N 3904		24146
VT119		2N 3906		21533
INTEGRATED CIRCUITS				
IC101		Fairchild 69-958-79		
		Unselected		26511
IC102		Fairchild 69-958-79		25873
SOCKETS				
SKA		BNC 50		1222
SKB		BNC 50		1222
SKC		BNC 50		1222
SKD		BNC 50		1222
SWITCHES				
S101-S102		Push button		26447
S103-S107		Push button		26448
S109-S110		Push button	Part of S101/S102	26447



CLOCK GENERATOR CIRCUIT DIAGRAM

Supplement for PG52P3, PG52P3A and PG52P13 Standard and Modulated Output Modules

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Introduction

Section 1

The P3, P3A and P13 output modules for the PG52 system, provide outputs into 50Ω with rise and fall times typically 5nS. The positive and negative levels of the output pulse may be varied independently over the range 0 to +10V and 0 to −10V respectively. (i.e. 20V pk/pk). Attenuated ranges allow those levels to be reduced successively from 10V to 100mV.

A pulse invert facility allows both the generation of negative pulses and output duty cycles approaching 100%. The two input sockets allow the generation of output pulses from two independent sources.

The P3A differs from the P3 only in having rotary rather than edge-operated controls for setting positive and negative level. The P13 module is similar to the P3A, but it only has one input and it includes amplitude modulation facilities. An externally applied signal can be switched to control the positive level, the negative level or both, over-riding the appropriate manual controls. The information in this supplement applies to all three modules except where specifically stated.

This handbook supplement should be read in conjunction with the main frame and system handbook, Pt. No.30163.

Single width. 2", modules operating in a PG52, PG52A or PG52B main frame.

2.1 PG52P3 and PG52P13

Output Levels: Positive and negative levels independently adjustable up to +10V and −10V respectively, into 50Ω. Push button attenuator with uncalibrated fine control, gives output ranges of 10V, 5V, 2.5V, 1V, 0.5V, 0.25V and 0.1V. Accuracy ±5% with fine control in calibrate position.

Output Impedance: 50Ω on all ranges except ±10V. Low impedance on ±10V range.

Rise Time: Rise and fall times <7nS (typically 5nS).

Perturbations: Preshoot, overshoot etc., less than 5% of maximum pulse height on ±10V range.

On all attenuated ranges perturbation will be typically 5% of maximum pulse height +20mV.

Protection: Output protected against open and short circuits.

Input: Two input sockets operating with an 'OR' function to +10V input signals.

Maximum input rise time 20nS.

Input resistance>3K

Maximum input voltage ±20V pk.

Normally intended to be driven from standard PG52 system interface signals.

Maximum input frequency is 25MHz

Minimum input pulse width is 20nS

2.2 PG52P13

As PG52A but with single pulse input only.

POS. LEVEL MODULATION

Pos. output level controlled 0 to +10V by 0 to +10V (±1V) input signal. Crosstalk to neg. level better than −30dB.

NEG. LEVEL MODULATION

Neg. output level controlled 0 to −10V by 0 to +10V (±1V) input signal. Crosstalk to pos. level better than −30dB.

Pos. and neg. modulation selected simultaneously will allow pos. and neg. output levels to be controlled, 1 to 10V, symmetrical about 0V.

Mod. I/P resistance >10K.
Max. I/P voltage ±20V pk.
Output slew rate better than
50V/mS (increasing amplitude)
10V/mS (decreasing amplitude)

The following description covers the detailed function and control of the modules while the use of the modules within the system is covered by the handbook for the main frame and system.

3.1 INPUT

The switching inputs of the modules are intended to be driven from standard +10V PG52 system interface signals from one of the range of waveform generating or processing modules. A positive signal on either of the input sockets with that input selected by the appropriate push button, will normally give an output transition from the selected negative level to the selected positive level. The output will return to the negative level only when both inputs are at 0V. (The P13 version has only one switching input and hence this OR function to positive inputs does not apply, the output being at the positive level when the one input is at +10V).

The output levels are reversed when the INVERT button is pressed, the output being negative while either input is positive and being positive while both inputs are at 0V.

Other pulse sources of 10V but less than ±20V pk. can be used as inputs, if their rise times are less than 20nS. The input resistance is greater than 3K.

The minimum specified input pulse width is 25nS but it will typically operate down to 16nS. The unit will operate up to a p.r.f. of 25MHz and typically, up to 30MHz. This limitation is a function of selected output levels.

3.2 AMPLITUDE CONTROL

Independent control of the positive and negative levels of the output pulse between 0 and +10V and 0 and −10V respectively, is provided by the two fine controls at the top of the panel. Each level is defined within 5% of 10V at the maximum end, when loaded by 50Ω. The module should not normally be operated with the level controls less than the equivalent of 1V apart. The attenuator is provided for low level outputs.

3.3 ATTENUATOR

The full +10V to −10V output into 50Ω is provided at the output socket when the DIRECT ±10V button is depressed.

The level can be attenuated to ±5V, ±2V or ±1V by operation of the appropriate button. Further attenuation to ±0.5V, ±0.2V and ±0.1V can be obtained by depressing the ÷10 button. The ÷10 facility is not available with the ±10V output control.

3.4 WAVESHAPE

When terminated by 50Ω, the output rise and fall times for any large step on the ±10V range will be 6nS or less (typically 5nS). The perturbations or preshoot, overshoot, etc., will be less than 5% of the maximum amplitude. The unit is dc coupled and droop is negligible.

The use of the attenuator may introduce a further 1nS to the rise time together with extra perturbations etc. of 20mV (50mV above 10MHz) noticeable only on the lower ranges.

It is pointed out that low level pulse waveforms without the added perturbations can be obtained if external 50Ω coaxial attenuators are used in the output lead.

3.5 OUTPUT IMPEDANCE AND TERMINATION

The unit provides a low output impedance on the DIRECT ±10V range and 50Ω output impedance on the attenuated ranges. It is intended to be used into a 50Ω coaxial system and only under these conditions will the full output rise time and perturbation specification be met. It is pointed out that excessive overshoot etc. is generated if the output is not connected to the load via a 50Ω coaxial cable such as the PL43 supplied. This must subsequently be correctly terminated with a non-reactive 50Ω resistance. If a high impedance load is to be driven, the 50Ω termination, TP19, supplied should be used at the load end of the cable. With the limitation of excessive over-shoot, the unit can be used into high impedance loads on any range. Approx. twice the stated output voltage will appear on the attenuated ranges. Not more than ±11V will appear on the DIRECT ±10V range.

The attenuated ranges can also be used to drive into low impedance or short circuit loads. The DIRECT ±10V range cannot be driven into loads less than 50Ω. The output is protected against short circuit but should not be run under continuous overload on this range.

3.6 PROPAGATION DELAY

The propagation delay between the application of an input pulse and the subsequent output transition is approx. 20nS for normal outputs and 25nS for inverted. There is also a possible differential delay of 3nS between positive and negative-going edges.

3.7 MODULATION P13 ONLY

Until the POS. LEVEL or the NEG. LEVEL buttons are pressed, the P13 module operates as a P3 or P3A module with only one input.

Operation of the POS. LEVEL button disables the POS. LEVEL control at the top of the panel and its function is taken by the voltage applied to the modulation input socket. The 0 to +10V range of output level is obtained by a similar +10V input range with an approx. +0.7V offset, i.e. +1.7V input is equivalent to +1V output and +10.7 input is equivalent to +10V output, the relationship between being approximately linear. The output level can only be controlled over the normal 0 to +10V range.

Operation of the NEG. LEVEL button only, similarly disables the NEG.LEVEL control and the same positive input voltage which defined the positive level above, controls the neg. output level from 0 to -10V, i.e. increasing input from approx. +0.7V to +10.7V takes the neg. output level from 0 to -10V.

Simultaneous operation of both buttons then disables both level controls and a positive-going modulation input gives diverging pos. and neg. output levels from

0V to +10V and -10V respectively, approximately symmetrical about OV.

The modulation input circuitry is protected against excessive inputs up to ±20V pk. The input resistance is greater than 10K. The rate of response of the output levels is limited to 50V/mS for increasing output amplitude and 10V/mS for decreasing amplitude. With the modulation input open circuited, the output is biassed to approximately 5V. This allows ac coupled input signals to modulate the output about the mid point of its range.

It will be appreciated, that the modulation facility can be used in one of two ways :–

(a) A low frequency input signal can modulate the amplitude of a fast pulse waveform. This signal could be a dc. derived from an external source and the module used as a programmeable output unit.

or (b) A relatively slow switching input can be used to chop off parts of a modulating waveform.

In the absence of a switching input, the output will follow directly or be the inverse of the modulation input. The Invert button will determine whether the output sits at the pos. or neg. level and the appropriate modulation should be selected.

The modules operate from the +20V and -20V supplies in the main frame. P3 and P3A are identical in their circuitry. The following description applies to all modules except for the final section which describes the additional modulation circuitry of the P13. Transistors are designated 'TR' and diodes 'D' on the P13 circuit, as against 'VT' and 'MR' on the P3 and P3A and used in the following text. The reference numbers are identical however.

4.1 INPUT SWITCHING

The A and B input signals drive VT302 and VT303 respectively as saturated switches. A positive input on either will rapidly switch their common collector point from +20V to 0V. The negative-going edge of an input pulse is coupled via C301 or C302 to turn on VT301 for a short period, giving a rapid return to the common collector point of +20V at the end of an input pulse.

The resultant signal from this common collector point is fed directly (in the normal mode) or via a similar inverting stage, VT304 and VT305, (in the INVERT mode) to a complementary emitter follower stage, VT306 and VT307. This output is in turn level shifted by the zener diodes, MR306 and 307 to drive the complementary saturated switch pair, VT309 and VT310. VT308 provides a constant current load for this shift network.

4.2 LEVEL CONTROL AND OUTPUT

The emitter potential of VT309 can be controlled approximately between 0 and +10V on the +V line by the positive level control. Similarly the emitter potential of VT310 can be controlled between 0 and -10V on the -V line by the negative level control. Thus the common collector point of these two switching transistors is rapidly switched between +V and -V as one of the other of these transistors is switched on. The base biasing is so arranged that always one but never both of the pair are on at any one time. MR312 provides a small bias to the double emitter follower output pair, VT311 and VT312, with their common emitter junction being switched directly or through the attenuator network, to the output socket.

4.3 POWER SUPPLIES

The +V line is generated by the cascaded emitter followers VT314 and VT313, from the wiper potential of the positive level control, R350. R234 and R235 prevent excessive current from damaging the output stage if the output is short circuited.

The preset controls, R349 and R351, set the maximum output voltages to +10V and -10V respectively. On the P3, resistors R336 and 337 are selected during factory test to define the OV level of the controls. On the P13, preset controls R329 and R330 are used for this.

4.4 MODULATION (P13 only)

When the POS LEVEL modulation switch S301 is operated, the base of TR314 (the potential of which determines the +V line voltage) is transferred from the wiper of the POS LEVEL control, R350, to the modulation input signal. The latter is via the emitter follower TR317 and the level shifting diodes, D313 and D314.

Transistors, TR318, 319 and TR320, form an inverting amplifier with unity gain, such that the collector potential of TR320 goes negative as the modulation input voltage goes positive. Thus when the NEG.LEVEL modulation switch, S302, is operated, the -V line voltage is controlled by the modulation input rather than the NEG LEVEL control, R352.

The modular construction of the instrument allows fault location by substitution. Any module suspected of being at fault can be replaced by another module to confirm the suspected fault to be within one module. Full or partial failure of all modules is probably due to a fault in the common power supply or its distribution in the main frame. The fuses should be checked and also the potentials on the +20V and -20V lines. A fault within one module, taking excessive current from one of the lines can overload the line and degrade the performance of the other modules.

When a fault is localised within the power supply or any one module the faulty part can be returned to the factory for repair, or further investigation can be carried out with the help of the relevant circuit diagram and circuit description. Component replacement in any module may require it to be recalibrated.

5.1 ACCESS

Access to the circuitry of each module is easily obtained by removing the two covers. Any module can be operated out of the main frame on a suitable extension lead. The necessary plug and sockets are from the S.T.C. 1 SEP range, plug type 12 – 212 – 110 > Advance pt. no.26459
socket type 13 – 302 – 201 > Advance pt. no.25301

5.2 FAULT LOCATION AND SETTING-UP SEQUENCE

Faults within this module can best be located by following the signal path through the various switching stages to the output.

The P13 should be made to function in its normal mode before introducing the external level control.

If the output signal cannot be controlled in the negative direction, it is likely that there is a fault on the -V line. Similarly, lack of control in the positive direction is probably due to failure of the +V line. Power supply checks should first be carried out on the incoming +20V and -20V lines. These should be set within +200mV of the nominal 20V. The +V and -V lines should be capable of control from approx. +1V to +11V and -1V to -11V respectively, the actual levels being set as described later. Signal levels through the switching stage up to the common collectors of VT406 and VT407, should be approximately 0 to +20V.

The common collector of VT309 and VT310 should swing between the +V and -V lines, less the voltage drops in MR310 and MR311, and the output voltage from VT311 and VT312 should follow.

The only calibration necessary is to set the range of the front panel level controls to 10V at maximum and 0V at minimum. This should be checked on the 10V, direct output range driving into a 50Ω load.

The +10V level should be set by R349 (set +10V) with the pos. level at maximum, neg. level at minimum. At the same time, R330 (set -0V) should be set on a P13 module or R337 changed on a P3 or P3A.

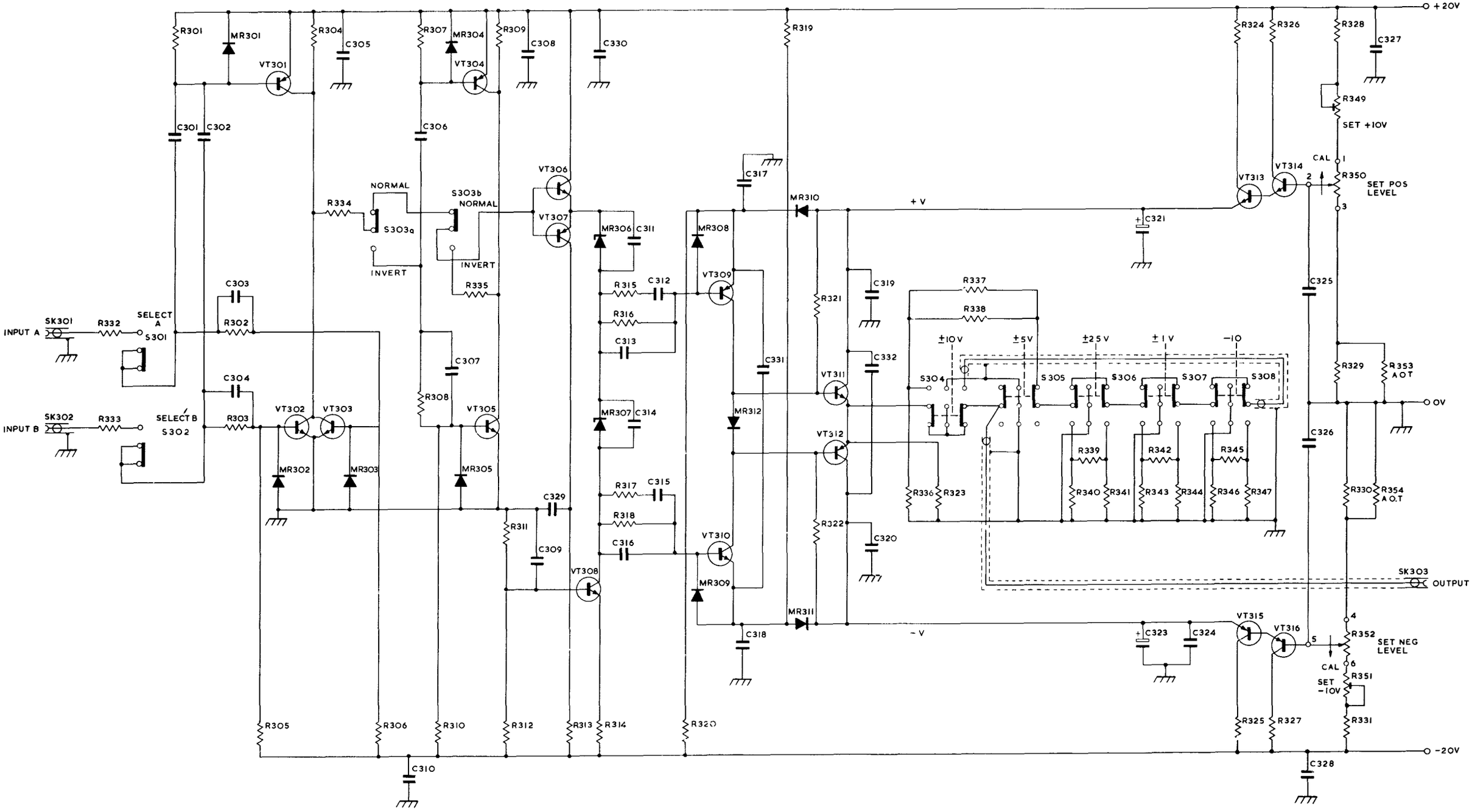
The -10V level should be set by R351 (set -10V) with the neg. level at maximum and the pos. level at minimum. At the same time, R329 (set +0V) should be set on a P13 module or R336 changed on a P3 or P3A. These changes should only be necessary if other components have been changed in the power supply or output stage circuitry.

PG52 P3

Ref	Value	Description	Tol%±		Part No.
RESISTORS					
R301	1K	Cr. Carbon	5	1/8W	384
R302	4.7K	Cr. Carbon	5	"	386
R303	4.7K	Cr. Carbon	5	"	386
R304	3.3K	Cr. Carbon	5	"	1638
R305	15K	Cr. Carbon	5	"	315
R306	15K	Cr. Carbon	5	"	315
R307	2.2K	Cr. Carbon	5	"	425
R308	18K	Cr. Carbon	5	"	634
R309	3.3K	Cr. Carbon	5	"	1638
R310	68K	Cr. Carbon	5	"	1636
R311	3.3K	Cr. Carbon	5	"	1638
R312	470	Cr. Carbon	5	"	1373
R313	1K	Cr. Carbon	5	"	384
R314	220	Cr. Carbon	5	"	304
R315	100	Cr. Carbon	5	"	11504
R316	10K	Cr. Carbon	5	"	11503
R317	100	Cr. Carbon	5	"	11504
R318	10K	Cr. Carbon	5	"	11503
R319	2.7K	Cr. Carbon	5	½W	18555
R320	2.7K	Cr. Carbon	5	½W	18555
R321	2.2K	Cr. Carbon	5	1/8W	425
R322	2.2K	Cr. Carbon	5	"	425
R323	1K	Cr. Carbon	5	"	384
R324	33	RRC LG75	5	—	2277
R325	33	RRC LG75	5	—	2277
R326	330	Cr. Carbon	5	1W	19037
R327	330	Cr. Carbon	5	1W	19037
R328	470	Cr. Carbon	5	1/8W	1373
R329	150	Cr. Carbon	5	"	301
R330	220	Cr. Carbon	5	"	304
R331	470	Cr. Carbon	5	"	1373
R332	47	Cr. Carbon	5	"	727
R333	47	Cr. Carbon	5	"	727
R334	47	Cr. Carbon	5	"	727
R335	47	Cr. Carbon	5	"	727
R336	100	Electrosil TR8	1	"	21870
R337	100	Electrosil TR6	1		23507
R338	100	Electrosil TR6	1		23507
R339	37.4	Electrosil C5	1		26479
R340	150	Electrosil TR6	1		26480
R341	150	Electrosil TR6	1		26480
R342	120	Electrosil C5	1		26481
R343	75	Electrosil TR6	1		21866
R344	75	Electrosil TR6	1		21866
R345	249	Electrosil C5	1		26482
R346	61	Electrosil TR6	1		21867
R347	61	Electrosil TR6	1		21867
R348	47	Cr. Carbon	5	1/8W	727
R349	220	Cont.Pot Davall Type 80			25229
R350	1K	Cont.Pot Plessey W.M.P.			27156
R351	220	Cont. Pot Davall Type 80			25229
R352	1K	Cont. Pot Plessey W.M.P.			27156
R353		A.O.T.			
R354		A.O.T.			
CAPACITORS					
C301	10pF	G. P. Ceramic			22364
C302	10pF	G. P. Ceramic			22364
C303	33pF	G. P. Ceramic			22370
C304	33pF	G. P. Ceramic			22370
C305	0.1μF	Lemlac	+80 -20	30V	19647
C306	10pF	G. P. Ceramic			22364
C307	22pF	G. P. Ceramic			22368
C308	0.1μF	Lemlac	+80 -20	30V	19647
C309	0.1μF	Lemlac	+80 -20	30V	19647
C310	0.1μF	Lemlac	+80 -20	30V	19647
C311	.01μF	G. P. Ceramic			22395
C312	22pF				22368
C313	5.6pF	G. P. Ceramic			22361
C314	0.1μF	G. P. Ceramic			22395
C315	22pF	G. P. Ceramic			22368
C316	5.6pF	G. P. Ceramic			22361
C317	0.1μF	Lemlac	+80 -20	30V	19647
C318	0.1μF	Lemlac	+80 -20	30V	19647
C319	0.1μF	Lemlac	+80 -20	30V	19647
C320	0.1μF	Lemlac	+80 -20	30V	19647
C321	100μF	C437 AR/G100		40V	20779
C323	100μF	C437 AR/G100		40V	20779
C324	0.1μF	Lemlac	+80 -20	30V	19647
C325	0.1μF	Lemlac	+80 -20	30V	19647
C326	0.1μF	Lemlac	+80 -20	30V	19647
C327	0.1μF	Lemlac	+80 -20	30V	19647
C328	0.1μF	Lemlac	+80 -20	30V	19647
C329	0.1μF	Lemlac	+80 -20	30V	19647
C330	.01μF	G. P. Ceramic			22395
C331	0.1μF	Lemlac	+80 -20	30V	19647
C332	0.1μF	Lemlac	+80 -20	30V	19647

PG52 P3 (cont.)

Ref	*Value*	*Description*	*Tol%±*	*Part No.*
TRANSISTORS				
VT301		2N 3906		21533
VT302		2N 3904		24146
VT303		2N 3904		24146
VT304		2N 3906		21533
VT305		2N 3904		24146
VT306		2N 3904		24146
VT307		2N 3906		21533
VT308		C 424		21871
VT309		2N 4080		25862
VT310		BSX 28		25739
VT311		MT 3725		25863
VT312		MT 3726		25864
VT313		40250		4224
VT314		2N 3053		4039
VT315		MJ 3701		22624
VT416		MM 1614		19320
DIODES				
MR301		1N 916		1949
MR302		1N 916		1949
MR303		1N 916		1949
MR304		1N 916		1949
MR305		1N 916		1949
MR306		Zener ZF.3.9		3817
MR307		Zener ZF12		4031
MR308		1N 916		1949
MR309		1N 916		1949
MR310		1N 916		1949
MR311		1N 916		1949
MR312		BAY 82		25865
SWITCHES				
S301		Push button		26572
S302		Push button		26572
S303		Push button		26572
S304		Push button		26571
S305		Push button		26571
S306		Push button		26571
S307		Push button		26571
S308		Push button		26571



NOTES –
1 S304 TO S307 ARE INTERLOCKED

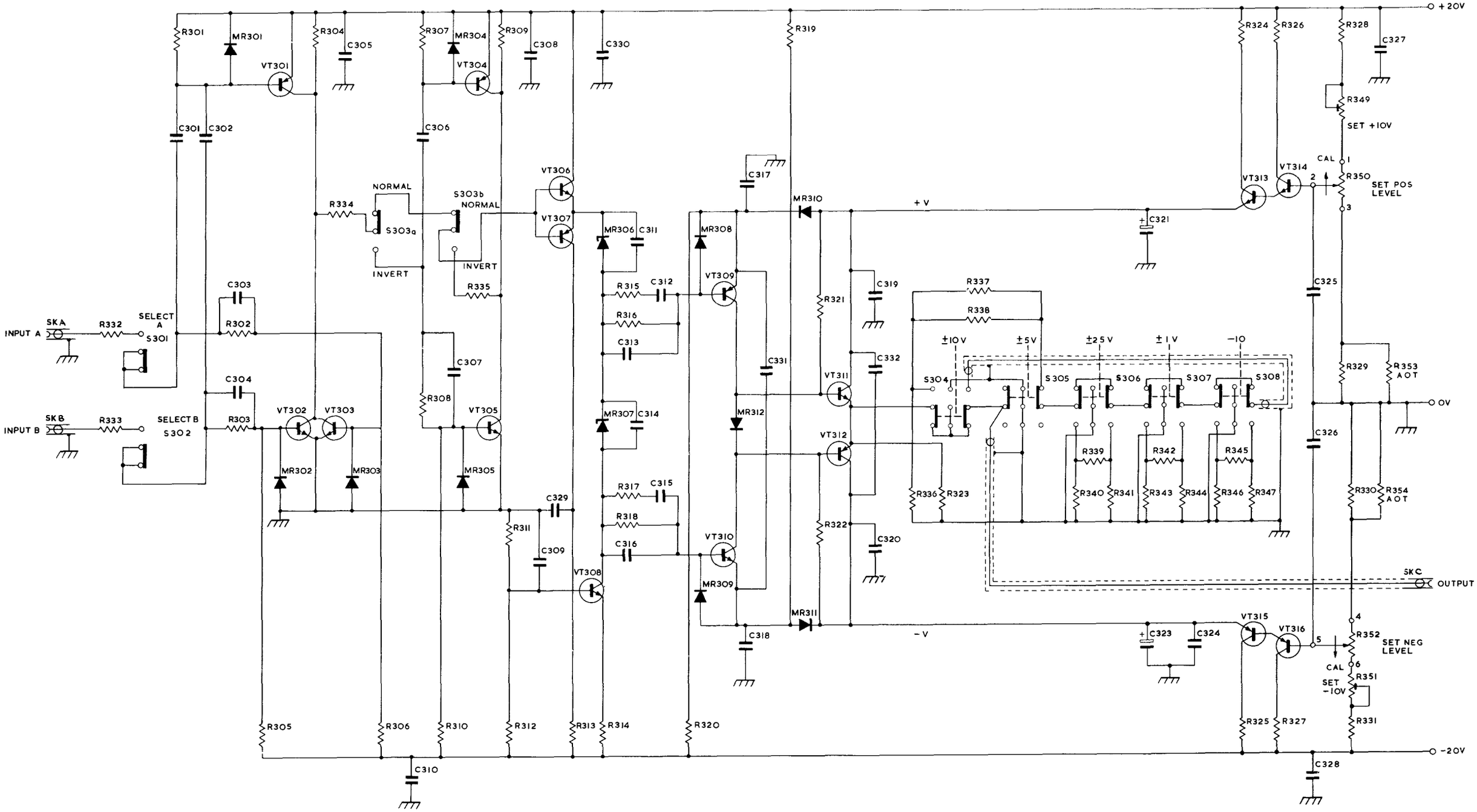
PG52 P3 STANDARD OUTPUT CIRCUIT DIAGRAM

PG52 P3A

Ref	Value	Description	Tol%±		Part No.
RESISTORS					
R301	1k	Cr. Carbon	5	1/8W	384
R302	4.7k	Cr. Carbon	5	1/8W	386
R303	4.7k	Cr. Carbon	5	1/8W	386
R304	3.3k	Cr. Carbon	5	1/8W	1638
R305	15k	Cr. Carbon	5	1/8W	315
R306	15k	Cr. Carbon	5	1/8W	315
R307	2.2k	Cr. Carbon	5	1/8W	425
R308	18k	Cr. Carbon	5	1/8W	634
R309	3.3k	Cr. Carbon	5	1/8W	1638
R310	68k	Cr. Carbon	5	1/8W	1636
R311	3.3k	Cr. Carbon	5	1/8W	1638
R312	470Ω	Cr. Carbon	5	1/8W	1373
R313	1k	Cr. Carbon	5	1/8W	384
R314	220Ω	Cr. Carbon	5	1/8W	304
R315	100Ω	Cr. Carbon	5	1/8W	11504
R316	10k	Cr. Carbon	5	1/8W	11503
R317	100Ω	Cr. Carbon	5	1/8W	11504
R318	10k	Cr. Carbon	5	1/8W	11503
R319	2.7k	Cr. Carbon	5	½W	18555
R320	2.7k	Cr. Carbon	5	½W	18555
R321	2.2k	Cr. Carbon	5	1/8W	425
R322	2.2k	Cr. Carbon	5	1/8W	425
R323	1k	Cr. Carbon	5	1/8W	384
R324	33	RRC LG75	5		2277
R325	33	RRC LG75	5		2277
R326	330Ω	Cr. Carbon	5	1W	19037
R327	330Ω	Cr. Carbon	5	1W	19037
R328	470Ω	Cr. Carbon	5	1/8W	1373
R329	150Ω	Cr. Carbon	5	1/8W	301
R330	220Ω	Cr. Carbon	5	1/8W	304
R331	470Ω	Cr. Carbon	5	1/8W	1373
R332	47Ω	Cr. Carbon	5	1/8W	727
R333	47Ω	Cr. Carbon	5	1/8W	727
R334	47Ω	Cr. Carbon	5	1/8W	727
R335	47Ω	Cr. Carbon	5	1/8W	727
R336	100Ω	Electrosil TR8	1	1/8W	21870
R337	100Ω	Electrosil TR6	1		23507
R338	100Ω	Electrosil TR6	1		23507
R339	37.4Ω	Electrosil C5	1		26479
R340	150Ω	Electrosil TR6	1		26480
R341	150Ω	Electrosil TR6	1		26480
R342	120Ω	Electrosil C5	1		26481
R343	75Ω	Electrosil TR6	1		21866
R344	75Ω	Electrosil TR6	1		21866
R345	249Ω	Electrosil C5	1		26482
R346	61Ω	Electrosil TR6	1		21867
R347	61Ω	Electrosil TR6	1		21867
R348	47	Cr. Carbon	5	1/8W	727
R349	220Ω	Cont.Pot.Plessey MPD/PC			28522
R350	1k	Cont. Pot.			A4/30128
R351	220Ω	Cont.Pot.Plessey MPD/PC			28522
R352	1k	Cont. Pot.			A4/30128
R353		A.O.T.			
R354		A.O.T.			
CAPACITORS					
C301	10pF	G.P. Ceramic			22364
C302	10pF	G.P. Ceramic			22364
C303	33pF	G.P. Ceramic			22370
C304	33pF	G.P. Ceramic			22370
C305	0.1μF	Lemlac	+80 -20	30V	19647
C306	22pF	G.P. Ceramic			22364
C307	22pF	G.P. Ceramic			22368
C308	0.1μF	Lemlac	+80 -20	30V	19647
C309	0.1μF	Lemlac	+80 -20	30V	19647
C310	0.1μF	Lemlac	+80 -20	30V	19647
C311	.01μF	G.P. Ceramic			22395
C312	22pF	G.P. Ceramic			22368
C313	5.6pF	G.P. Ceramic			22361
C314	0.1μF	G.P. Ceramic			22395
C315	22pF	G.P. Ceramic			22368
C316	5.6pF	G.P. Ceramic			22361
C317	0.1μF	Lemlac	+80 -20	30V	19647
C318	0.1μF	Lemlac	+80 -20	30V	19647
C319	0.1μF	Lemlac	+80 -20	30V	19647
C320	0.1μF	Lemlac	+80 -20	30V	19647
C321	100μF	C437 AR/G100		40V	20779
C323	100μF	C437 AR/G100		40V	20779
C324	0.1μF	Lemlac	+80 -20	30V	19647
C325	0.1μF	Lemlac	+80 -20	30V	19647
C326	0.1μF	Lemlac	+80 -20	30V	19647
C327	0.1μF	Lemlac	+80 -20	30V	19647
C328	0.1μF	Lemlac	+80 -20	30V	19647
C329	0.1μF	Lemlac	+80 -20	30V	19647
C330	.01μF	G.P. Ceramic			22395
C331	0.1μF	Lemlac	+80 -20	30V	19647
C332	0.1μF	Lemlac	+80 -20	30V	19647

PG52 P3A (cont.)

Ref	*Value*	*Description*	*Tol%±*	*Part No*
TRANSISTORS				
VT301		2N 3906		21533
VT302		2N 3904		24146
VT303		2N 3904		24146
VT304		2N 3906		21533
VT305		2N 3904		24146
VT306		2N 3904		24146
VT307		2N 3906		21533
VT308		C424		21871
VT309		2N 4080		25862
VT310		BSX 28		25739
VT311		MT 3725		25863
VT312		MT 3726		25864
VT313		40250		4224
VT314		2N 2053		4039
VT315		MJ 3701		22624
VT316		MM 1614		19320
MR301		1N 916		1949
MR302		1N 916		1949
MR303		1N 916		1949
MR304		1N 916		1949
MR305		1N 916		1949
MR306		Zener ZF 3.9		3817
MR307		Zener SF12		4031
MR308		1N 916		1949
MR309		1N 916		1949
MR310		1N 916		1949
MR311		1N 916		1949
MR312		BAY 82		25865
SOCKETS				
SKA		BNC 50Ω		1222
SKB		BNC 50Ω		1222
SKC		BNC 50Ω		26587
SWITCHES				
S301-S303		Push Button		26572
S304-S308		Push Button		26571
L301		Ferroxcube FX1360		18828



NOTES –
1 S304 TO S307 ARE INTERLOCKED

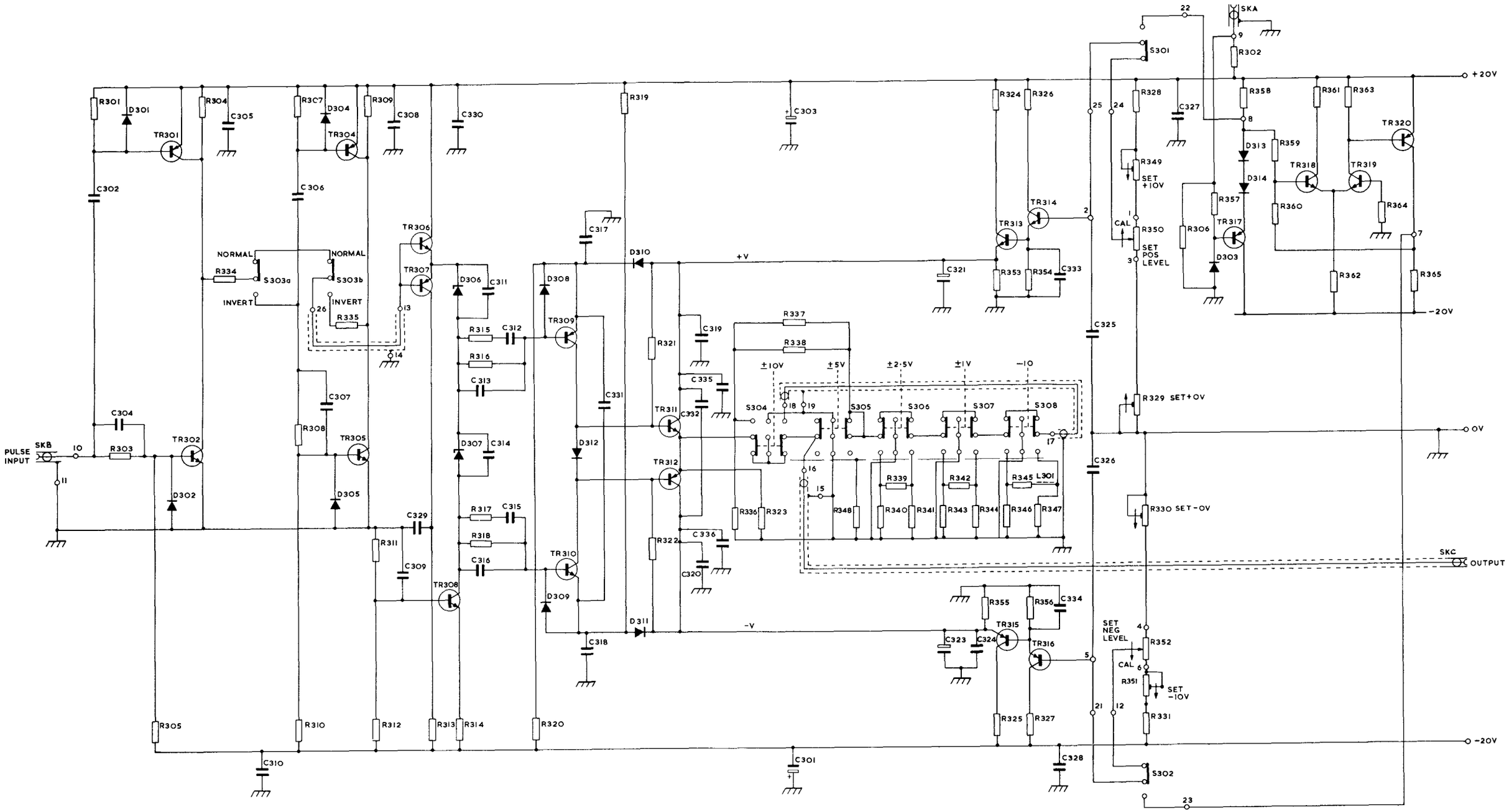
PG52 P3A STANDARD OUTPUT CIRCUIT DIAGRAM

PG52 P13

Ref	Value	Description	Tol%±		Part No.
RESISTORS					
R301	1k		5	1/8W	384
R302	39k		5	1/8W	1639
R303	4k7		5	1/8W	386
R304	3k3		5	1/8W	1638
R305	15k		5	1/8W	315
R306	12k		5	1/8W	1685
R307	2k2		5	1/8W	425
R308	18k		5	1/8W	634
R309	3k3		5	1/8W	1638
R310	68k		5	1/8W	1636
R311	3k3		5	1/8W	1638
R312	470Ω		5	1/8W	1373
R313	1k		5	1/8W	384
R314	220Ω		5	1/8W	304
R315	100Ω		5	1/8W	11504
R316	10k		5	1/8W	11503
R317	100Ω		5	1/8W	11504
R318	10k		5	1/8W	11503
R319	2k7		5	½W	18555
R320	2k7		5	½W	18555
R321	2k2		5	1/8W	425
R322	2k2		5	1/8W	425
R323	1k		5	1/8W	384
B324	33Ω		5	6W	2277
R325	33Ω		5	6W	2277
R326	330Ω		5	1W	19037
R327	330Ω		5	1W	19037
R328	470Ω		5	1/8W	1373
R329	220Ω	Plessey MPD/PC			28522
R330	220Ω	Plessey MPD/PC			28522
R331	470Ω		5	1/8W	1373
R332		Not fitted			
R333		Not fitted			
R334	47Ω		5	1/8W	727
R335	47Ω		5	1/8W	727
R336	100Ω		1		21870
R337	100Ω		1		23570
R338	100Ω		1		23570
R339	37Ω5		1		29108
R340	150Ω		1		29109
R341	150Ω		1		29109
R342	120Ω		1		29110
R343	75Ω		1		29111
R344	75Ω		1		29111
R345	247Ω5		1		29112
R346	61Ω		1		29113
R347	61Ω		1		29113
R348	47Ω		1	1/8W	727
R349	220Ω	Plessey MPD/PC			28522
R350	1k	Pot. Control			A4/30128
R351	220Ω	Plessey MPD/PC			28522
R352	1k	Pot. Control			A4/30128
R353	1k5		5	1/8W	385
R354	1k5		5	1/8W	385
R355	1k5		5	1/8W	385
R356	1k5		5	1/8W	385
R357	3k3		5	1/8W	1638
R358	1k5		5	1/8W	385
R359	10k		5	1/8W	11503
R360	10k		5	1/8W	11503
R361	2k2		5	1/8W	425
R362	4k7		5	1/8W	386
R363	2k2		5	1/8W	425
R364	4k7		5	1/8W	386
R365	1k		5	1/8W	384
CAPACITORS					
C301	100μF			40V	20779
C302	10pF				22364
C303	100μF			40V	20779
C304	22pF				22368
C305	01μF			30V	19647
C306	10pF				22364
C307	22pF				22368
C308	.01μF			30V	19647
C309	.01μF			30V	19647
C310	.01μF			30V	19647
C311	.01μF				22395
C312	22pF				22368
C313	5pF6				22361
C314	.01μF				22395
C315	22pF				22368
C316	5pF6				22361
C317	.01μF			30V	19647
C318	.01μF			30V	19647
C319	.01μF			30V	19647
C320	.01μF			30V	19647
C321	1μF			160V	2364
C322		Not fitted			
C323	1μF			160V	2364
C324	.01μF			30V	19647
C325	.01μF			30V	19647
C326	.01μF			30V	19647
C327	.01μF			30V	19647
C328	.01μF			30V	19647
C329	.01μF			30V	19647
C330	.01μF				22395
C331	.01μF			30V	19647
C332	.01μF			30V	19647
C333	.1μF			160V	2740
C334	.1μF			160V	2740
C335	.1μF			160V	2740
C336	.1μF			160V	2740
TRANSISTORS					
TR301		2N 3906			21533
TR302		2N 3904			24146
TR303		Not fitted			
TR304		2N 3906			21533
TR305		2N 3904			24146
TR306		2N 3904			24146
TR307		2N 3906			21533
TR308		C424			21871

PG52 P13 (cont.)

Ref	*Value*	*Description*	*Tol%±*	*Part No.*
TR309		2N 4080		25862
TR310		BSX 28		25739
TR311		MM 3725		25863
TR312		MM 3726		25864
TR313		40250		4224
TR314		2N 3053		4039
TR315		MJ 3701		22624
TR316		MM 1614		19320
TR317		MM 1614		19320
TR318		2N 930		21548
TR319		2N 930		21548
TR320		MM 1614		19320
DIODES				
D301		1N 916		1949
D302		1N 916		1949
D303		1N 916		1949
D304		1N 916		1949
D305		1N 916		1949
D306		Zener	3V9	3817
D307		Zener	12V	4031
D308		1N 916		1949
D309		1N 916		1949
D310		1N 916		1949
D311		1N 916		1949
D312		BAY 82		25865
D313		1N 916		1949
D314		1N 916		1949
MISCELLANEOUS				
L301		Ferrite FX1306		18828
S301-S303				26572
S304-S308				26574
PLA				26459
SKA				1222
SKB				1222
SKC				26587



PG52 P13 MODULATED OUTPUT CIRCUIT DIAGRAM

Supplement for

PG52 P6

Modular Plug-In

ADVANCE
INSTRUMENTS (Sales Office)

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Contents

Introduction

Section 1

This PG52. P6 output module for the PG52 system provides a positive or negative output of up to 50V into 50Ω. It has an unlimited duty cycle giving a maximum output power capability of 50W. It has a dual input facility to allow the generation of output pulses from independent sources and an invert facility which can overcome any duty cycle limitation of these inputs. It contains its own integral power supply driven directly from the a.c. supply via the main frame.

This handbook supplement should be used in conjunction with the handbook for the PG52 main frame and system, Part Number 30163.

Specification

Section 2

The PG52 P6 output module is a double width 4" unit operating in a PG52, PG52A or PG52B main frame.

INPUT

Two BNC input sockets operating in an 'OR' function to +5 volt input signals.

Required input rise time	10nS or less
Maximum input voltage	+ −20V peak
Input resistance	> 3kΩ

Normally intended to be driven from standard PG52 system interface signals.

Maximum input frequency	3MHz
Minimum input pulse width	100nS

OUTPUT

Positive or negative with respect to ground, variable 10 volts to 50 volts into 50Ω.

Accuracy	± 5% at 50 volts
Duty Cycle	unlimited (50W maximum)
Rise and fall times	<15nS. (typically <10nS)
Pertubation	< ±8% of pulse height (Typically <5% at 50 volts).
Output impedance	approximately 5Ω.
Power Consumption	approximately 70W.
Weight	8¼lbs (3.8kgm).

TERMINATION TP21

50Ω, 50W through resistance.

Size:	5½" x 3½" x 7½" (14cm x 9cm x 19cm)
Weight:	1½lbs (0.7kgm).

3.1 PREPARATION FOR USE

Before inserting the module into any main frame, ensure that the supply input selector, which is visible through the top cover of the module, is set correctly. Unless specifically ordered for 100/130V operation, the module is despatched from the factory set for 200/260V operation.

To change the input supply selector, remove the top cover of the plug-in. The supply slider switch is then accessible. Remove the switch locking plate by unscrewing the two fixing screws, slide the selector switch over and then turn the plate through 180°. Secure the two fixing screws and replace the top cover.

When a P6 module is first used in a PG52 or PG52A main frame the auxiliary AC supply connection must be completed within the frame. Line and Neutral should be linked from TB2 on the right side-member, to the second and fourth pins from the bottom of the right hand module socket, SK8 (see circuit diagram of PG52 and PG52A in the main frame handbook). The subsequent links to SK7, SK6 and SK5 are included in manufacture, but for safety, the AC supply is only connected to the modules when it is needed. It is always connected on the PG52B.

FUSES

Check the rating of FS601 (the fuse on the back panel of the module) and the rating of the auxiliary fuse/fuses to be as shown below.

The module will only operate in the right hand half of the main frame where the internal cooling is adequate.

Preferably it should be inserted in the extreme right hand position but it may be used with one or two single width modules to its right.

3.2 VENTILATION

The module requires effective forced air cooling within the main frame. It is important that the input and output areas on the rear and right side of the frame are not restricted. The frame must be operated with a full complement of modules or blank panels to ensure correct air circulation. To minimise power dissipation, otherwise unused modules can be inserted upside down in the frame when they will not be connected to the internal supplies. When using the module under full power into the TP21ŋ do not restrict the ventilation of the termination.

Before use in a PG52 main frame (or in a PG52A frame before serial No. 306) the blank right hand side cover should be changed for a perforated cover Pt. No.27944. In the absence of the correct cover the instrument can be used without any side cover fitted.

3.3 INPUT

The inputs to the module should normally be the +10V PG52 interface levels. Alternatively, other input voltages greater than +5V with rise and fall times less than 10nS can be used. The maximum input voltage is ±20V pk. The input resistance is approx 3KΩ.

The two input sockets operate in an 'OR' configuration to positive input signals to allow double pulse operation from two independent pulse inputs.

It should be noted that the output level is determined by transitions of the input signals rather than the DC level, and after switch on, the state of the output is not determined until the first input transistion is received.

Main frame, type.	Input Supply Voltage Range.	PG52P6 (FS601)	Main frame Aux. fuse/fuses. (FS4 & FS6)
PG52 and PG52A	100–130	2A size 'O' Slow Blow Pt. No. 20439,	5A Size 'O' Pt. No. 12807.
	200–260	1A size 'O' Slow Blow Pt. No. 21619	5A Size 'O' Pt. No. 12807
PG52B	100–130	2A size 'O' Slow Blow Pt. No. 20439	4A size 'OO' Pt. No. 5120
	200–260	1A size 'O' Slow Blow Pt. No. 21619	4A size 'OO' Pt. No. 5120

3.4 OUTPUT

WARNING

THE UNIT IS CAPABLE OF DELIVERING AN OUTPUT POWER OF 50W AND MAY ONLY BE CONNECTED INTO LOADS WITH A POWER DISSIPATION LIMIT BELOW THIS IF CARE IS TAKEN TO RESTRICT THE INPUT DUTY CYCLE THUS LIMITING THE MEAN OUTPUT POWER.

With the positive (+) button only pressed, a positive input signal will drive the output, into 50Ω, from ground to a positive level between 10 and 50 volts as determined by the OUTPUT LEVEL control on the front panel. With the negative (–) button only pressed, the output will be from ground to the same negative level.

Operation of the INV button will cause the output to switch from the selected +ve, or –ve, level to ground for the duration of a positive input pulse. This facility overcomes any maximum mark/space ratio limitation of the input signal and .allows the output duty cycle to approach 100%.

The output is specified to operate into a non-reactive 50 load and the specified pulse shape will only be achieved when connected to such a load via a 50Ω coaxial connector such as the PL43.

The output is protected against operation into short circuit, capacitive loads or any loads less than 50Ω. IT MUST NOT BE OPERATED INTO INDUCTIVE LOADS.

The output is designed to operate up to 50V into 50 i.e. to deliver 1A. There is additional range on the level control to give an e.m.f. of 60V. The control should not be set above the 50V position when driving into 50Ω or the current overload circuitry may operate. However this over-range can be used into a high impedance as described in section 3.6.

3.5 PROTECTION

The internal power supply has a re-entrant maximum current characteristic such that it will supply a mean current of 1A at 50V output, 0.5A at 25V output etc. Thus, if any load less than 50Ω is connected, the power supply voltage will collapse until that load is removed.

Further protection is provided to detect any transient change of output current greater than 1A. Such a transient will cause the drive signals to be inhibited and the 50V power supply to collapse for a period of approx. 2mS. The power supply will subsequently be re-established and if the overload has been removed the unit will function normally. If not, the trip cycle will be repeated.

The maximum operating rate is 3MHz. To avoid exceeding this rate, and thus causing damage, an automatic protection circuit prevents the acceptance of a second positive going input transition within 330nS of the first positive going transition, or of a negative transition within 330nS of a previous negative transition. This causes a count down of input frequencies above 3MHz and inhibits the generation of consecutive pulses with leading or trailing edges separated by less than 330nS.

As this can give a change of output duty cycle, particular care should be taken when operating with closely spaced pulses operating into loads less than 50W rating although the input duty cycle is low.

3.6 TERMINATION

To achieve the specified rise time and overshoot, the unit must be operated into a 50Ω load and connected via a 50Ω coaxial cable such as the PL43. If it is to be run at 100% duty cycle this load must be capable of dissipating 50W. Incorrect termination may cause considerable overshoot and ringing on the pulse at the load due to reflections in the cable. The TP21 is provided as a 50Ω 50W load. It has a 50Ω through resistance between input and output. When operated with the shorting cap on its output it provides a correct termination for the cable and an output can be taken via a "T" adaptor on the input into a high impedance load (>>50Ω). Alternatively without the shorting cap fitted, 1 amp pulses can be taken from the output of the load into low impedance loads (>>50Ω).

It should be noted that the 20 or 30 pF input capacitance of a conventional real time oscilloscope can introduce distortion to the waveform when it is connected to the input of the TP21 to monitor the signal. It is preferable to use a low input capacitance probe such as the Tektronix P6035 connected directly onto the input to the load with a suitable adaptor.

If some overshoot and ringing can be tolerated when driving a high impedance load, the TP21 can be connected directly onto the output of the module as a 50Ω through load (series resistor) to provide back termination of the subsequent cable. In this way it is possible to use the over-range capability of the level control and achieve a 60V pulse into a high impedance.

The circuit of the P6 unit can be divided into the blocks shown in Fig. 1. Also shown are the waveforms expected at the various points. The module consists of an input stage which is driven from the same supplies (referred to ground) as the complete PG52 system. Transformer coupled signals are taken from this stage into a slave bistable which, via driver and amplification circuitry, feeds the output stage.

The module contains its own floating internal power supplies. The output polarity change is achieved by grounding one side or other of the output supply. The output is driven between the positive and negative of this supply, giving a positive output voltage when the negative side of the supply is grounded and negative when the positive side is grounded. The output pulse amplitude control varies the output power supply voltage from 10V to 50V.

The circuit will be described in three sections, these are:

(1) the input circuitry and slave bistable.

(2) the drive and output circuitry

(3) the power supply and protection circuitry

4.1 THE INPUT AND SLAVE BISTABLE CIRCUITS

This part of the circuit is driven from the general PG52 system interface level (+10V) which is referred to ground and the +20 and −20 volt lines. The input sockets are coupled to the bases of transistors, TR601 and TR602. Diodes, D601 to D604, protect these transistors against excessive input excursions. These transistors are connected as a parallel gate and form one half of an emitter-coupled long-tailed network with transistor, TR603.

The differential output from the circuit is coupled by C604 and C605 into the primary windings of transformers T602 and T603. The secondary voltages are sharp differentiated spikes (due to the time constant of the transformer and associated coupling capacitor) and feed via the polarity and inversion switches, S603 and S602 respectively, into the slave bistable. Thus each transition of the input voltage switches the bistable to follow the input signal either directly or inverted. The bistable circuitry is referred to the OV (the positive side of the 50V output supply) while the input signals are referred to ground (the OV and chassis of the system).

This bistable circuit is controlled by the pulses received through diodes D606 and D609 from the input stage. The set and reset state being determined by the polarity and inversion selection switches.

The circuit comprises transistors TR610 and TR614, as a cross-coupled bistable with additional speed-up provided by ac coupling the collector voltages into transistors, TR612 and TR613. These act as 'pull-up' switches on the collectors of TR610 and TR614 respectively.

The output from the bistable is coupled through R636 to the buffer and driver stages.

4.2 BUFFER AND DRIVER CIRCUITS

The 0 to +12V pulse generated by the slave bistable passes through the complementary emitter follower pair, TR615 and TR616, into the complementary switches TR617 and TR618. Diodes, D618, 619 and 623 bias the emitters of this pair so that only one of the pair is turned on at any time. This stage provides speed-up to the pulse in both its positive and negative going transitions to drive the complementary emitter follower stage, TR619 and TR620.

The low impedance pulse output from this stage is level shifted by the zener diode D624 to give a signal of approximately ±5 volts, about OV., to drive into the output switching circuits. TR623 supplies a constant current through D624, independant of the 10 to 50V change in the output supply with the level control.

This pulse will turn transistor TR621 on or off as a saturated switching stage with its collector current supplied by the constant current source TR624. Thus its collector voltage swing is from OV (in its 'on' state) toward −62V (in its 'off' state), until it is caught, at −50V by diode D636. Transistor TR622 is a.c. coupled from this same drive pulse and turns on only during the positive-going transitions of the pulse. This action speeds up the negative-going transition of the collector potential of TR621 as it turns off. The amplitude of the pulse at the collectors of transistors TR621 and TR622 is approximately five volts greater than the output level as set by the front panel control R612 i.e. a maximum level of some 62 volts. In fact, the range of control of the 50V output supply is from 12V to 61V.

Diode D645 will limit any excess base current in TR621 once its collector has reached saturation level. This prevents excessive propagation delay on narrow widths. The output from the switching circuit is taken via resistor R686 to the output circuit. This resistor with capacitor C641 is selected to limit overshoot on the output waveshape.

The output circuit is formed by the complementary emitter followers, TR625 and TR626, and six transistors, TR627 to TR632. The latter are connected as three parallel complementary emitter-follower pairs, with current sharing resitors in each emitter.

The resultant low impedance output which follows the waveform generated on the collector of TR627 is taken to the output socket, SKC.

Diodes, D643 and D644, clip transient reflections in mismatched output cables.

4.3 OUTPUT POLARITY AND INVERT SWITCHING

The polarity of the output pulse, either from ground positive or from ground negative is determined by S604 which grounds the negative or positive side of the 50V output supply, accordingly. This part of the polarity switch is mechanically linked to the front panel polarity switch, S602. S602a and S602b determine the phase of the output pulse in relation to the input pulse and provide the necessary inversion with polarity. Similarly the INVERT switch, S603, also reverses the connection between the coupling transformers and slave bistable.

4.4 POWER SUPPLY CIRCUITRY

Apart from the input circuitry which operates fromt he +20V and −20V supplies of the main frame, the module operates from a number of self generated, stabilised supply lines.

These are:−

a) The output supply (variable between 10V and 50V) the positive side of which is referred to as the 0V line and the negative as the −50V line. There is also a −51V line, approx. 1V more negative than the −50V line.

b) The +12 and −5V lines which are with respect to 0V, the positive side of the variable output supply.

c) The −62V line which is always −12V with respect to −50V, the negative side of the variable output supply.

These are all derived from a supply transformer, T601, fed from the input supply via the AUX. fuse in the main frame and picked up on the rear connector, PLA. The line connection has a fuse FS601, before the input supply range selector switch, S601, on the transformer primary.

The transformer has three independent secondaries and these are rectified by full wave bridges, MR601 to MR603, and smoothed by capacitors, C644, C645 and C646, to give d.c. voltages of approximately 20 volts, 80 volts and 20 volts, respectively.

The output from bridge, MR601, feeds via FS602 to a stabiliser circuit for the +12 volts and −5 volts lines.

The +12V line is obtained by driving zener diode, D629, from the current source transistor, TR633. This zener potential (approx. 13V) provides the base voltage for the compound emitter follower arrangement of TR635 and TR634. The output from the emitter of TR634 is then stabilised at approximately +12 volts above the '0V' line. Most of the return current from this line and D629 flows through the zener, D630, giving a further −5 volt line, from the 0V line. These two lines are used to feed both the slave bistable and subsequent buffer circuitry in the signal path and to feed the stabiliser circuit for the 50V stabiliser.

The 80V output from MR602 is taken via FS603 to the stabiliser circuit of the 50 volt stabilised line. D642 is the reference zener diode for the −50 volt supply. The resistor chain, R660, 616, 612, 663 and 662, acts as a potential divider between this reference and the −50V line. The potential of the junction of R619 and R612 is compared with 0V by the long tailed pair, TR641 and TR642. Any difference is amplified by TR642 the output potential transferred by the emitter follower, TR606, to control the series regulator, TR636. Thus if the −50V line is too far negative, the base potential of TR641 is negative.

Current is diverted from TR641 to TR642 and the collector potential of TR642 goes further negative. This change is transferred through TR606 to reduce the conduction through TR636. The increase in collector-emitter voltage of TR636 shifts the whole of the unstabilised supply across C645 more positive with respect to 0V hence sending the −50V line more positive, correcting the original error.

With the base of TR641 stabilised at 0V, there is a constant current of 10mA from D642 through R660 and R619. This current continues through R612, R663 and R662 and the output voltage is defined by the sum of these resistors. R612 is the OUTPUT LEVEL control and is used to vary the output supply and hence the output pulse amplitude over the range 10 to 50V. R660 adjusts the current in the divider chain setting the pulse output to 50V at the calibrated point near the maximum end of the control range of R612. The output voltage at the minimum end of the control range is set to 10V by adjustment of R662.

The actual total range of control of the 50V output supply is from approx. 12 volts to approx. 61V which allowing for losses of voltage through the various components in the output stage provides the over range capability of 60V e.m.f. There is an approximate 1V difference in output stage loss between positive and negative outputs and this is overcome by the introduction of R620 into the potential divider of the stabiliser circuit in the positive output mode only.

The control loop will respond rapidly to an increase of load current as TR636 turns on. The cascaded emitter follower pair, TR607 and TR637, complement TR606 and TR636 and conduct only to prevent any transient increase output voltage when the load current is reduced.

The stabilised −50V line potential is used to define the voltage swing at the collector of TR612. The return current from this line is passed through D647 to generate a line approx. 1V more negative, −51V. The collectors of TR628, 630 and 632, the output stage, are returned to this line and the additional negative bias avoids zero or forward bias of their collector base junctions.

4.5 PROTECTION CIRCUITS

Three forms of protection circuitry are built into the circuit to prevent damage to the power supply or output transistors due to excessive input frequency or output loading. These are:—

a) A mean current limit in the 50V stabiliser circuit.
b) A peak current trip on the output line.
c) An output frequency limiter.

The mean current limit is an integral part of the 50V stabiliser circuit. The emitter current of the series regulator transistor, TR636, flows through the current detector resistor, R652. As this current increases, the potential at the junction of D632 and R650 rises. When this overcomes the negative bias introduced by R651 and R655, TR638 conducts. The collector potential of TR638 drops and the emitter follower, TR639, transfers this change to over-ride the stabilising output of TR642 and to reduce the stabilised supply voltage. R655 with preset R654, is returned to the stabilised voltage and the bias it introduces to the base of TR638, decreases as the line voltage decreases. Thus the current limit is reduced as the supply is reduced, giving a re-entrant characteristic to the stabiliser. The circuit will supply approx. 1A at 50V but only a little more than 0.5A at 25V. The power supply output will then collapse if a load of less than 50Ω is applied.

Once an overload is removed the time constant of C648 with R656 and R657, limits the rate of recovery of the supply voltage.

The response times of the stabiliser as a whole and the current overload circuit in particular, are much slower than the switching time of the output stage. The decoupling capacitors, C643, C653, C654, C650 and C642, absorb the fast transients of the necessarily rapid load current.

Because of the relatively slow response of the mean current detection circuitry, further fast protection is is necessary to prevent excessive current from damaging the output stage when the output is short circuited or driven into a low impedance load. A 1A trip circuit is fitted which must operate even when the output is being driven with narrow pulses at a low repetition rate and the mean current is too low to operate the protection circuit described above.

The output cable passes through a ferrite core on the output socket forming a single turn primary winding of a current transformer, T604.A current transition in excess of 1A in the output will induce an e.m.f. in the centre tapped secondary winding sufficient to overcome the bias set by preset, R641; causing D616 or D617 to conduct into the base of TR609. This transistor with TR608, forms a monostable with a period of approx. 2mS. Thus any excess output current is detected rapidly to send the collector of TR608 positive for 2mS. turning on both TR611 and TR638 via R630 and R617 respectively. The effect of TR611 through S603c, is to lock the slave bistable and prevent the output stage from turning off while carrying a heavy current. The effect of turning on TR638, is to simulate a heavy overload current in the mean current detector and cause the stabilised output supply to collapse rapidly.

At the end of approx. 2mS, the clamp on the bistable is removed and after a period of approx., 8mS, determined by C648, the power supply potential will increase slowly. If the overload is still present on the output socket, the trip cycle will repeat.

The third protection circuit is to prevent damage to the output stage which would occur if it is driven faster than 3MHz. TR604 and TR605 form a monostable circuit with a period of approx. 330nS and a fast recovery. Each negative transistion of the collector of TR610 in the slave bistable initiates the monostable via C608. The collector of TR604 goes positive, turning on TR643 for 330nS and clamping the secondary drive to D606. Thus during this period TR610 can be turned off but not be turned on again. The slave bistable is then prohibited from responding to closely spaced pulse pairs or to input frequencies greater than 3MHz. It will follow such inputs in a count-down mode.

5.1. FUSES

Within the P6 unit are three fuses. The normal supply input fuse, FS601, is a size '0' 1 Amp slow-blow type (Pt. No.21619) for operation on 200-260V supplies. For operation from 100-130V this should be a 2 Amp slow-blow type (Pt, No.20439). This fuse is mounted on the rear panel of the module and is readily accessible. Mounted internally on the rectifier printed circuit board assembly are the fuses for the 50 volt and 12 volt lines. These are 1 Amp '00' size, (Pt. No.1254) and 250 mAmp '00' size, (Pt. No.19815) respectively. To gain access to these two fuses it is only necessary to remove the right hand side cover.

5.2 ACCESS

Full access to all sub assemblies is obtained on removing the side covers and the top and bottom trays. Fig 2 shows the location of components with these covers off. Improved access to the back of the stabiliser and driver boards is obtained if the stabiliser board is detached from the frame. It can be moved outward without disconnecting any of the wiring.

The module can be operated out of the main frame on a suitable extension lead. The necessary plug and socket are from the ITT ISEP range

plug type 12 - 212 - 110 Advance Part no.26459.

socket type 13 - 302 - 201 Advance Part no.25301.

Care should be taken because these connections carry the AC supply voltage.

5.3 FAULT LOCATION

Faults can generally be localised to a particular area of the circuitry by examining the power supplies and then the switching waveforms at various points along the signal path from input to output as shown in the block diagram, Fig. 1. The circuit diagram, Fig. 3, gives full details including pin numbers where a connection is taken from one printed circuit board to another.

Until it is necessary to check for operation in the positive mode, it is recommended that the module is switched to negative output when the positive or OV side of the 50V output supply, is connected to ground. The drive waveforms do not then shift in d.c. level with respect to ground as the output level control is varied.

Before checking waveforms in detail the power supplies should be checked.

These are

a) +20V and −20V from main frame, used only on the input board.

b) a.c. supply from the main frame via fuse, FS601, and the supply selector switch, S601, to transformer, T601.

c) +12V and −5V with respect to OV, from the stabiliser board and used on the input and driver boards.

d) −50V variable approx. 12V to 60V with respect to OV by the output level control, from the stabiliser board to the driver board.

e) −51V, follows −50V with additional −1V bias, from the rectifier board to the output board via the driver board.

f) −62V which is −12V with respect to −50V line, from stabiliser board to driver board.

These lines should be checked initially without input drive or output loading. If the −50V line is at approx. −10V and cannot be varied by the output level control, there may be a fault in the output or driver boards rather than the stabiliser. The −51V and −50V lines should be disconnected from these boards before examining the stabiliser further.

The ripple on the +12V line should be at 100Hz and less than 1mV pk/pk.

The ripple on the −50V line when the −51V line is loaded with 1A, should be at 100Hz and less than 10mV pk/pk. The line should change less than 2V from no load to 1A on the −51V line and less than ±0.5V at full load for ±10% variation of ac supply. When the output circuit is operating at 50V into 50Ω, the transient level change on the 50V line should be less than 0.5V at each load current transition, normally damped oscillation of 1½ cycles with a period of 20μS. C649 is fitted if necessary and its value selected on factory test to prevent oscillation on this line.

With the power supplies operating satisfactorily, an input signal at approx. 1kHz should be applied and an oscilloscope used to follow it through various stages as shown in the block diagram, Fig.1, which also shows the expected waveforms and levels. It should first operate

unloaded at this low frequency. The load should then be applied and the positive output mode tried. If satisfactory with output levels up to 50V, the frequency can be increased and the output waveshape examined in detail. The various preset controls should be set according to the sequence in section 5.4.

A low frequency oscilloscope can be used to check the general operation of the module if a high impedance probe is used to monitor switching waveforms and the output cable is terminated with the TP21 as close as possible to the oscilloscope.

However it should be noted that the 20 to 30pF input capacitance of an oscilloscope, can cause distortion due to reflections in the interconnecting cable. Detailed measurements of pulse shape should be made with a wide bandwidth probe directly on the termination via a 'T' connector or preferably via 50Ω coaxial attenuators into a sampling oscilloscope. For the latter, the duty cycle of the output waveform should be restricted to limit the power into the attenuators. (i.e. a 1:50 maximum mark space at 50V output for the normal 1W attenuator pad).

5.4 CALIBRATION

1) Set R641 and R654 fully counter clockwise. Set R660 and R662 to mid position. Select negative invert and monitor the output voltage unloaded with a dc multi-meter. Switch on and apply a single input pulse from a P1 module (use manual operation). This should set the output to its "on" state.

Set the Output level control to maximum, fully clockwise. Adjust R660 for an output of 60V.

2) Set the Output Level control to minimum (fully anticlockwise). Load the output with 50Ω and adjust R662 ro 10V output.

Repeat adjustment of R660 and R662 if necessary until unloaded output voltage is 60V at maximum and loaded voltage is 10V at minimum.

3) Set Output level control to give 50V output into 50Ω and set the position of the knob on the shaft to the 50V scale mark.

4) Set the input waveform to an approximate square wave at 10Hz. Set the Output Level to maximum and monitor with an oscilloscope the output waveform into a load of 50Ω in parallel with an additional 500Ω. (i.e. load current is 1.1A). Set R654 to the point where droop on the output voltage first appears (i.e. the mean current detector operates).

5) Set the input waveform to an approximate square wave at 100kHz. Set the Output Level to the 50V mark.

Monitor the output waveform into 50Ω and increase R641 until the current trip is seen to operate and then reduce its setting until the waveform just returns to normal. Check that this setting gives correct operation on positive and negative outputs, normal and invert mode and with variations of pulse width.

The value of R614 is selected on factory tests to set the period of the frequency limit monostable to inhibit input frequencies above 3MHz. This will only need to be changed if associated components are also changed.

Similarly R677, C638, R686 and C641 are selected to optimise the output waveform. R677 and C638 affect the shape of the positive going and negative going edges respectively. R686 and C641 prevent excessive overshoot. These will only need to be changed if associated drive or output components are changed.

R620 is selected to equalise the output amplitude at 50V into 50Ω between positive and negative output modes.

RESISTORS

Ref	Value	Description	Tol ± %	Rating	Part No.
R600	220		5	1/8W	3832
R601	3k3		5	1/8W	1638
R602	33k		5	1/8W	317
R603	3k3		5	1/8W	1638
R604	33k		5	1/8W	317
R605	180Ω		5	1/8W	1517
R606	680		5	1/8W	18548
R607	180		5	1/8W	1517
R608	820		5	1/8W	18549
R609	1k		5	1/8W	384
R610	820		5	1/8W	1637
R611	3k3		5	1/8W	1638
R612	5k6	Pot. Control			A4/30130
R613	1k		5	1/8W	384
R614	15k		5	1/8W	315
R615	10		5	1/8W	2259
R616	10k		5	1/8W	11503
R617	1.2k		5	1/8W	2087
R618	1k		5	1/8W	384
R619	330		5	1/8W	1894
R620	100		5	1/8W	11504
R621		A.O.T.	5	1/8W	
R622	33k		5	1/8W	317
R623	18k		5	1/8W	634
R624	1k2		5	1/8W	2087
R625	470		5	1/8W	1373
R626	470		5	1/8W	1373
R627	18k		5	1/8W	634
R628	33k		5	1/8W	317
R629	12k		5	1/8W	2087
R630	10k		5	1/8W	11503
R631	680		5	1/8W	309
R632	3Ω3	Type LX	10	1/10W	28613
R633	2k7		5	1/8W	311
R634	22k		5	1/8W	1544
R635	1k2		5	1/8W	2087
R636	120		5	1/8W	735
R637	3.3k		5	1/8W	1638
R638	3.3k		5	1/8W	1638
R639	82		5	1/8W	730
R640	82		5	1/8W	730
R641	470	Plessey MPD/PC			28524
R642	150		5	1/8W	301
R643	15k			6W	921
R644	4k7		5	1/2W	18558
R645	4k7		5	1/2W	18558
R646	390		5	1/8W	2410
R647	4k7		5	1/8W	386
R648	180		5	1/8W	2210
R649	1k		5	1/8W	384
R650	2k2		5	1/8W	425
R651	47k		5	1/8W	318
R652	2Ω2			6W	19790
R653	47			6W	31907
R654	10k	Plessey MPD/PC			28525
R655	56k		5	1/8W	756
R656	1M		5	1/8W	766
R657	2M2		10	1/8W	24838
R658	270	A,O,T,	5	1/8W	2716
R659	390		5	1/8W	2410
R660	470	Plessey MPD/PC			28524
R661	100		5	1/2W	18538
R662	470	Plessey MPD/PC			28524
R663	820		5	1/8W	1637
R664	1k		5	1/8W	384
R665	1k		.5	1/8W	384
R666	220		5	1W	19035
R667	3k3		5	1/8W	1638
R668	1k		5	1/8W	384
R669	100		5	1/8W	11504
R670	10k		5	1/8W	11503
R671	100		5	1/8W	11504
R672	5k6		5	1/8W	787
R673	4k7		5	1/8W	386
R674	1k		5	1/8W	384
R675	1k		5	1/8W	384
R676	4k7		5	1/8W	386
R677	68		5	1/8W	1640
R678	3k3		5	1/8W	1638
R679	47	A.O.T.	5	1/8W	727
R680	10		5	1/8W	2259
R681	560		5	1/8W	308
R682	1k		5	1/8W	384
R683	470		5	1/8W	1373
R684	1k		5	1/8W	384
R685	560		5	1/8W	308
R686	100	A.O.T.	5	1/8W	11504
R687	10		5	1/8W	2259
R688	1k		5	1/8W	384
R689	10		2		28771
R690	10		2		28771
R691	10		2		28771
R692	10		5	1/8W	2259
R693	10k		5	1/8W	11503
R694	10		2		28771
R695	10		2		28771
R696	10		2		28771
R697	470		5	1/8W	1373
R698	220		5	1/8W	304

CAPACITORS

Ref	*Value*	*Description*	*Tol ± %*	*Rating*	*Part No.*
C601	10pF				22364
C602	.1μF			30V	19647
C603	10pF				22364
C604	120pF				22377
C605	120pF				22377
C606	.1μF			30V	19647
C607	.1μF			30V	19647
C608	10pF				22364
C609	33pF				22370
C610	.1μF			30V	19647
C611	22pF				22368
C612	.1μF			160V	2740
C613	.47μF			160V	2429
C614	15pF				22366
C615	15pF				22366
C616	15pF				22366
C617	15pF				22366
C618	10pF				22364
C619	5μF			64V	20773
C620	22pF				22368
C621	.1μF			30V	19647
C622	22pF			64V	21514
C623	.1μF			30V	19647
C624	120pF				22377
C625	120pF				22377
C626	5pF6				22361
C627	68pF				22374
C628	68pF				22374
C629	5pF6				22361
C630	.1μF			30V	19647
C631	.1μF			30V	19647
C632	.1μF			30V	19647
C633	.1μF			30V	19647
C634	.22μF			160V	2601
C635	470pF				22383
C636	33pF				22370
C637	470pF				22383
C638	56pF	A.O.T.			22373
C639	.1μF			30V	19647
C640	.1μF			30V	19647
C641					
C642	.1μF			160V	2740
C643	2.2μF			64V	25738
C644	1000μF			40V	2742
C645	2240μF			100V	28270
C646	1000μF			40V	2742
C647	100μF			40V	20779
C648	.1μF			160V	2740
C650	.1μF			160V	2740
C651	.1μF			30V	19647
C652	.1μF			30V	19647
C653	1μF			160V	2364
C654	.1μF			160V	2740
C655	.01μF				22395
C656	6pF8				22362
C657	1μF			160V	2364
C658	.01μF				22395
C659	.01μF				22395
C660	.01μF				22395

TRANSISTORS

TR601	BSX20	23307
TR602	BSX20	23307
TR603	BSX20	23307
TR604	BSX20	23307
TR605	MPS 3640	24128
TR606	2N 3053	4039
TR607	2N 4037	21882
TR608	BSX20	23307
TR609	BSX20	23307
TR610	BSX20	23307
TR611	BSX20	23307
TR612	BSX29	25740
TR613	BSX29	25740
TR614	BSX20	23307
TR615	BSX20	23307
TR616	2N 3906	21533
TR617	BSX29	25740
TR618	BSX28	25739
TR619	BSX20	23307
TR620	2N 3906	21533
TR621	2N 4031	30047
TR622	2N 4047	30048
TR623	SFT187	24916
TR624	SFT187	24916
TR625	2N 4047	30048
TR626	2N 4031	30047
TR627	2N 4047	30048
TR628	2N 4031	30047
TR629	2N 4047	30048
TR630	2N 4031	30047
TR631	2N 4047	30048
TR632	2N 4031	30047
TR633	2N 3096	21533
TR634	2N 3053	4039
TR635	2N 3904	24146
TR636	SDT 9202	24385
TR637	2N 4920	30049
TR638	BC 108	26110
TR639	2N 3096	21533
TR640	2N 3053	4039

Ref	Value	Description	Tol ± %	Rating	Part No
TR641) TR642)		SL 301A Dual			30256
TR643		BSX20			23307
TR644		BSX20			23307
D601		1N 916			1949
D602		1N 916			1949
D603		1N 916			1949
D604		1N 916			1949
D605		1N 916			1949
D606		1N 916			1949
D607		1N 916			1949
D608		1N 916			1949
D609		1N 916			1949
D610		1N 916			1949
D611		1N 916			1949
D612		1N 916			1949
D613		1N 916			1949
D614		ZENER		3V3	4034
D615		1N 916			1949
D616		1N 916			1949
D617		1N 916			1949
D618		1N 4003			23462
D619		1N 4003			23462
D620		1N 916			1949
D621		1N 916			1949
D622		1N 916			1949
D623		1N 4003			23462
D624		ZENER		6V8	4666
D625		1N 916			1949
D626		1N 916			1949
D627		ZENER		5V6	4109
D628		ZENER		2V7	21002
D629		ZENER		13V	19540
D630		ZENER Z3B56CF			20978
D631		ZENER Z3B30CF			28266
D632		1N 4003			23462
D633		1N 916			1949
D634		1N 914			23802
D635		1N 914			23802
D636		1N 916			1949
D637		1N 914			23802
D638		1N 916			1949
D639		1N 914			23802
D640		ZENER		3V3	4034
D641		1N 4003			23462
D642		ZENER		5V6	4109
D643		1N 901			1949
D644		1N 916			1949
D645		1N 916			1949
D646		1N 916			1949
D647		1N 4003			23462
D648		1N 4003			23462
D649		1N 916			1949
D650		1N 916			1949
MR601		WO2			19725
MR602		WO2			19725
MR603		WO2			19725
T601		Transformer, Supply			C35153
T602		Transformer, Pulse			A.28274
T603		Transformer, Pulse			A.28274
T604		Transformer, Pulse			A.28276
SKA					1222
SKB					1222
SKC					26587
PLA		1 SBP 11 Way			26459
S601					A4/30045
S602/3					A4/30060
S604					30061
FS601		SLO-BLO 200-260V		1A	21619
		100-130V		2A	20439
FS602				250mA	19815
FS603				1A	1254

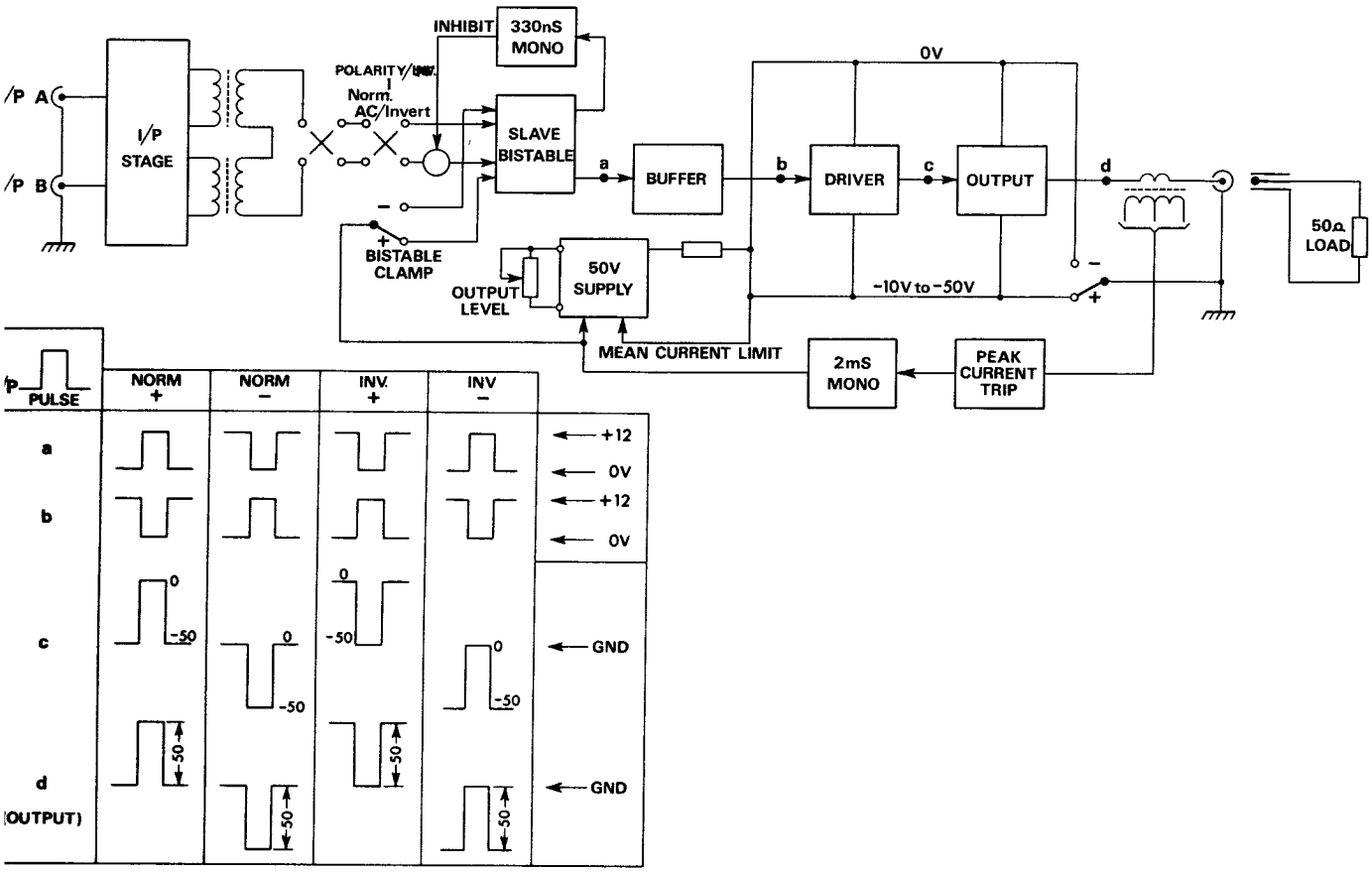


Fig. 1 Block Diagram & Waveforms

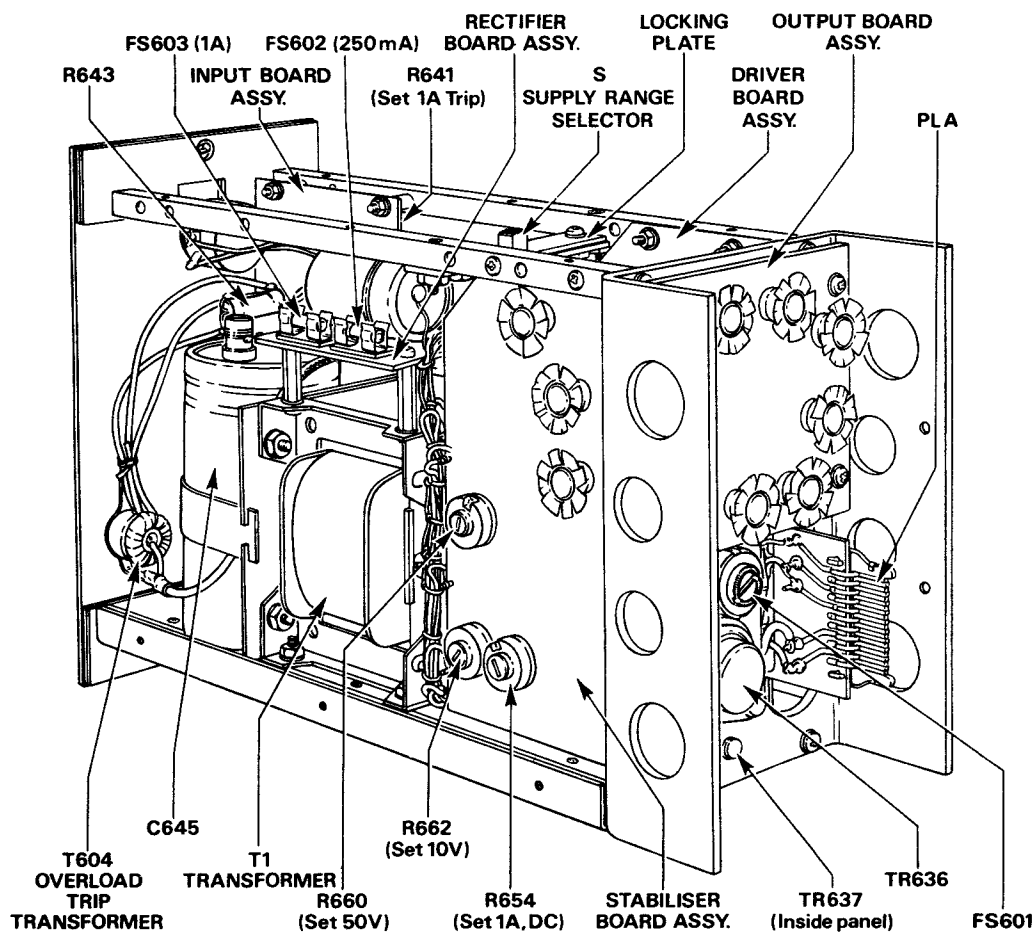


Fig. 2 Component Layout

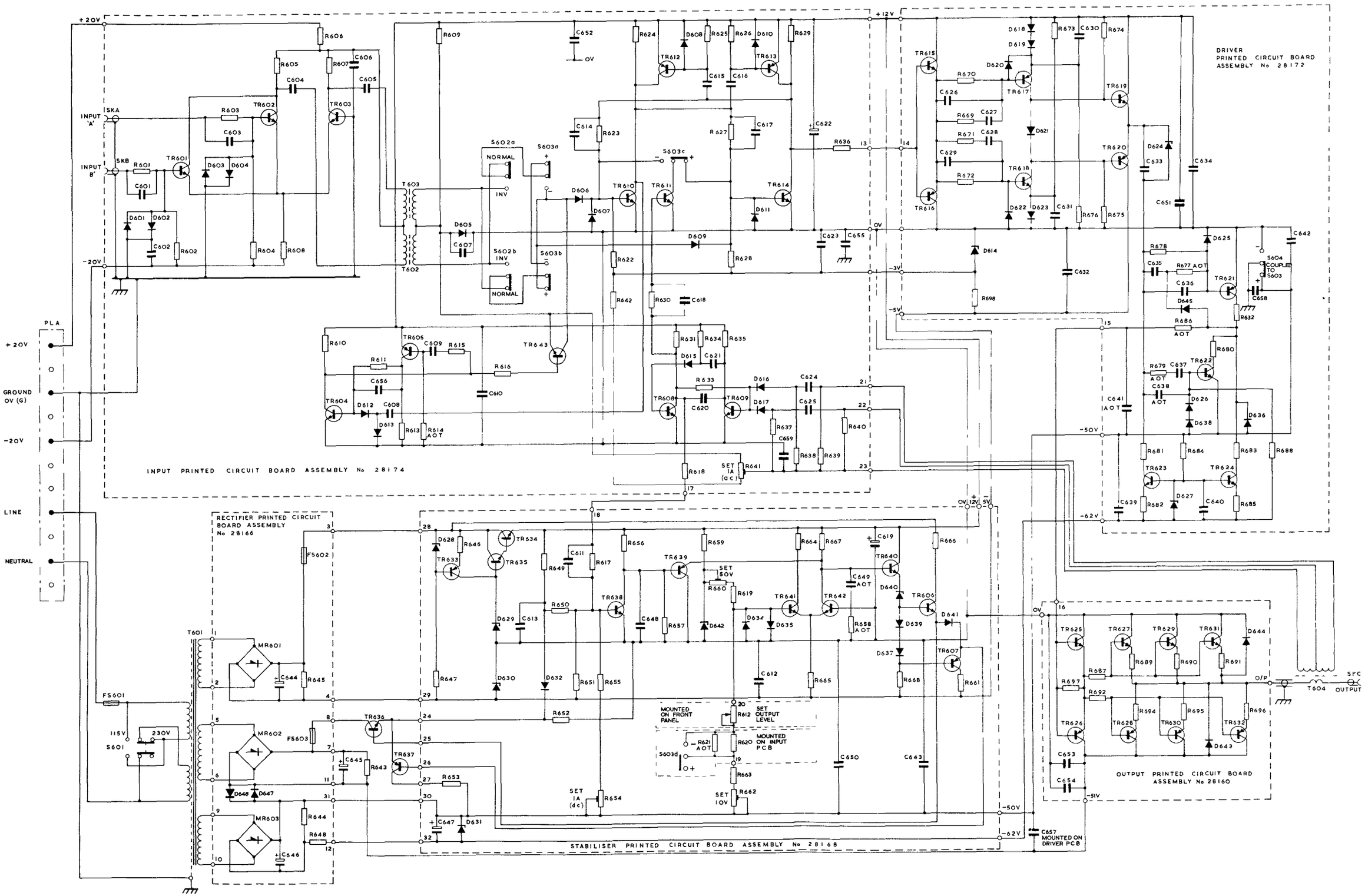


Fig. 3 Circuit Diagram

Supplement for
PG52P2, PG52P2A and PG52P12
Pulse Width or Delay and
Modulated Width or Delay Modules

ADVANCE
INSTRUMENTS (Sales Dept.)

Raynham Road Bishop's Stortford Herts England
Telephone 0279 55155
Telegrams Advancelec
Telex 81510

Division of ADVANCE ELECTRONICS LIMITED

Contents

Introduction

Section 1

These variable pulse width generator modules are used within the PG52 system to determine the width of output pulses or the delay between one event and another. They cover the range 25nS to 1 sec. and while they are mainly intended to be driven from other modules in the system, the input trigger level can be adjusted to allow them to trigger as required from a variety of waveforms from other signal sources.

The PG52P2A differs from the PG52P2 only in having a rotary fine control in place of edge-operated controls. The PG52P12 is similar to the PG52P2A but in addition has the facility for control of the output width over the selected 10:1 range by means of an externally applied voltage. The information in this supplement applies to all three modules except where specifically stated.

This handbook supplement should be read in conjunction with the main frame and system handbook, Pt. No. 30163.

Specification

Section 2

Single width, 2" modules operating in a PG52, PG52A or PG52B main frame.

2.1 PG52 and PG52A

RANGE

25nS to 1 sec. in switched decade ranges with uncalibrated intermediate control.
Accuracy ±5% at decade points up to 5MHz.

DUTY CYCLE

Up to 70% below 10MHz
50% above 10MHz

INPUT

An output pulse is initiated by the negative going transition of the input signal level through the trigger level.

Trig. level range	+5V to −5V
Sensitivity	2·5V pk.pk. below 10MHz
	5V pk.pk. above 10MHz
Max. input voltage	±20V pk.
Max. input frequency	25MHz
Max.source impedance	600Ω

OUTPUT

Two parallel output sockets provide the standard system interface signal of +10V.
A test point is provided.

2.2 PG52P12

As PG52P2A, with the additional facility of external modulation; an approximate swing of 0 to +10V input voltage being equivalent to a 10:1 reduction of width, available on any selected decade range.

Input resistance	>10K
Max.input voltage	±20V pk.

The following description covers the detailed function and control of the modules while the typical use of the module within the system is covered in the handbook for the main frame and system.

3.1 TRIGGER INPUT

The module is triggered by a negative-going transition of the input level through the trigger level. It is normally intended to be driven from a standard +10V system interface signal, in which case the TRIGGER LEVEL control should be set at its +5V or NORMAL position. For optimum operation above 10MHz it may be necessary to reduce this setting. The unit will not trigger reliably at frequencies above 25MHz.

The input can however, be driven from any other source and the trigger level adjusted between +5V and −5V by the control, to suit a wide range of waveforms (e.g. low frequency sine waves, ramp voltages etc.) where the trigger level control can be used to select the point at which the period is initiated. Alternatively, this control can be used to avoid spurious triggering with noisy input waveforms.

The sensitivity of the trigger circuit about the trigger level is approx. 2.5V pk.pk. for input frequencies below 10MHz, rising to approx. 5V pk.pk. above 10MHz.

The input resistance is greater than 3K and the input circuitry is protected against voltages up to +20V or −20V pk.

The trigger level control is mounted on the front panel of the PG52P2 and PG52P2A modules. On the PG52P12 it is a preset control, mounted on the printed circuit board but with easy access for screwdriver adjustment through the bottom of the left side cover.

It should be noted that the PG52P10 module has a more sensitive input and more versatile facilities when it is required to trigger the system from external signals.

3.2 PERIOD SETTING

Select the period units required (1 sec. mS, μS or 100nS on the left hand bank of push button switches).

On the mS and μS ranges, select the required multiplying factors (X1, X10 or X100) on the right hand bank of push buttons. These push buttons have no effect on the 1 sec. and 100nS ranges.

With the fine control in the CAL position, the period will be as selected. Operation of the fine control away from the CAL position will reduce the period over at least a decade range (to 25nS on the 100nS range). The P2 module has two controls with a coarse and fine action.

3.3 DUTY CYCLE LIMITATIONS

For normal operation, the pulse width should not exceed 70% of the repetition period. For repetition frequencies above 10MHz, the width should not exceed 50% of the repetition period. However, such limitations can be overcome by the use of the INVERT function on the Output modules.

The unit can also be used to count-down the input frequency if the pulse width is set to be an approximate multiple of the repetition period up to a factor of 10. Careful adjustment of the fine period control will give a stable count-down. Particular applications of this count-down mode of operation are described in section 3:6:12 of the main frame and system handbook.

3.4 OUTPUT

The standard system interface output signal is provided through two paralleled output sockets, i.e. an approximate 0 to +10V waveform from a low source impedance (less than 100Ω). It is intended to drive the inputs of other modules but it can alternatively feed any other load of impedance >500Ω.

Beyond this, the output current is limited and the waveform may be seriously distorted. The module is protected against short circuits but should not be run continuously in this condition.

The output is also fed through a 5·6K resistor to a front panel test point. This is intended to allow a C.R.O. to examine the output waveform while the module is connected in a system.

3.5 PROPAGATION DELAY

When initiated with a fast input singal, the leading edge of the output pulse will occur after a typical delay of 20nS.

3.6 MODULATION (P12 only)

Until the MOD button is operated, the PG52P12 module operates as described above. When the button is operated, the fine control becomes inoperative and its function in controlling the output pulse width over the selected 10:1 range (4:1 on 100nS range), is replaced by a voltage in the range 0 to +10V applied to the modulation input socket. This is an uncalibrated function but with the input voltage at 0V, the width will be between the nominal maximum for the range selected and +20% of that nominal. With the input voltage at +10V, the width will be $^1/_{10}$ of the nominal or less. The maximum input voltage is ±20V pk.

These modules operate from the +20V supplies from the main frame. Circuit references in brackets in the following description, apply to the P12 where different from the P2 or P2A.

4.1 VARIABLE LEVEL TRIGGER CIRCUIT

This is composed of the long-tailed pair, VT201 and VT202 (TR201 and TR202), driven from the current source, VT203 (TR203). The input signal is applied to the base of VT201 as a directly coupled input while the base potential of VT202 is set by the trigger level control potentiometer, R246. Positive feedback from the collector of VT201 is applied through R207 and C204 to the base of VT202, to give a trigger action as the input passes through the trigger level.

The output from the comparator is taken from the collector of VT202 (TR202) to drive VT204 (TR204). This stage produces a 10 volt step which is differentiated by C208 to give a very narrow spike. This spike is used to trigger the variable period monostable circuit.

4.2 VARIABLE PERIOD MONOSTABLE CIRCUIT

The circuit consists of a long-tailed input pair, VT205 and VT206 (TR205 and TR206) with a capacitive feedback path from the collector of VT205 (TR205) to the base of VT206 (TR206). The appropriate timing capacitor (C212 to C221 inclusive) is coupled through the double emitter follower, VT207 and VT208 (TR207), and selected by S201 to S208. The charging current is fed to the capacitor from VT209 (TR209) which is controlled by the variable period control, R245. The base potential of VT209 is slightly modified by operation of R250, the Fine Period control. The latter applies to the PG52P2 only.

The circuit is triggered from the positive spike produced by the variable trigger level circuit. This edge is fed to the base of VT205 (TR205).

Transistor, VT205 (TR205), is normally in conduction and a positive-going trigger edge from VT204 is coupled via C208 to turn it off. The resultant negative step on the collector of VT205 (TR205) is transferred through the selected timing capacitor to the base of VT206 (TR206). This transistor turns on, keeping VT205 (TR205) off. Diode, MR204 (D204), is reverse biased and the timing capacitor charges at a rate determined by the current source, VT209 (TR209). The current is variable over a ten to one range, the actual value being set by R245 (the fine period control). The base of VT209 is switched by S201 – 208 to one of the preset calibration potentiometers R240 – 244.

As the timing capacitor charges, the base potential of VT206 (TR206) rises until the point where VT206 (TR206) is cut off. This will turn on VT205 (TR205) with the feedback path again speeding the action. The timing capacitor is rapidly discharged through MR204 (D204) ready for the next trigger pulse.

4.3 THE SWITCHING DETAIL

The range of width is selected by S201 – 208. As the width is increased, larger values of capacity are switched in cumulatively, i.e. in many cases the capacitor for one range is in parallel with those for smaller ranges. The following table shows which capacitors are switched in for any given range.

RANGE	SELECTED CAPACTORS
100nS	C212, C213 (AOT)
1μS	C212, C213 214 & C215 (AOT)
10μS	C212 to C216
100μS	C212 to C217
1mS	C212 to C215 & C218
10mS	C212 to C216, C218 & C219
100mS	C212 to C220
1 Sec.	C212 to C217 & C221

The preset control potentiometers, R240 – R244, set the maximum width on the 100μS to 1Sec ranges respectively. The trimmer, C212, sets the maximum width on the 100nS range while the capacitors; C214 with C215, C216 and C217; are matched to within ±2% so that adjustment of R240 on the 100μS range will bring the 'μS' ranges within specification.

4.4 THE OUTPUT STAGE

The output of the monostable is directly coupled through VT211 (TR211) to the output emitter follower, VT212 and VT213 (TR212 and TR213). Transistor, VT210 (TR210), is a.c. coupled to the drive and turns on only for a short period to speed up the turn-off edge of VT211 (TR211).

The output emitter followers provide a low output impedance but are protected against damage from accidental short circuiting of the output, by R234 and R237 (R238) and the series resistors, R235 and R236. Zener diode, MR209 (D209), and the emitter follower, VT214 (TR214), produce a +11 volt line to drive the input and output circuits and bias the monostable.

4.5 MODULATION CIRCUIT (P12 only)

Operation of the MOD switch, S208, transfers the emitter of TR209 from the set period control, R245, to the collector of TR215 and the current in the latter then controls the period of the monostable circuit.

As the potential applied to the input socket is increased from 0V, the current in TR216 is increased. Its collector potential, the base potential of TR215, drops and the collector current of TR215 increases; reducing the period of the monostable. The transfer characteristic of the circuit is modified by the diode network, D210, D211 and D212, with their associated resistors, R256 to R262 inclusive, resulting in an approximately linear change of width with applied voltage.

The modular construction of the instrument allows fault location by substitution. Any module suspected of being at fault can be replaced by another module to confirm the suspected fault to be within one module. Full or partial failure of all modules is probably due to a fault in the common power supply or its distribution in the main frame. The fuses should be checked and also the potentials on the +20V and −20V lines. A fault within one module, taking excessive current from one of the lines, can overload the line and degrade the performance of the other modules.

When a fault is localised within the power supply or any one module, the faulty part can be returned to the factory for repair or further investigation can be carried out with the help of the relevant circuit diagram and circuit description. Component replacement in any module may require it to be recalibrated.

The circuitry of the module is all solid-state and as such should require no regular maintenance. Stiff action of the push button switches can be overcome by the sparing use of a switch lubricant.

5.1 ACCESS

Access to the circuitry of each module is easily obtained by removing the two covers. Any module can be operated out of the main frame on a suitable extension lead. The necessary plug and sockets are from the STC 1SEP range,

plug type 12–212–110	Advance Pt.No.26459
socket type 13–302–201	Advance Pt.No.25301

5.2 FAULT LOCATION AND CALIBRATION

Faults within this module can be localised to the input trigger circuit, the monostable or the output circuit by investigation of the output of each section in turn. Correct operation on some period ranges but not on others indicates a fault in the range switching or in the timing capacitors.

Recalibration may be necessary after changing components. It should be carried out in the sequence given below after checking that the incoming +20V and −20V supply lines are correct within 200mV. The trigger level control should be set to '+5 NORMAL' and the module driven from a Clock Generator, P1, module at a frequency to give an output duty cycle less than 50%.

1) Select the 100μS range. With the fine period control at 'CAL', adjust the preset R240, for correct output width.
2) Set the fine period control to minimum end of its travel. (Output pulse width to be less than 10μS). Reset the fine period control to CAL .
3) Select the 100nS range and adjust the trimmer capacitor for the correct output width.
4) Select the 1μS range. The factory selected capacitor, C215, should be changed if the output pulse is not within specification.
5) Select the 10μS range. The output pulse width should be to specification. C216, the capacitor for this range is matched to C217, the capacitor for the 100μS range. R240, previously set at step 1, may need fine adjustment to obtain the best compromise setting for this 10μS range and the 100μS range.
6) Select the 1mS range. Adjust the preset, R241, for output pulse width to specification.
7) Select the 10mS range. Adjust the preset, R242, for output pulse width to specification.
8) Select the 100mS range. Adjust the preset, R243, for output pulse width to specification.
9) Select the 1 sec. range. Adjust the preset, R244, for output pulse width to specification.

If at any step in the above procedure there is insufficient control available on the preset potentiometer, the factory selected resistor, R224, may need to be changed. The full calibration procedure must then be repeated.

PG52 P2A PULSE WIDTH & DELAY

Ref	Value	Description	Tol%±		Part No.
RESISTORS					
R201	3.3k	Cr. Carbon	5	1/8W	1638
R202	10k	Cr. Carbon	5	1/8W	11503
R203	10k	Cr. Carbon	5	1/8W	11503
R204	1.2k	Cr. Carbon	5	1/8W	2087
R205	330Ω	Cr. Carbon	5	1/8W	1894
R206	220Ω	Cr. Carbon	5	1/8W	304
R207	1k	Cr. Carbon	5	1/8W	384
R208	5.8k	Cr. Carbon	5	1/8W	787
R209	56Ω	Cr. Carbon	5	1/8W	2411
R210	220Ω	Cr. Carbon	5	1/8W	304
R211	10k	Cr. Carbon	5	1/8W	11503
R212	1k	Cr. Carbon	5	1/8W	384
R213	6.8k	Cr. Carbon	5	1/8W	313
R214	4.7k	Cr. Carbon	5	1/8W	386
R215	56Ω	Cr. Carbon	5	1/8W	2411
R216	390Ω	Cr. Carbon	5	1/8W	2410
R217	4.7k	Cr. Carbon	5	1/8W	386
R218	390Ω	Cr. Carbon	5	1/8W	2410
R219	10Ω	Cr. Carbon	5	1/8W	2259
R220	150Ω	Cr. Carbon	5	1/8W	301
R221	390Ω	Cr. Carbon	5	1/8W	2410
R222	470Ω	Cr. Carbon	5	1/8W	1373
R223	1k	Cr. Carbon	5	1/8W	384
R224	47Ω	Cr. Carbon	5	1/8W	727
R225	10k	Cr. Carbon	5	1/8W	11503
R226	100Ω	Cr. Carbon	5	1/8W	11504
R227	4.7k	Cr. Carbon	5	1/8W	386
R228	82Ω	Cr. Carbon	5	1/8W	730
R229	100k	Cr. Carbon	5	1/8W	319
R230	820Ω	Cr. Carbon	5	1/8W	1637
R231	1.8k	Cr. Carbon	5	1/8W	310
R232	220Ω	Cr. Carbon	5	1/8W	304
R233	1k	RRC 5SCD4	5		17758
R234	100Ω	RWV4-J	5		1240
R235	47	RRC 5SCD4	5		4038
R236	47	RRC 5SCD4	5		4038
R237	680	Cr. Carbon	5	1/8W	309
R238	470	Cr. Carbon	5	1W	19039
R239	5.6k	Cr. Carbon	5	1/8W	787
R240	1k	Cont.Pot.Plessey MPD/PC			26870
R241	1k	Cont.Pot.Plessey MPD/PC			26870
R242	1k	Cont.Pot.Plessey MPD/PC			26870
R243	1k	Cont.Pot.Plessey MPD/PC			26870
R244	1k	Cont.Pot.Plessey MPD/PC			26870
R245	4.7k	Cont.Pot.			A4/30127
R246	4.7k	Cont.Pot.Plessey W.M.P.			24560
R247	10k	Cr. Carbon	5	1/8W	11503
CAPACITORS					
C201	10pF	G.P. Ceramic			22364
C202	0.1μF	Lemlac	+80 -20	30V	19647
C203	0.1μF	Lemlac	+80 -20	30V	19647
C204	100pF	G.P. Ceramic			22376
C205	0.1μF	Lemlac	+80 -20	30V	19647
C206	0.1μF	Lemlac	+80 -20	30V	19647
C207	100pF	G.P. Ceramic			22376
C208	18pF	G.P. Ceramic			22367
C209	0.1μF	Lemlac	+80 -20	30V	19647
C210	0.1μF	Lemlac	+80 -20	30V	19647
C211	0.1μF	Lemlac	+80 -20	30V	19647
C212	60pF	Trimmer Mullard CO10 AA/60A			1866
C213	30pF	Lemco A.O.T.			
C214	200pF	Lemco 115E Insul.			18331
C215	39pF	Lemco A.O.T.			
C216	2400pF	Selected	1		25730
C217	.022μF	Selected	1		25732
C218	.02μF	Selected			25734
C219	2.2μF	Filmcap TE1	5		25738
C220	22μF	Kemet K22J15K	10	15V	19260
C221	220μF	Kemet K220J10K	10	10V	19259
C222	22pF	G.P. Ceramic			22368
C223	22pF	G.P. Ceramic			22368
C224	680pF	G.P. Ceramic			22385
C225	0.1μF	Lemlac	+80 -20	30V	19647
C226	0.1μF	Lemlac	+80 -20	30V	19647
C227	100pF	C437 AR/G100		40V	20779
C228	0.1μF	Lemlac	+80 -20	30V	19647
C229	100μF	C437 AR/G100		40V	20779
C230	0.1μF	Lemlac	+80 -20	30V	19647
C231	0.1μF	Lemlac	+80 -20	30V	19647
C232	0.1μF	Lemlac	+80 -20	30V	19647

PG52 P2A PULSE WIDTH & DELAY (cont.)

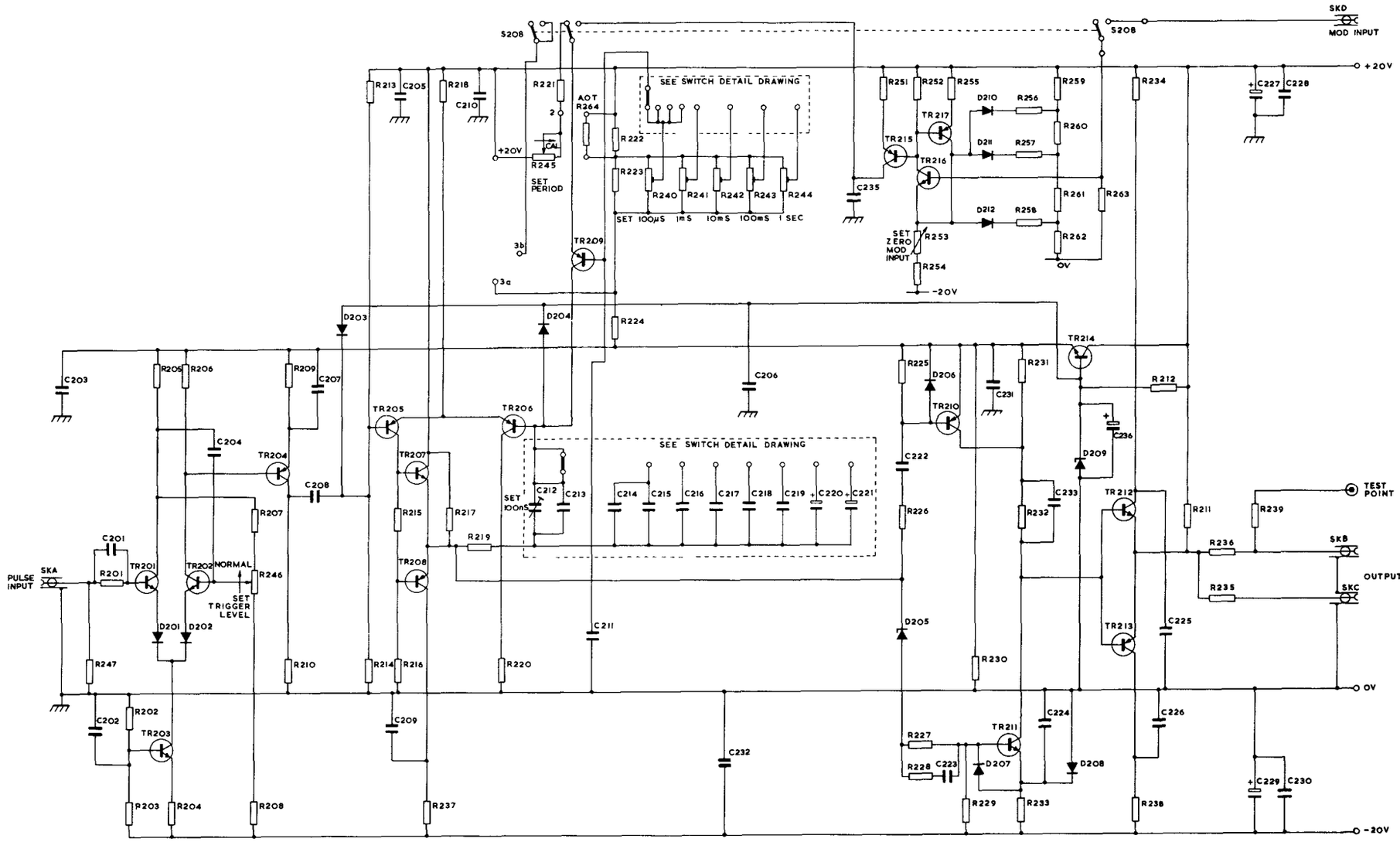
Ref	Value	Description	Part No.
TRANSISTORS			
VT201		BSX 20	23307
VT202		BSX 20	23307
VT203		BSX 20	23307
VT204		BSX 29	25740
VT205		BSX 29	25740
VT206		BSX 29	25740
VT207		MM 1613	19323
VT208		2N 3905	20818
VT209		2N 3702	19840
VT210		2N 3906	21533
VT211		BSX 28	25739
VT212		2N 3904	24146
VT213		2N 3906	21533
VT214		2N 3053	4039
DIODES			
MR201		1N 916	1949
MR202		1N 916	1949
MR203		1N 916	1949
MR204		1N 916	1949
MR205		Zener 2.7V	21002
MR206		1N 916	1949
MR207		1N 916	1949
MR208		1N 916	1949
MR209		Zener 12V	4031
MISCELLANEOUS			
S201-S204			26463
S205-S207			26462
SKA		BNC 50Ω	1222
SKB		BNC 50Ω	1222
SKC		BNC 50Ω	1222

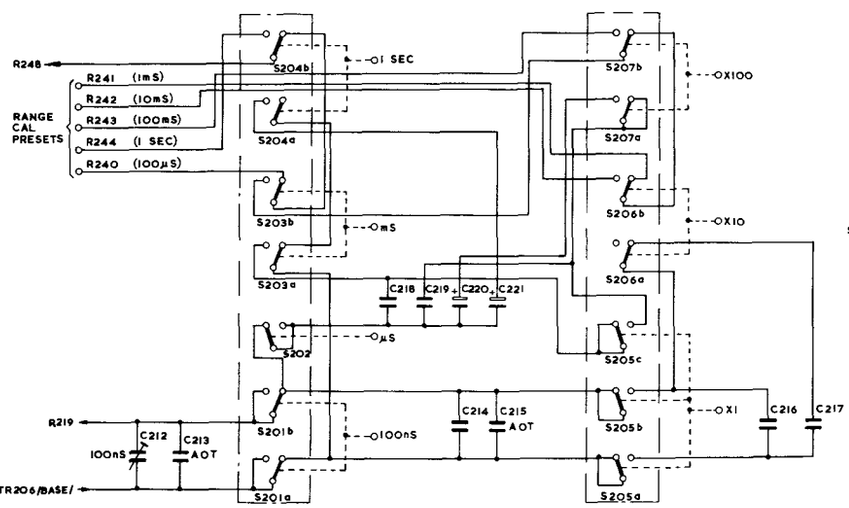
PG52 P12

Ref	Value	Description	Tol%±		Part No.
RESISTORS					
R201	3.3k		5	1/8W	1638
R202	10k		5	1/8W	11503
R203	10k		5	1/8W	11503
R204	1.2k		5	1/8W	2087
R205	330Ω		5	1/8W	1894
R206	220Ω		5	1/8W	304
R207	1k		5	1/8W	384
R208	5.6k		5	1/8W	787
R209	56Ω		5	1/8W	2411
R210	220Ω		5	1/8W	304
R211	10k		5	1/8W	11503
R212	1k		5	1/8W	384
R213	6.8k		5	1/8W	313
R214	4.7k		5	1/8W	386
R215	56Ω		5	1/8W	2411
R216	390Ω		5	1/8W	2410
R217	4.7k		5	1/8W	386
R218	390Ω		5	1/8W	2410
R219	10Ω		5	1/8W	2259
R220	100Ω		5	1/8W	11504
R221	390Ω		5	1/8W	2410
R222	470Ω		5	1/8W	1373
R223	1k		5	1/8W	384
R224	47Ω		5	1/8W	727
R225	10k		5	1/8W	11503
R226	100Ω		5	1/8W	11504
R227	4.7k		5	1/8W	386
R228	82Ω		5	1/8W	730
R229	100k		5	1/8W	319
R230	820Ω		5	1/8W	1637
R231	1.8k		5	1/8W	310
R232	220Ω		5	1/8W	304
R233	1k		5		17758
R234	100Ω		5		1240
R235	47Ω		5	1/8W	4038
R236	47Ω		5	1/8W	4038
R237	680Ω		5	1/8W	309
R238	470Ω		5	1W	19039
R239	5.6k		5	1/8W	787
R240	1k	Plessey MPD/PC			26870
R241	1k	Plessey MPD/PC			26870
R242	1k	Plessey MPD/PC			26870
R243	1k	Plessey MPD/PC			26870
R244	1k	Plessey MPD/PC			26870
R245	4.7k	Control Pot.			A4/30127
R246	4.7k	Plessey WMP			27923
R247	10k		5	1/8W	11503
R248		Not fitted			
R249		Not fitted			
R250		Not fitted			
R251	270Ω		5	1/8W	2716
R252	1.5k		5	1/8W	385
R253	15k	Plessey MPD/PC			28526
R254	22k		5	1/8W	1544
R255	3.3k		5	1/8W	1638
R256	560Ω		5	1/8W	308
R257	10k		5	1/8W	11503
R258	22k		5	1/8W	1544
R259	1.5k		5	1/8W	385
R260	330Ω		5	1/8W	1894
R261	270Ω		5	1/8W	2716
R262	10Ω		5	1/8W	2259
R263	15k		5	1/8W	315
CAPACITORS					
C201	10pF				22364
C202	.1μF			30V	19647
C203	.1μF			30V	19647
C204	100pF				22376
C205	.1μF			30V	19647
C206	.1μF			30V	19647
C207	100pF				22376
C208	18pF				22367
C209	.1μF			30V	19647
C210	.1μF			30V	19647
C211	.1μF			30V	19647
C212	60pF	Trimmer			1866
C213		A.O.T.			
C214	200pF		1		18331
C215		A.O.T.			
C216	2200pF		1	400V	25730
C217	.022μF		1	160V	25732
C218	.24μF		5	125V	25734
C219	2.2μF		5		25738
C220	22μF		10	15V	19260
C221	220μF		10	10V	19259
C222	22pF				22368
C223	22pF				22368
C224	680pF				22385
C225	.1μF			30V	19647
C226	.1μF			30V	19647
C227	100μF			40V	20779
C228	.1μF			30V	19647
C229	100μF			40V	20779
C230	.1μF			30V	19647
C231	.1μF			30V	19647
C232	.1μF			30V	19647
C233	56pF				22373
C234					
C235	1000pF				22387
C236	22μF		10	15V	19260
TRANSISTOR					
TR201		2N 3227			28634
TR202		BSX 20			23307
TR203		BSX 20			23307
TR204		BSX 29			25740
TR205		BSX 29			25740
TR206		BSX 29			25740

PG52 P12 (cont.)

Ref	*Value*	*Description*	*Part No.*
TR207		MM 1613	19323
TR208		2N 3905	20818
TR209		2N 3702	19840
TR210		2N 3906	21533
TR211		BSX 28	25739
TR212		2N 3904	24146
TR213		2N 3906	21533
TR214		2N 3053	4039
TR215		MM 1614	19320
TR216		2N 930	21548
TR217		MM 1614	19320
DIODES			
D201		1N 916	1949
D202		1N 916	1949
D203		1N 916	1949
D204		1N 916	1949
D205		Zener	2.7V 21002
D206		1N 916	1949
D207		1N 916	1949
D208		1N 916	1949
D209		Zener	12V 4031
D210		1N 916	1949
D211		1N 916	1949
D212		1N 916	1949
MISCELLANEOUS			
S201-S204			26463
S205-S208			29224
SKA			1222
SKB			1222
SKC			1222
SKD			1222
PLA			26459





SWITCH DETAIL

S201 TO S204 ARE INTERLOCKED AS UNITS BANK
S205 TO S207 ARE INTERLOCKED AS MULTIPLYING FACTOR BANK
SWITCHES DRAWN FOR µS x 1

PG52 P12 CIRCUIT DIAGRAM