

Proposed Specification for additional circuit to be added to Eurotext CF70206.

In order to overcome a problem with the synchronisation from some VCRs, it is proposed to add the equivalent to the circuitry shown in Figure 1 to the design for the Eurotext CF70206.

The device resulting from this change will be known as the **CF70207**, with a device ID to be decided (it can either be the same as the CF70206, or a new unique device ID). The internal software for the CF70207 will be the same as the CF70206.

The output obtained from the additional circuit will appear on what used to be the "MUTE" pin (pin 13) on the CF70206. This output (BADL23) will be a logic 0 for a good sync and a logic 1 for a bad sync.

The proposed pin out for the CF70207 is shown in Figure 3.

Circuit Description

The circuit in figure 1 is intended to detect the situation when the Eurotext phase locked loop causes a phase error with respect to bad VCR syncs before line23. Waveforms for the circuit are shown on the page following Fig 1.

The first d-type flip flop is clocked on the falling edge of the WIND signal, and thus the Q output will be set to a 1. Shortly after this, the sliced sync from the VCR should occur, clearing the Dtype, and setting the Q output to a 0. When the L23WIND signal occurs on line 23, the Q output of the first D type should be a 0 as just described, and the rising edge of the L23WIND signal will clock this state into the second Dtype, resulting in its Q output being set to a logic 0 (GOOD sync).

If the sync from the VCR fails to occur in the time between the end of the last WIND signal and the start of the L23WIND signal, then the 2nd Dtype will see a 1 on its D input when the L23WIND signal goes high, and the Q output will be set to a 1 (BAD).

Figure 1

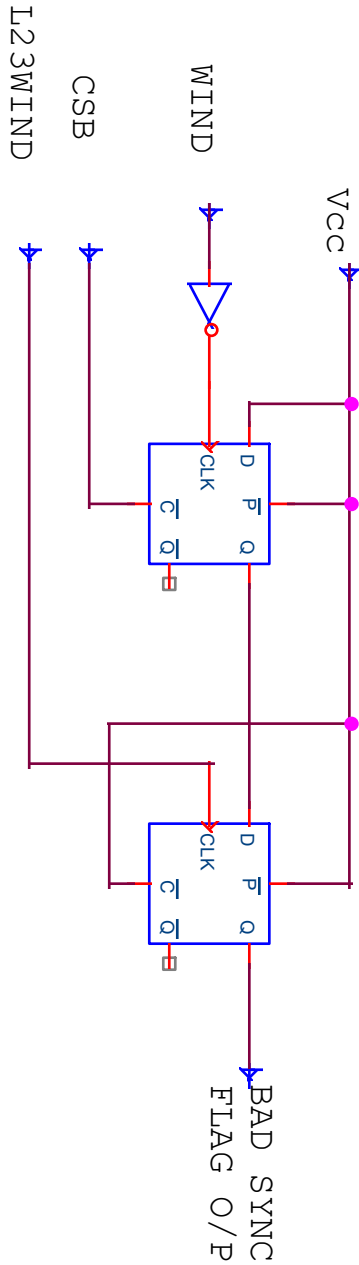


Figure 2

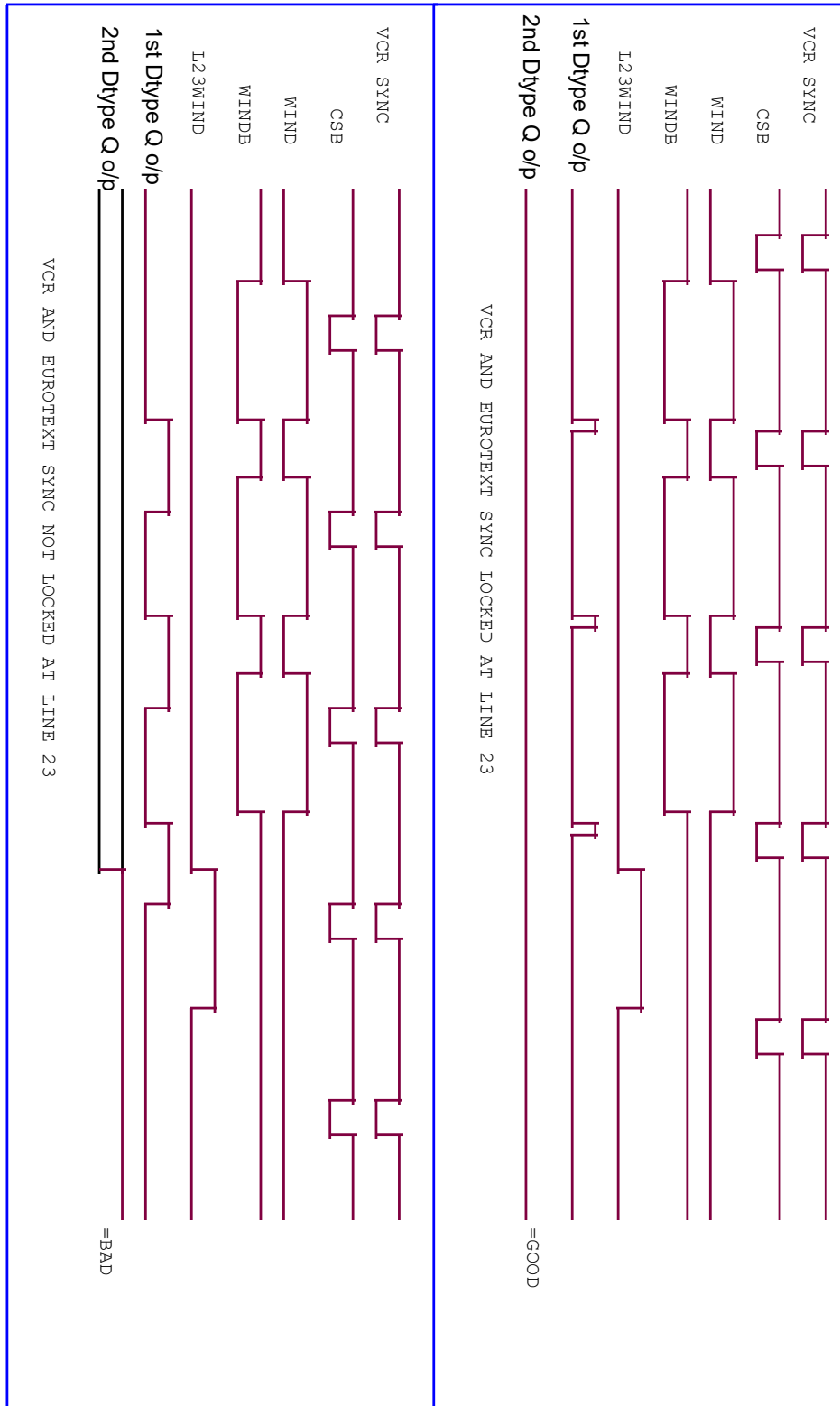
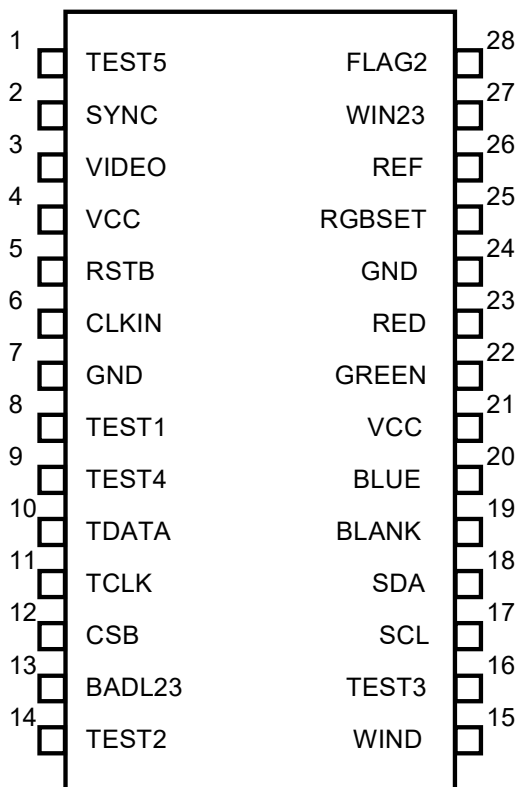


Figure 3



CF70207